The Interface Circuits Data Book

for

Design Engineers

Second Edition
1986 Supplement

TEXAS INSTRUMENTS

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INCORPORATED

LCC5921
71001-51-G

IMPORTANT NOTICES

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Information contained herein includes data previously published in:

The Interface Circuits Data Book, First Edition LCC4330
The Line Driver and Line Receiver Data Book, 1981 LCC4290A
The Peripheral Driver Data Book, 1981 LCC4280A
The Memory Interface Data Book, 1977 LCC4300
The Display Driver Data Book, 1977 LCC4310

Some corrections to the previously published data have been made in this book, which represents the most recent data on these interface circuits at the time of publication.

ISBN 0-89512-109-3
Library of Congress catalog number: 81-51166

General Information

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ALPHANUMERIC INDEX

*Future products, to be announced

ALPHANUMERIC INDEX

INTERFACE CIRCUITS INTERCHANGEABILITY GUIDE (MANUFACTURERS ARRANGED ALPHABETICALLY)

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

ADVANCED MICRO DEVICES

EXAMPLE OF NOMENCLATURE

AM	75325	N
Prefix	Device Type	Package Type
		N = Plastic DIP (second source designation for TI Plastic DIP)
		P = Plastic DIP
		J = Ceramic DIP (second source designation for TI Ceramic DIP)
		D = Ceramic DIP

AMD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
AM0026C		SN75369
AM1488	SN75188	
AM1489	SN75189	
AM1489A	SN75189A	
AM26LS31C	AM26LS31C	
AM26LS32C	AM26LS32AC	
AM26LS33C	AM26LS33AC	
AM26S10C	AM26S10C	
AM26S10M	AM26S10M	
AM26S11C	AM26S11C	
AM26S11M	AM26S11M	
AM5520	SN5520	
AM5521	SN5520	
AM5524	SN5524	
AM5525	SN5524	
AM7520	SN7520	
AM7521	SN7520	
AM7524	SN7524	
AM7525	SN7524	
AM7820A	SN55182	
AM7830	SN55183	
AM7831	DS7831	
AM7832	DS7832	
AM8820A	SN75182	
AM8830	SN75183	
AM8831	DS8831	
AM8832	DS8832	
AM8T26A		SN75136
AM9614C	SN75114	
AM9614M	SN55114	
AM9615C	SN75115	
AM9615M	SN55115	
AM55107B	SN55107B	
AM55108B	SN55108B	
AM55109	SN55109A	
AM55110	SN55110A	
AM55234	SN55234	
AM55235	SN55234	
AM55238	SN55238	
AM55239	SN55238	
AM55325	SN55325	
AM75107B	SN75107B	
AM75108B	SN75108B	
AM75109	SN75109A	
AM75110	SN75110A	
AM75207	SN75207	
AM75208	SN75208	
AM75234	SN75234	
AM75235	SN75234	
AM75238	SN75238	
AM75239	SN75238	
AM75325	SN75325	

FAIRCHILD

EXAMPLE OF NOMENCLATURE

75450B	D	C
Device Type	Package Type D = Ceramic DIP P = Plastic DIP R = Ceramic Mini DIP T = Plastic Mini DIP H = Metal Can F = Flat Package	Temperature Range C = Commercial 0°C to 70°C or 75°C M = Military −55°C to 125°C

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
μA8T13M	SN55121	
μA8T13C	SN75121	
μA8T14M	SN55122	
μA8T14C	SN75122	
μA8T23C	SN75123	
μA8T24C	SN75124	
μA1488C	SN75188	
μA1489C	SN75189	
μA1489AC	SN75189A	
5524M	SN5524	
5525M	SN5524	
5528M	SN5528	
5529M	SN5528	
5534M		SN55232
5535M		SN55232
5538M		SN55238
5539M		SN55238
7524C	SN7524	
7525C	SN7524	
7528C	SN7528	
7529C	SN7528	
7534C		SN75232
7535C		SN75232
7538C		SN75238
7539C		SN75238
9612C		SN75158
9614M	SN55114	
9614C	SN75114	
9615M	SN55115	
9615C	SN75115	
9616C		SN75188 / SN75150
9617C		SN75152 / SN75154 / SN75189 / SN75189A

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
9626C		SN75136
9627C		SN75152
9634C		SN75159
9636AC	uA9636AC	
9637AC	uA9637AC	
9637AM		SN55157
9638C	uA9638C	
9638M		SN55158
9640C	AM26S10C	
9640M	AM26S10M	
9641C	AM26S11C	
9641M	AM26S11M	
9643		SN75322 / SN75363
9644C		SN75361A
9664C	SN75492	
9665AC	SN75466	
9665C	ULN2001A	
9666AC	SN75467	
9666C	ULN2002A	
9667AC	SN75468	
9667C	ULN2003A	
9668AC	SN75469	
9668C	ULN2004A	
55107AM	SN55107A	
55107BM	SN55107B	
55108AM	SN55108A	
55108BM	SN55108B	
55109M	SN55109A	
55110M	SN55110A	
55121M	SN55121	
55122M	SN55122	

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
55224M		SN55234
55225M		SN55234
55232M	SN55232	
55233M	SN55232	
55234M	SN55234	
55235M	SN55234	
55238M	SN55238	
55239M	SN55238	
55325M	SN55325	
55326M	SN55326	
55327M	SN55327	
55450AM	SN55450B	
55450BM	SN55450B	
55451AM	SN55451B	
55451BM	SN55451B	
55452AM	SN55452B	
55452BM	SN55452B	
55453AM	SN55453B	
55453BM	SN55453B	
55454AM	SN55454B	
55454BM	SN55454B	
55460M	SN55460	
55461M	SN55461	
55462M	SN55462	
55463M	SN55463	
55464M	SN55464	
55470M	SN55470	
55471M	SN55471	
55472M	SN55472	
55473M	SN55473	
55474M	SN55474	
75107AC	SN75107A	
75107BC	SN75107B	
75108AC	SN75108A	
75108BC	SN75108B	
75109C	SN75109A	
75110C	SN75110A	
75112C	SN75112	
75121C	SN75121	
75122C	SN75122	
75123C	SN75123	
75124C	SN75124	
75150C	SN75150	

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
75154C	SN75154	
75207C	SN75207	
75208C	SN75208	
75224C		SN75234
75225C		SN75234
75232C	SN75232	
75233C	SN75232	
75234C	SN75234	
75235C	SN75234	
75238C	SN75238	
75239C	SN75238	
75325C	SN75325	
75326C	SN75326	
75327C	SN75327	
75430C	SN75430	
75431C	SN75431	
75432C	SN75432	
75433C	SN75433	
75434C	SN75434	
75450AC	SN75450B	
75450BC	SN75450B	
75451AC	SN75451B	
75451BC	SN75451B	
75452AC	SN75452B	
75452BC	SN75452B	
75453AC	SN75453B	
75453BC	SN75453B	
75454AC	SN75454B	
75454BC	SN75454B	
75460C	SN75460	
75461C	SN75461	
75462C	SN75462	
75463C	SN75463	
75464C	SN75464	
75470C	SN75470	
75471C	SN75471	
75472C	SN75472	
75473C	SN75473	
75474C	SN75474	
75491C	SN75491	
75491AC	SN75491A	
75492C	SN75492	
75492AC	SN75492A	

EXAMPLE OF NOMENCLATURE

ITT	75450	–5	D
Prefix	Device Type	Temperature Range –1 = –55°C to 125°C –5 = 0°C to 70°C	Package D = Ceramic DIP N = Plastic DIP

ITT	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ITT491	SN75491	
ITT492	SN75492	
ITT493	SN75493	
ITT494	SN75494	
ITT1488	SN75188	
ITT1489	SN75189	
ITT1489A	SN75189A	
ITT5520	SN5520	
ITT5521	SN5520	
ITT5522	SN5522	
ITT5523	SN5522	
ITT5524	SN5524	
ITT5525	SN5524	
ITT5528	SN5528	
ITT5529	SN5528	
ITT5534		SN55232
ITT5535		SN55232
ITT7520	SN7520	
ITT7521	SN7520	
ITT7522	SN7522	
ITT7523	SN7522	
ITT7524	SN7524	
ITT7525	SN7524	
ITT7528	SN7528	
ITT7529	SN7528	
ITT7534		SN75232
ITT7535		SN75232
ITT9614	SN75114	
ITT9615	SN75115	
ITT55107A	SN55107A	
ITT55107B	SN55107B	
ITT55108A	SN55108A	
ITT55108B	SN55108B	
ITT55109	SN55109A	
ITT55110	SN55110A	
ITT55138	SN55138	
ITT55234	SN55234	
ITT55235	SN55234	

ITT	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ITT55324	SN55324	
ITT55325	SN55325	
ITT55450	SN55450B	
ITT55451	SN55451B	
ITT55452	SN55452B	
ITT55453	SN55453B	
ITT55454	SN55454B	
ITT55460	SN55460	
ITT55461	SN55461	
ITT55462	SN55462	
ITT55463	SN55463	
ITT55464	SN55464	
ITT75107A	SN75107A	
ITT75107B	SN75107B	
ITT75108A	SN75108A	
ITT75108B	SN75108B	
ITT75109	SN75109A	
ITT75110	SN75110A	
ITT75138	SN75138	
ITT75207	SN75207	
ITT75208	SN75208	
ITT75234	SN75234	
ITT75235	SN75234	
ITT75322	SN75322	
ITT75324	SN75324	
ITT75325	SN75325	
ITT75450	SN75450B	
ITT75451	SN75451B	
ITT75452	SN75452B	
ITT75453	SN75453B	
ITT75454	SN75454B	
ITT75460	SN75460	
ITT75461	SN75461	
ITT75462	SN75462	
ITT75463	SN75463	
ITT75464	SN75464	
ITT9614	SN75114	
ITT9615	SN75115	

MOTOROLA

EXAMPLE OF NOMENCLATURE

MC	75325	P
Prefix	Device Type	Package
		P = Plastic DIP
		L = Ceramic DIP
		G = Metal Can
		F = Flat Package

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MMH0026C		SN75369
MC8T13	SN75121	
MC8T14	SN75122	
MC8T23	SN75123	
MC8T24	SN75124	
MC8T26		SN75136
MC1411	ULN2001A	
MC1412	ULN2002A	
MC1413	ULN2003A	
MC1416	ULN2004A	
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
MC26S10	AM26S10C	
MC26S11	AM26S11C	
MC3443		SN75138
MC3446	MC3446	
MC3447		SN75160A
MC3453		SN75110A
MC3481	SN75126	
MC3485	SN75130	
MC3486	MC3486	
MC3487	MC3487	
MC5522	SN5522	
MC5523	SN5522	
MC5524	SN5524	
MC5525	SN5524	
MC5528	SN5528	
MC5529	SN5528	
MC5534		SN55232
MC5535		SN55232
MC5538		SN55238
MC5539		SN55238
MC7522	SN7522	

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MC7523	SN7522	
MC7524	SN7524	
MC7525	SN7524	
MC7528	SN7528	
MC7529	SN7528	
MC7534		SN75232
MC7535		SN75232
MC7538		SN75238
MC7539		SN75238
MC55107	SN55107A	
MC55108	SN55108A	
MC55325	SN55325	
MC75107	SN75107A	
MC75108	SN75108A	
MC75109	SN75109A	
MC75110	SN75110A	
MC75140	SN75140	
MC75325	SN75325	
MC75358	SN75368	
MC75365	SN75365	
MC75368	SN75368	
MC75450	SN75450B	
MC75451	SN75451B	
MC75452	SN75452B	
MC75453	SN75453B	
MC75454	SN75454B	
MC75460	SN75460	
MC75461	SN75461	
MC75462	SN75462	
MC75463	SN75463	
MC75464	SN75464	
MC75491	SN75491	
MC75492	SN75492	

NATIONAL

EXAMPLE OF NOMENCLATURE

DS	75325	N
Prefix	Device Type	Package
		N = Plastic DIP
		J = Ceramic DIP
		W = Flat Package
		H = Metal Can

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS0026C		SN75369
DS1488	SN75188	
DS1489	SN75189	
DS1489A	SN75189A	
DS1611		SN55471
DS1612		SN55472
DS1613		SN55473
DS1614		SN55474
DS26LS31	AM26LS31C	
DS26LS32	AM26LS32AC	
DS26S10C	AM26S10C	
DS26S10M	AM26S10M	
DS26S11C	AM26S11C	
DS26S11M	AM26S11M	
DS3488	MC3486	
DS3487	MC3487	
DS3611		SN75471
DS3612		SN75472
DS3613		SN75473
DS3614		SN75474
DS3629		SN75324
DS5520	SN5520	
DS5520A		SN5520
DS5521	SN5520	
DS5522	SN5522	
DS5522A		SN5522
DS5523	SN5522	
DS5524	SN5524	
DS5524A		SN5524
DS5526	SN5524	
DS5528	SN5528	
DS5528A		SN5528
DS5529	SN5528	
DS5534		SN55232
DS5534A		SN55232
DS5535		SN55232
DS5538		SN55238
DS5538A		SN55238

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS5539		SN55238
DS7520	SN7520	
DS7520A		SN7520
DS7521	SN7520	
DS7522	SN7522	
DS7522A		SN7522
DS7523	SN7522	
DS7524	SN7524	
DS7524A		SN7524
DS7525	SN7524	
DS7528	SN7528	
DS7528A		SN7528
DS7529	SN7528	
DS7534		SN75232
DS7534A		SN75232
DS7535		SN75232
DS7538		SN75238
DS7538A		SN75238
DS7539		SN75238
DS7800	SN55180	
DS7820	SN55182	
DS7820A	SN55182	
DS7830	SN55183	
DS7831	DS7831	
DS7832	DS7832	
DS8T26A	NBT26A	
DS88LS20		SN75182
DS8820	SN75182	
DS8820A	SN75182	
DS8830	SN75183	
DS8831	DS8831	
DS8832	DS8832	
DS8880	SN75480	
DS55107	SN55107B	
DS55108	SN55108B	
DS55109	SN55109A	
DS55110	SN55110A	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS55113	SN55113	
DS55114	SN55114	
DS55115	SN55115	
DS55121	SN55121	
DS55122	SN55122	
DS55325	SN55325	
DS55450	SN55450B	
DS55451	SN55451B	
DS55452	SN55452B	
DS55453	SN55453B	
DS55454	SN55454B	
DS55460	SN55460	
DS55461	SN55461	
DS55462	SN55462	
DS55463	SN55463	
DS55464	SN55464	
DS75107	SN75107B	
DS75108	SN75108B	
DS75109	SN75109A	
DS75110	SN75110A	
DS75113	SN75113	
DS75114	SN75114	
DS75115	SN75115	
DS75121	SN75121	
DS75122	SN75122	
DS75123	SN75123	
DS75124	SN75124	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS75150	SN75150	
DS75154	SN75154	
DS75207	SN75207B	
DS75208	SN75208B	
DS75322	SN75322	
DS75324	SN75324	
DS75325	SN75325	
DS75361	SN75361A	
DS75362		SN75365
DS75364	SN75364	
DS75365	SN75365	
DS75450	SN75450B	
DS75451	SN75451B	
DS75452	SN75452B	
DS75453	SN75453B	
DS75454	SN75454B	
DS75460	SN75460	
DS75461	SN75461	
DS75462	SN75462	
DS75463	SN75463	
DS75464	SN75464	
DS75491	SN75491	
DS75492	SN75492	
DS75493	SN75493	
DS75494	SN75494	
DS78LS20		SN55182
DS88LS20		SN75182

SIGNETICS

EXAMPLE OF NOMENCLATURE

75454B	V
Device Type	Package
	A = 14 pin Plastic DIP
	FH = 14 pin Ceramic DIP
	V = 8 pin Plastic DIP
	T = 8 pin Metal Can
	B = 16 pin Plastic DIP
	FJ = 16 pin Ceramic DIP

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
N8T13	SN75121	
N8T14	SN75122	
N8T15		SN75150
N8T16		SN75152
N8T23	SN75123	
N8T24	SN75124	
N8T26	N8T26	
N8T26A	N8T26A	
S8T13	SN55121	
S8T14	SN55122	55454B
DM7820	SN55182	
DM7830	SN55183	
DM8820	SN75182	
DM8830	SN75183	
DM8880	SN75480	
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
3207A		SN75365
3207A-1		SN75365
7520	SN7520	
7521	SN7520	

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
7522	SN7522	
7523	SN7522	
7524	SN7524	
7525	SN7524	
55325	SN55325	
55450B	SN55450B	
55451B	SN55451B	
55452B	SN55452B	
55453B	SN55453B	
55454B	SN55454B	
75S107		SN75107A
75S108		SN75108A
75S207		SN75207
75S208		SN75208
75324	SN75324	
75325	SN75325	
75361A	SN75361A	
75450B	SN75450B	
75451B	SN75451B	
75452B	SN75452B	
75453B	SN75453B	
75454B	SN75454B	

SPRAGUE

EXAMPLE OF NOMENCLATURE:

ULN	2068	B
Prefix	Type Number	Package
		A = Plastic DIP (N designation for TI)
		B = Plastic DIP with heatsink lead frame (NE designation for TI)
		M = Plastic mini-DIP (P designation for TI)
		J = Ceramic DIP (TI designation)

SPRAGUE	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
UDN2841	UDN2841	
UDN2845	UDN2845	
UDN3611	SN75471	
UDN3612	SN74572	
UDN3613	SN75473	
UDN3614	SN75474	
UDN5711	SN75476	
UDN5712	SN75477	
UDN5713	SN75478	
UDN5714	SN75479	
ULN2001A	ULN2001A	
ULN2002A	ULN2002A	

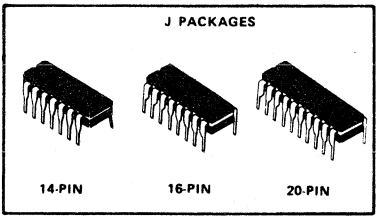
SPRAGUE	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ULN2003A	ULN2003A	
ULN2004A	ULN2004A	
ULN2005A	ULN2005A	
ULN2064	ULN2064	
ULN2065	ULN2065	
ULN2066	ULN2066	
ULN2067	ULN2067	
ULN2068	ULN2068	
ULN2069	ULN2069	
ULN2074	ULN2074	
ULN2075	ULN2075	

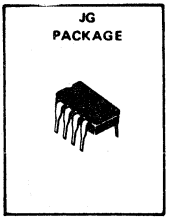
Thermal Information

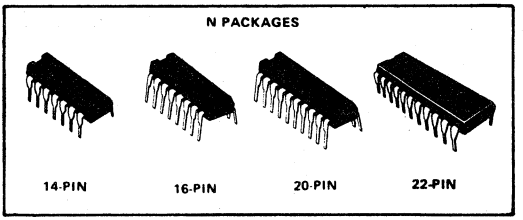
THERMAL RESISTANCE

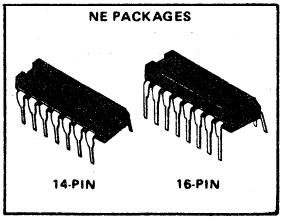
PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
JG ceramic dual-in-line† (alloy-mounted chips)	8	26†	119†
N plastic dual-in-line	14 thru 20	44	108
	22	39	94
NE plastic dual-in-line	14, 16	10	60
P plastic dual-in-line	8	45	125
W ceramic flat package	14		125

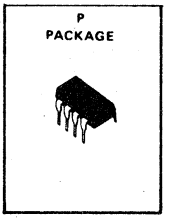
†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM," or a suffix of "/883" have alloy mounted chips.

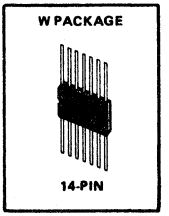








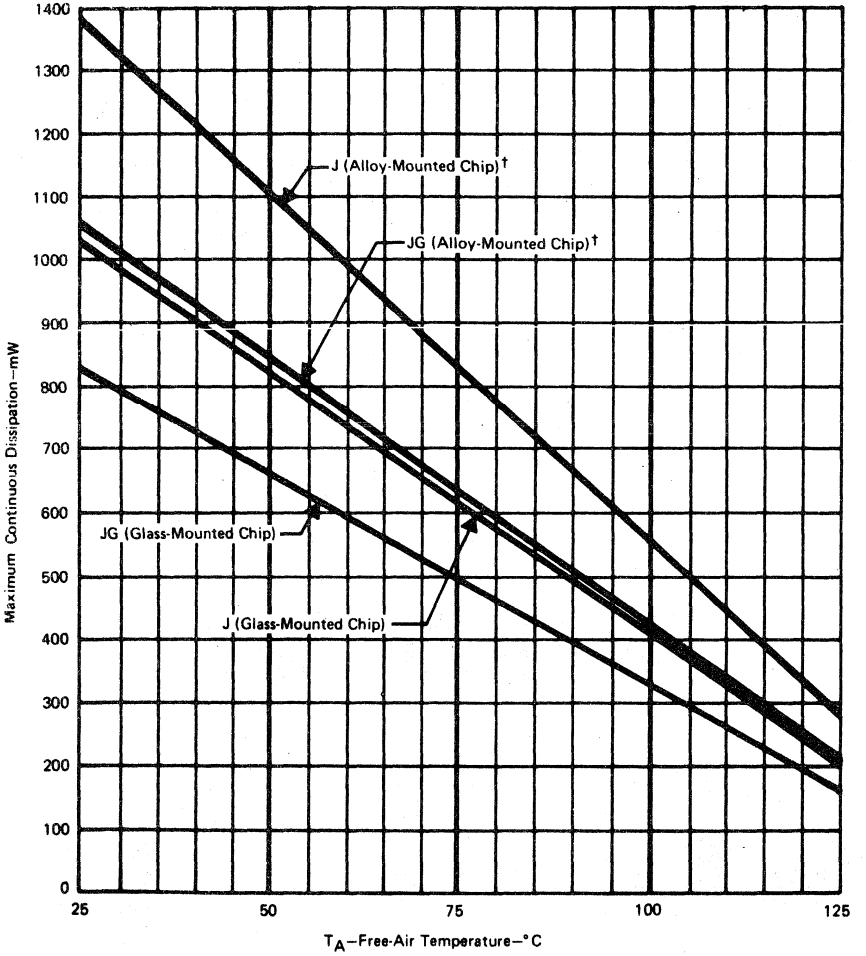




CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

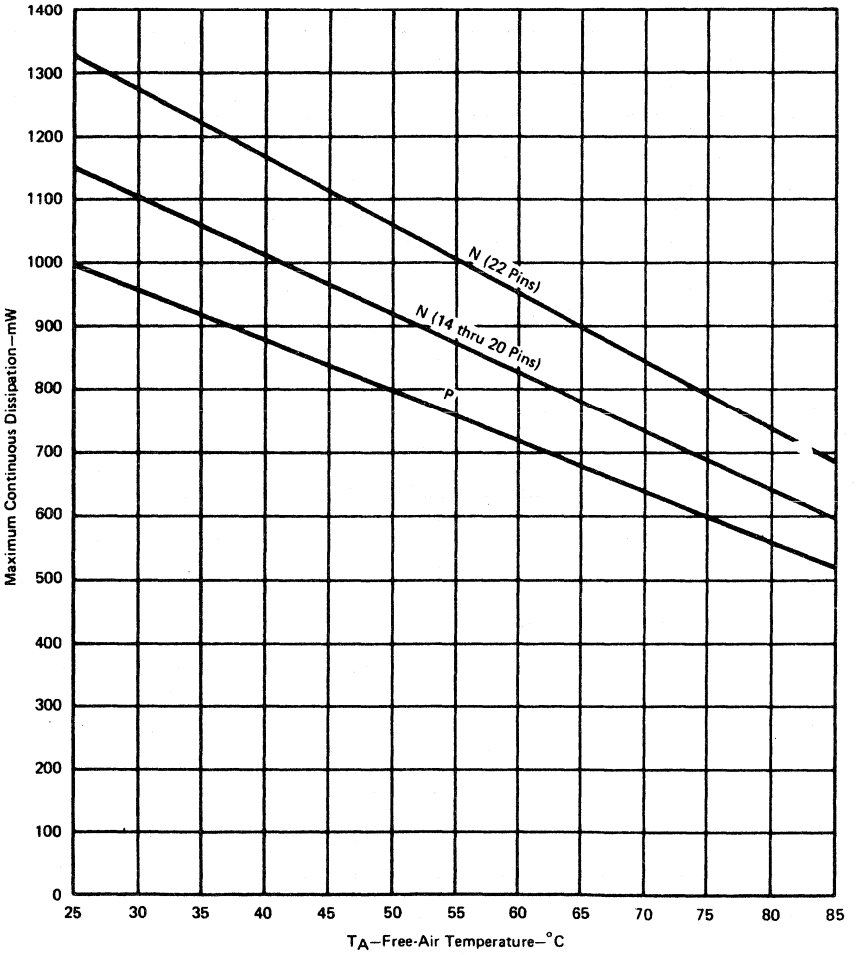
DISSIPATION DERATING CURVE



†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883" have alloy-mounted chips.

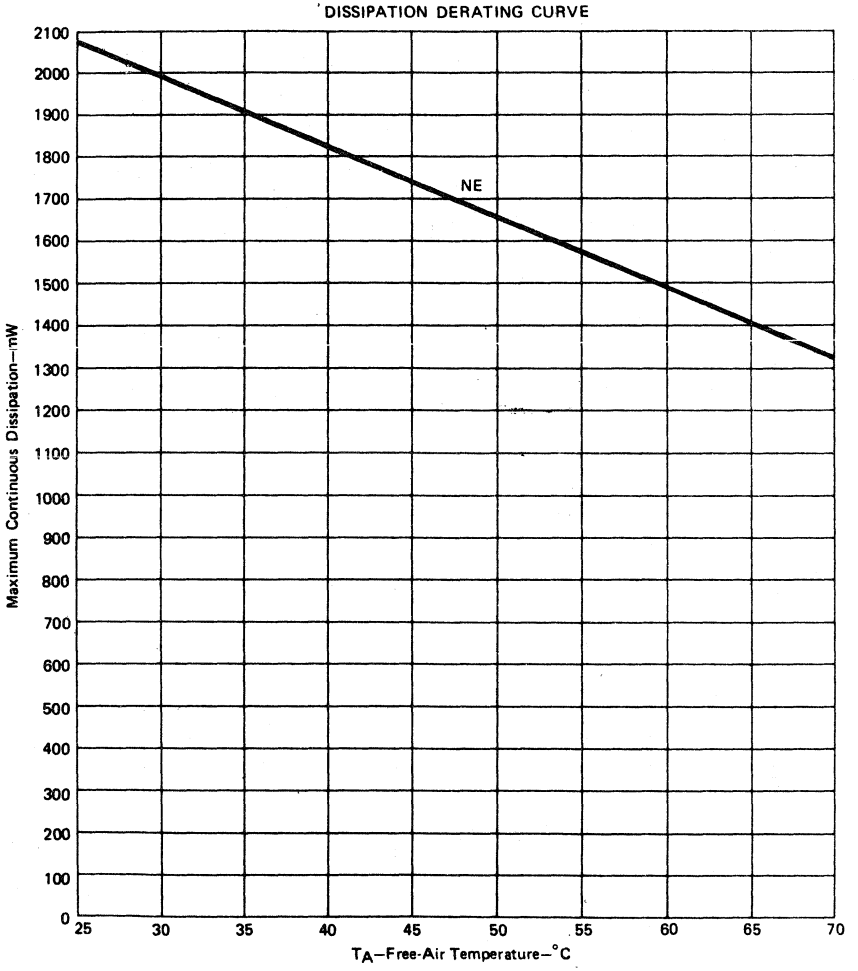
PLASTIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



PLASTIC MEDIUM-POWER DUAL-IN-LINE PACKAGE

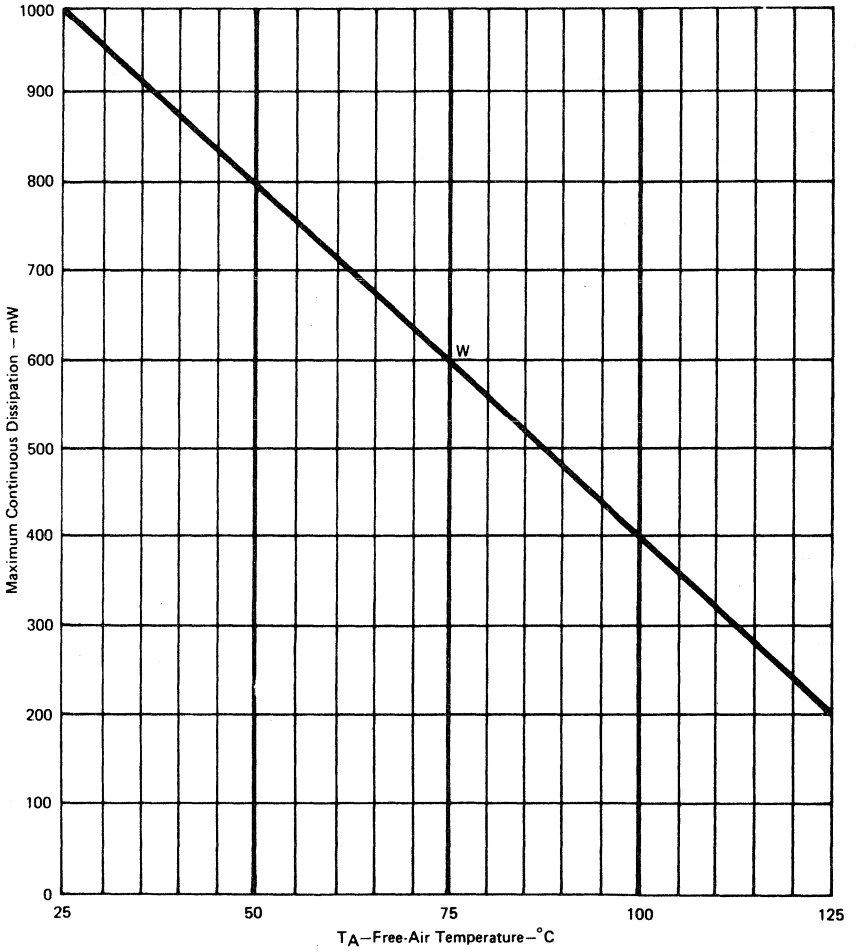
These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



CERAMIC FLAT PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



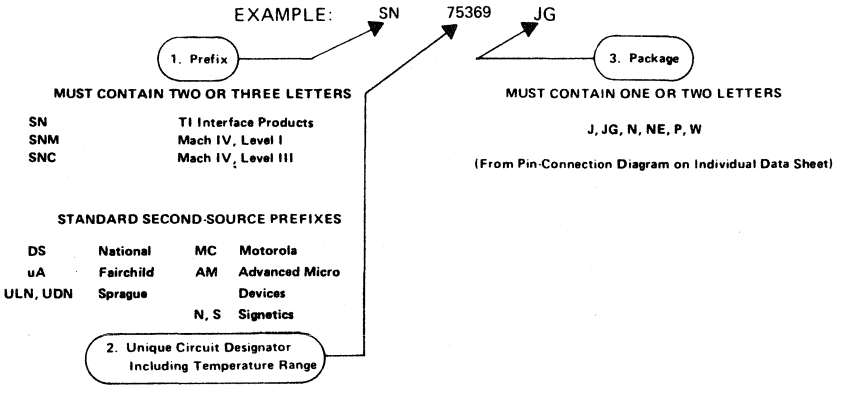
Ordering Instructions and Mechanical Data

3

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book apply for the circuit type(s) listed in the page heading, unless otherwise noted, regardless of package. The availability of a circuit function in a particular package is indicated by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.



Circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier
- Sectioned Cardboard Box
- Individual Plastic Box

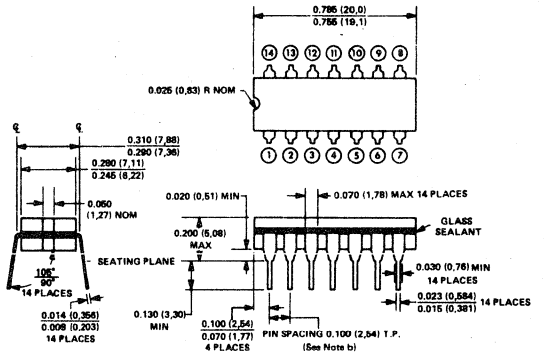
ORDERING INSTRUCTIONS AND MECHANICAL DATA

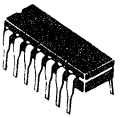
J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 20-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

3

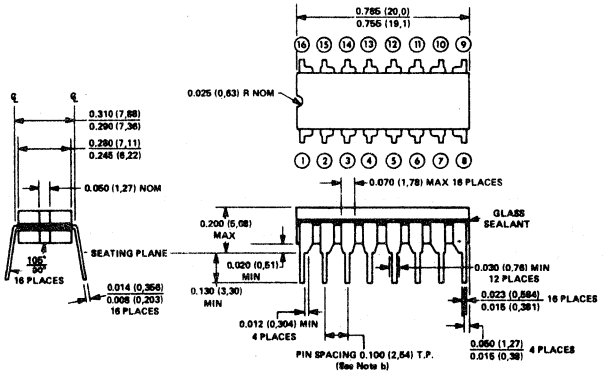
14-PIN J CERAMIC

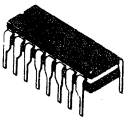




Falls within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC

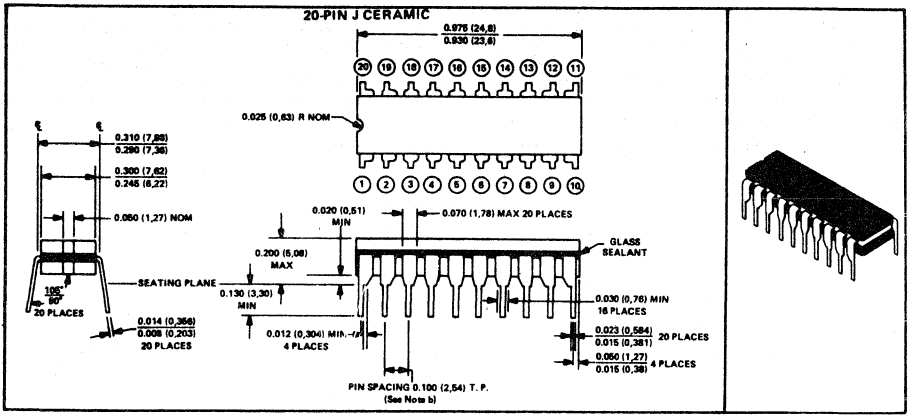




NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

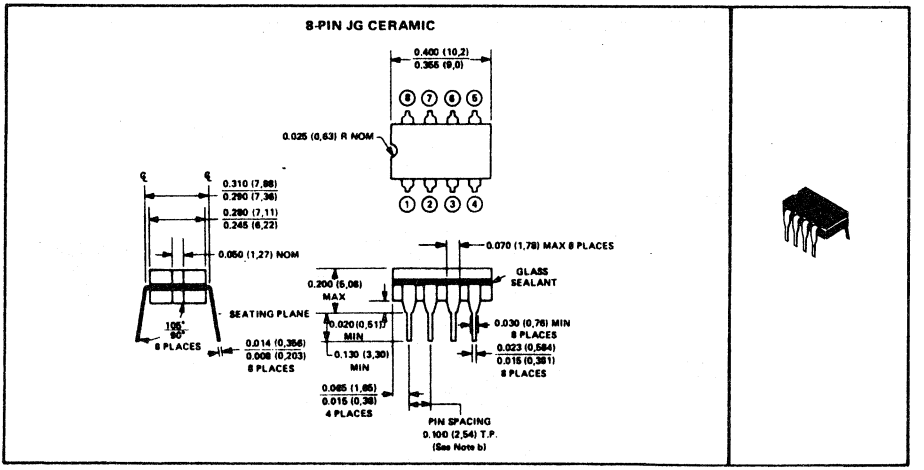
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

J ceramic dual-in-line packages (continued)



JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



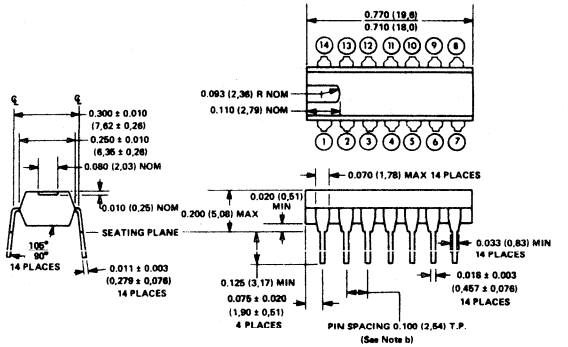
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

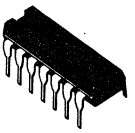
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

N and NE plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14- or 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly. The NE package has internal metal tabs connecting the two or three central leads on each side for better heat dissipation.

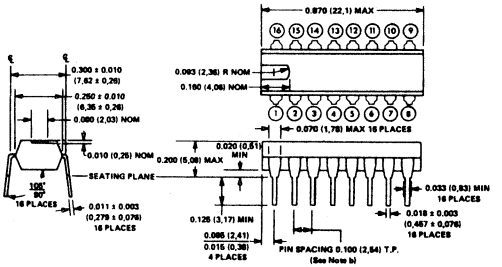
14-PIN N AND NE PLASTIC

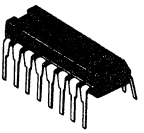




Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN N AND NE PLASTIC



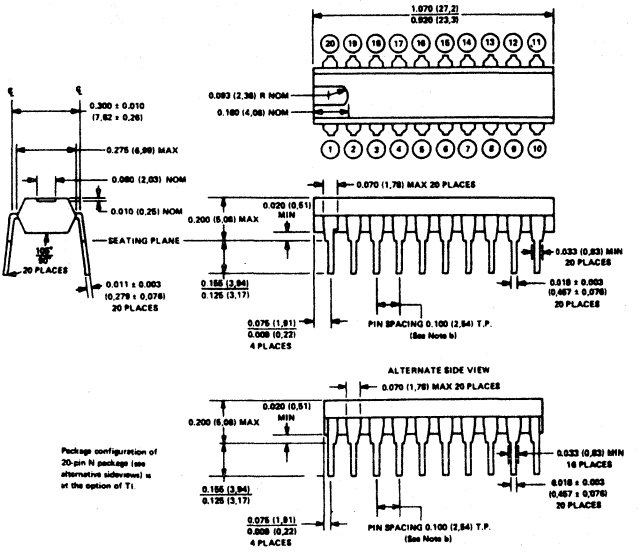


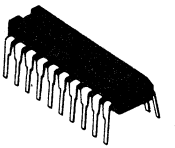
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

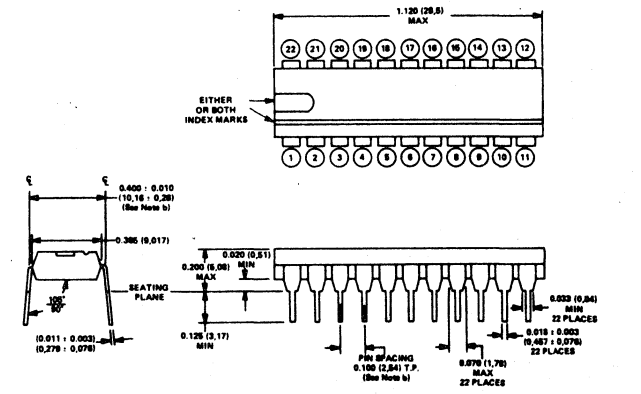
N dual-in-line plastic packages (continued)

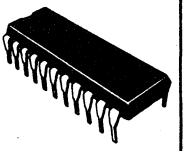
20-PIN N PLASTIC





22-PIN N PLASTIC





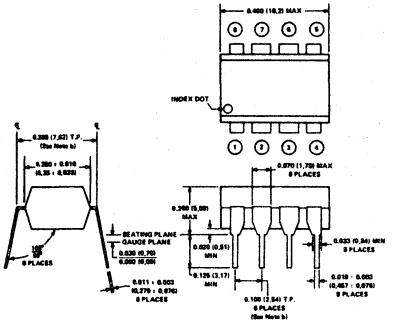
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

ORDERING INSTRUCTIONS AND MECHANICAL DATA

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated in an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated under high-humidity conditions. This package is intended for insertion in mounting hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC

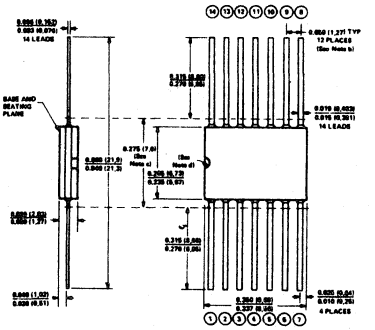


NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is within 0.005 (0,127) radius of true position at the gauge plane with maximum material condition and unit installed.

W ceramic flat package

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require an additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC FLAT PACKAGE



Falls within JEDEC MO-004AA Dimensions

NOTES: a. All dimensions are shown in inches and parenthetically in millimeters. Inch dimensions govern.
b. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
c. This dimension determines a zone within which all body and lead irregularities lie.
d. Index point is provided on cap for terminal identification only.

Peripheral Drivers

PERIPHERAL DRIVER SELECTION GUIDE

DRIVERS WITH LOGIC GATES

Military Temperature Range (−55°C to 125°C)

SWITCHING VOLTAGE	MAX RECOMMENDED OUTPUT CURRENT	DRIVERS PER PACKAGE	INTERNAL CLAMP DIODES	LOGIC GATE FUNCTION				PAGE NUMBER
				AND	NAND	OR	NOR	
20 V	300 mA	2	–	SN55450B				4-51
				SN55451B	SN55452B	SN55453B	SN55454B	4-51
30 V	300 mA	2	–	SN55460				4-63
				SN55461	SN55462	SN55463	SN55464	4-63
55 V	300 mA	2	–	SN55470				4-81
				SN55471	SN55472	SN55473	SN55474	4-81

4

Commercial Temperature Range (0°C to 70°C)

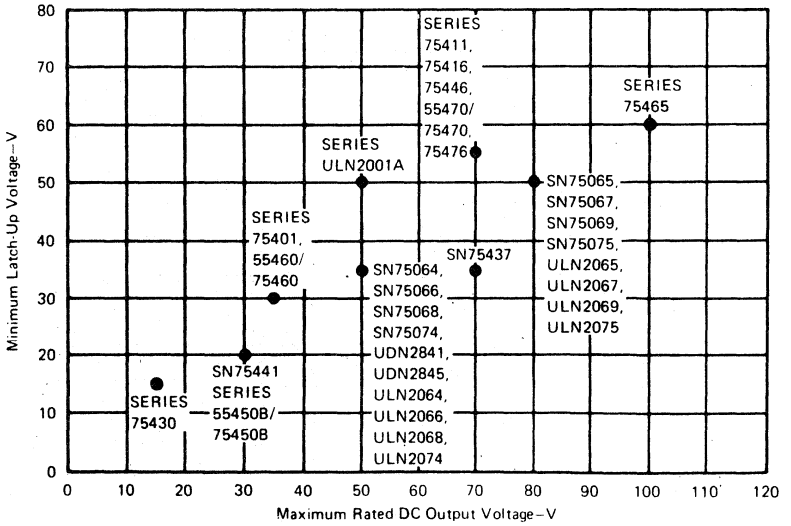
SWITCHING VOLTAGE	MAX RECOMMENDED OUTPUT CURRENT	DRIVERS PER PACKAGE	INTERNAL CLAMP DIODES	LOGIC GATE FUNCTION				PAGE NUMBER
				AND	NAND	OR	NOR	
15 V	300 mA	2	–	SN75430				4-29
				SN75431	SN75432	SN75433	SN75434	4-29
20 V	100 mA	2	–			SN75441		4-43
	300 mA	2	–	SN75450B				4-51
				SN75451B	SN75452B	SN75453B	SN75454B	4-51
30 V	300 mA	2	–	SN75460				4-63
				SN75461	SN75462	SN75463	SN75464	4-63
	500 mA	2	–	SN75401	SN75402	SN75403	SN75404	4-17
35 V	500 mA	4	YES		SN75437			4-39
55 V	300 mA	2	–	SN75470				4-81
				SN75471	SN75472	SN75473	SN75474	4-81
			YES	SN75476	SN75477	SN75478	SN75479	4-91
	350 mA	2	YES	SN75446	SN75447	SN75448	SN75449	4-47
	500 mA	2	–	SN75411	SN75412	SN75413	SN75414	4-21
			YES	SN75416	SN75417	SN75418	SN75419	4-25

DRIVERS WITHOUT LOGIC GATES

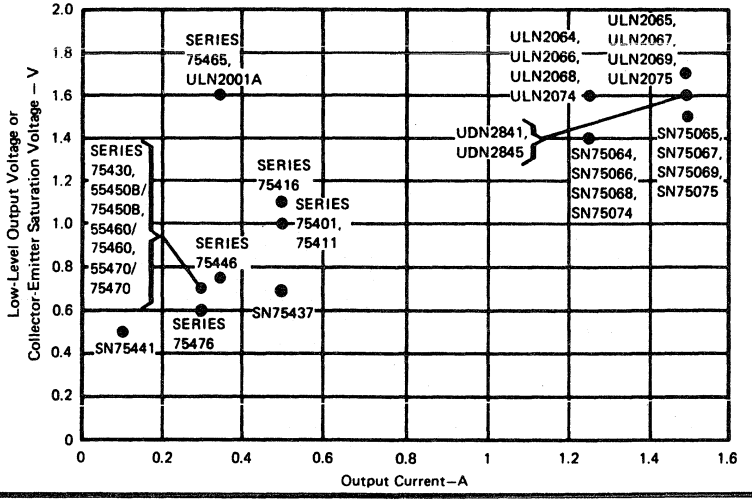
Commercial Temperature Range (0°C to 70°C)

SWITCHING VOLTAGE	MAX RECOMMENDED OUTPUT CURRENT	DRIVERS PER PACKAGE	INTERNAL CLAMP DIODES	DEVICE TYPES	PAGE NUMBER
35 V	1.25 A	4	YES	ULN2064 ULN2066	4-105
			YES	ULN2068	4-109
			YES	SN75064 SN75066	4-5
			YES	SN75068	4-9
			–	SN75074	4-13
			–	ULN2074	4-113
	1.5 A	4	–	UDN2841 UDN2845	4-95
50 V	350 mA	7	YES	ULN2001A ULN2002A ULN2003A	4-97
			YES	ULN2004A ULN2005A	4-97
	1.5 A	4	YES	ULN2065 ULN2067	4-105
			YES	ULN2069	4-109
			YES	SN75065 SN75067	4-5
			YES	SN75069	4-9
			–	SN75075	4-13
			–	ULN2075	4-113
60 V	350 mA	7	YES	SN75465 SN75466 SN75467	4-73
			YES	SN75468 SN75469	4-73

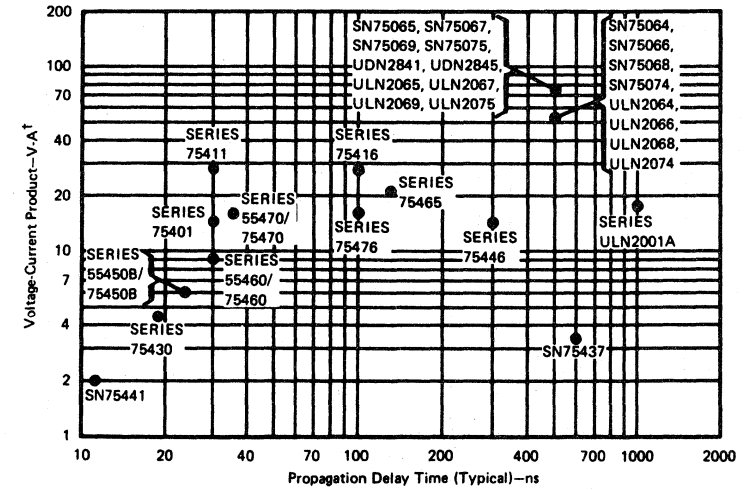
VOLTAGE CAPABILITY
OF PERIPHERAL DRIVERS



OUTPUT VOLTAGE
vs
OUTPUT CURRENT



VOLTAGE CURRENT PRODUCT†
vs
PROPAGATION DELAY TIME



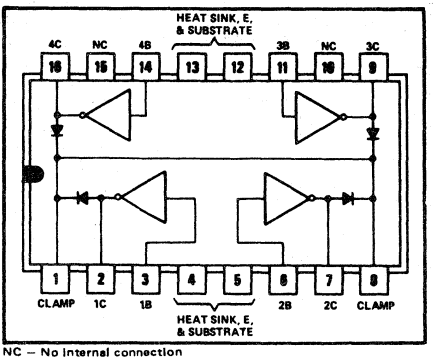
†This is the product of the minimum latch-up voltage and the maximum recommended output current.

TYPES SN75064, SN75065, SN75066, SN75067
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12788, NOVEMBER 1980—REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- SN75064 and SN75065 Have TTL-and DTL-Compatible Inputs
- SN75066 and SN75067 Have CMOS-and PMOS-Compatible Inputs
- Functionally Interchangeable with ULN2064 thru ULN2067, Respectively

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC — No internal connection

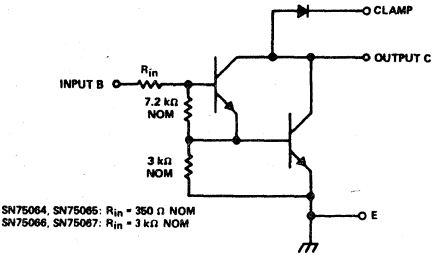
description

The SN75064, SN75065, SN75066, and SN75067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The SN75064 and SN75065 are intended for use with TTL, DTL, and 5-volt MOS logic. The SN75066 and SN75067 are intended for use with PMOS and higher voltage CMOS logic.

The SN75064 and SN75067 are characterized for operation from 0°C to 70°C.

schematic (each darlington pair)



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	SN75064	SN75065	SN75066	SN75067	UNIT
Collector-emitter voltage	50	80	50	80	V
Input voltage (see Note 1)	15	15	30	30	V
Peak collector current (see Figures 11, 12, and 13)	1.5	1.5	1.5	1.5	A
Input current	25	25	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

4

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN75064		SN75065		SN75066		SN75067		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100				100			μA
			V_{CE} = 50 V, T_A = 70°C		500				500			
			V_{CE} = 80 V				100				100	
			V_{CE} = 80 V, T_A = 70°C				500				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3					mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6					
			V_I = 5 V					0.9	1.8	0.9	1.8	
			V_I = 12 V					2.75	5.2	2.75	5.2	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2		6.5		6.5	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.5		2.5		10		10	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.13		1.13		1.13		1.13	V
			I_I = 935 μA, I_C = 750 mA		1.25		1.25		1.25		1.25	
			I_I = 1.25 mA, I_C = 1 A		1.4		1.4		1.4		1.4	
			I_I = 2 mA, I_C = 1.25 A, See Note 3		1.6				1.6			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 3				1.7				1.7	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50				50			μA
			V_R = 50 V, T_A = 70°C		100				100			
			V_R = 80 V				50				50	
			V_R = 80 V, T_A = 70°C				100				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75		1.75		1.75	V
			I_F = 1.5 A, See Note 3		2		2		2		2	

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. t_w = 10 ms, duty cycle < 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

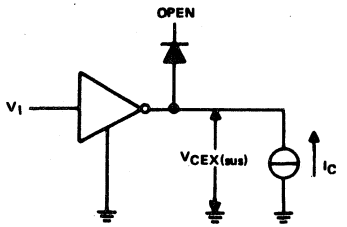


FIGURE 1–$V_{CEX(sus)}$

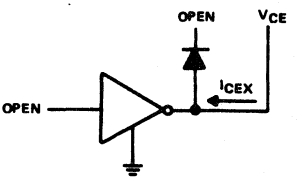


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

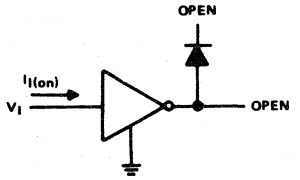


FIGURE 3–$I_{I(on)}$

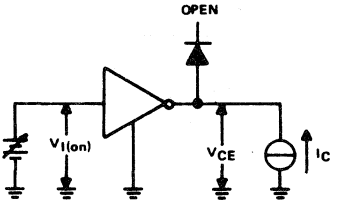


FIGURE 4–$V_{I(on)}$

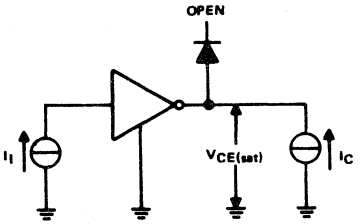


FIGURE 5–$V_{CE(sat)}$

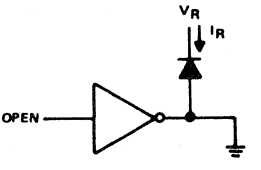


FIGURE 6–I_R

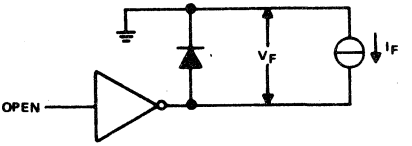
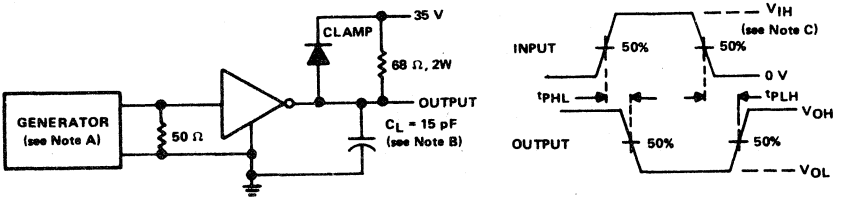


FIGURE 7–V_F



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.
C. V_{IH} = 2.5 V for SN75064 and SN75065. V_{IH} = 10 V for SN75066 and SN75067.

FIGURE 8 – SWITCHING TIMES

ELECTRICAL CHARACTERISTICS

SN75064, SN75065

INPUT CURRENT vs INPUT VOLTAGE

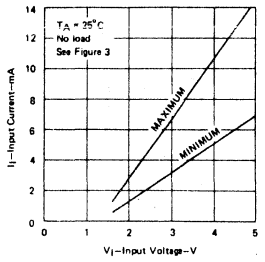


FIGURE 9

SN75066, SN75067

INPUT CURRENT vs INPUT VOLTAGE

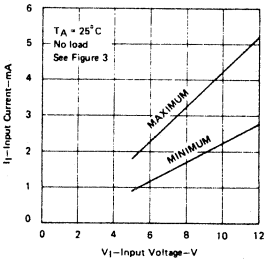


FIGURE 10

COLLECTOR CURRENT vs BASE CURRENT

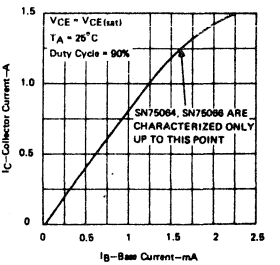


FIGURE 11

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

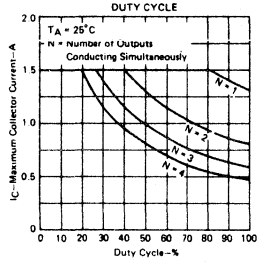


FIGURE 12

MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

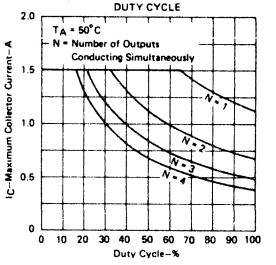


FIGURE 13

MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

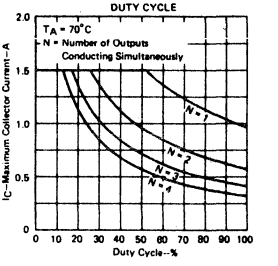


FIGURE 14

TYPICAL APPLICATION DATA

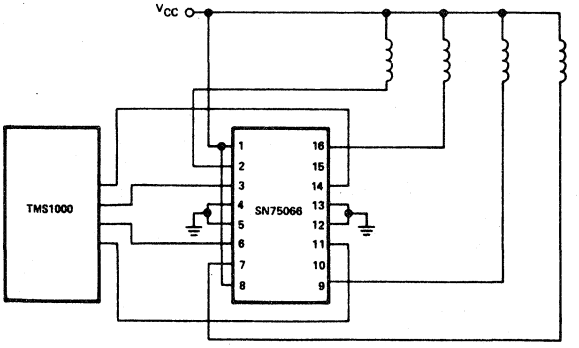


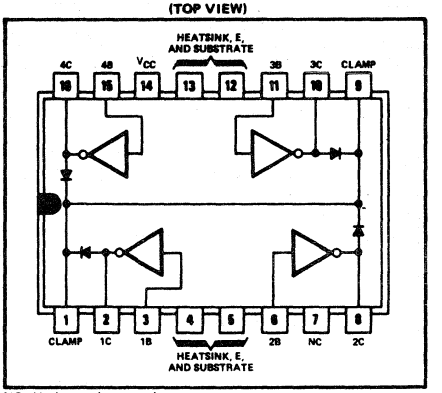
FIGURE 15–RELAY DRIVER INTERFACE

TYPES SN75068, SN75069
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO DL-S 12789, DECEMBER 1979 – REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible with TTL and 5-Volt CMOS
- Functionally Interchangeable with ULN2068 and ULN2069

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

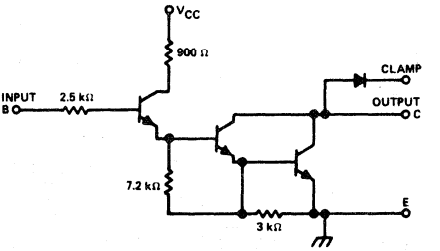
description

The SN75068 and SN75069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-volt CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The SN75068 and SN75069 can sink up to 1.5 amperes per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge).

The SN75068 and SN75069 are characterized for operation from 0°C to 70°C.

schematic (each switch)



Resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	SN75068	SN75069	UNIT
Collector-emitter voltage	50	80	V
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	15	15	V
Peak collector current (see Figures 10, 11, and 12)	1.5	1.5	A
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75068 MIN	SN75068 MAX	SN75069 MIN	SN75069 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V,	I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V			100			μA
			V_{CE} = 50 V,	T_A = 70°C		500			
			V_{CE} = 80 V					100	
			V_{CE} = 80 V,	T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V			250		250	μA
			V_I = 3.75 V			1000		1000	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, See Note 3	I_C = 1.5 A,		2.4		2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	V_I = 2.4 V,	I_C = 500 mA		1.13		1.13	V
			V_I = 2.4 V,	I_C = 750 mA		1.25		1.25	
			V_I = 2.4 V,	I_C = 1 A		1.4		1.4	
			V_I = 2.4 V, See Note 3	I_C = 1.25 A,		1.6			
			V_I = 2.4 V, See Note 3	I_C = 1.5 A,				1.7	
I_R	Clamp-diode reverse current	6	V_R = 50 V			50			μA
			V_R = 50 V,	T_A = 70°C		100			
			V_R = 80 V					50	
			V_R = 80 V,	T_A = 70°C				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A			1.75		1.75	V
			I_F = 1.5 A,	See Note 3		2		2	
I_{CC}	Supply current (only one switch conducting)	8	V_I = 2.4 V,	I_C = 500 mA		6		6	mA

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

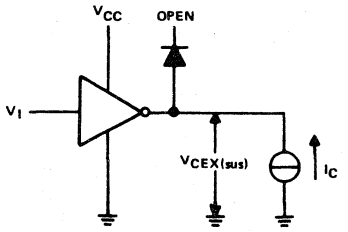


FIGURE 1–$V_{CEX(sus)}$

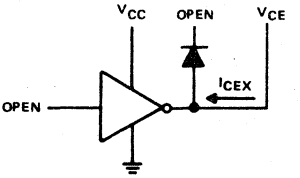


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

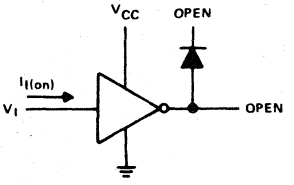


FIGURE 3–$I_{I(on)}$

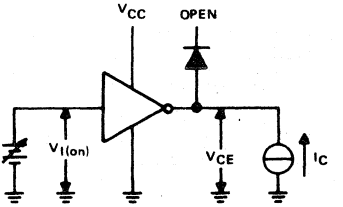


FIGURE 4–$V_{I(on)}$

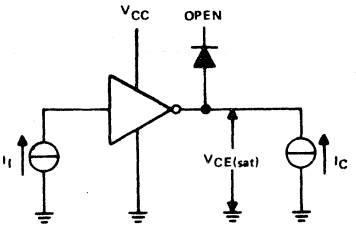


FIGURE 5–$V_{CE(sat)}$

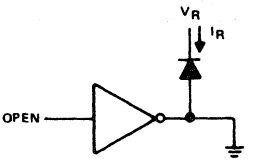


FIGURE 6–I_R

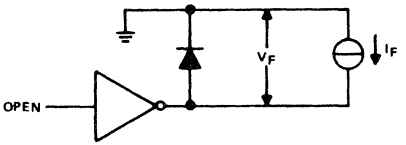


FIGURE 7–V_F

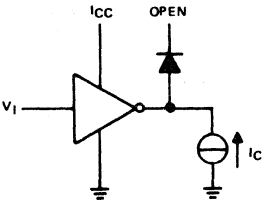
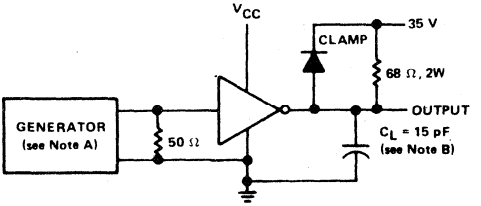
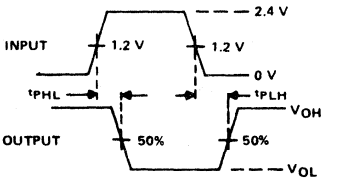


FIGURE 8–I_{CC}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 9–SWITCHING TIMES

THERMAL INFORMATION

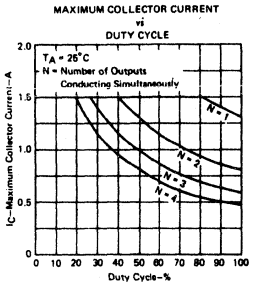


FIGURE 10

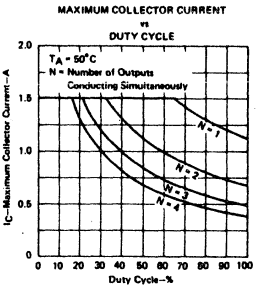


FIGURE 11

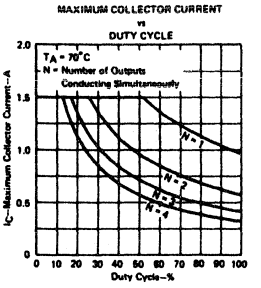


FIGURE 12

TYPICAL APPLICATION DATA

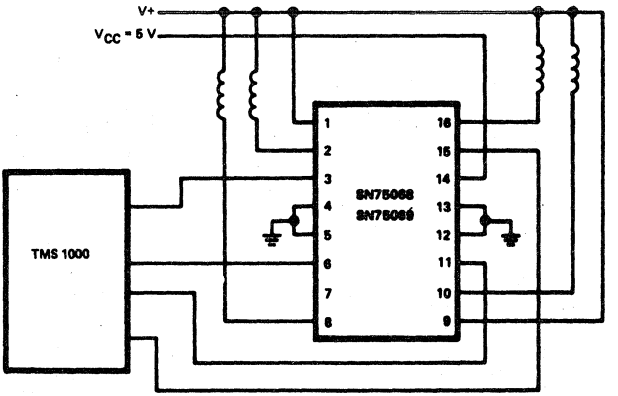


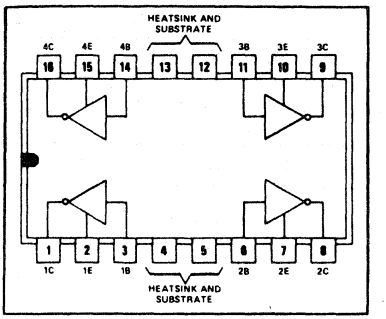
FIGURE 13—RELAY DRIVER INTERFACE

TYPES SN75074, SN75075
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12792, NOVEMBER 1980 – REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible With TTL or 5-V CMOS
- Functionally Interchangeable with ULN2074 and ULN2075

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



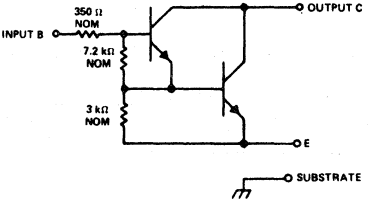
description

The SN75074 and SN75075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 amperes for each darlington pair.

The SN75074 and SN75075 are unique general purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

The SN75074 and SN75075 are characterized for operation from 0°C to 70°C.

schematic (each switch)



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2074	ULN2075	UNIT
Collector-emitter voltage	50	80	V
Input voltage with respect to substrate	30	60	V
Peak collector current (see Figures 9, 10, and 11)	1.5	1.5	A
Input current	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN75074 MIN	SN75074 MAX	SN75075 MIN	SN75075 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3	mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 2		2.5		2.5	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.13		1.13	V
			I_I = 935 μA, I_C = 750 mA		1.25		1.25	
			I_I = 1.25 mA, I_C = 1 A		1.4		1.4	
			I_I = 2 mA, I_C = 1.25 A, See Note 2		1.6			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 2				1.7	

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle < 10%.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

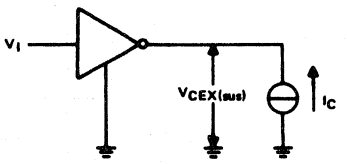


FIGURE 1–$V_{CEX(sus)}$

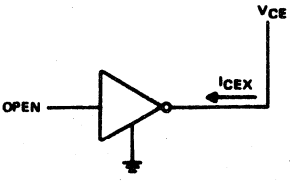


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

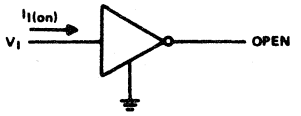


FIGURE 3–$I_{I(on)}$

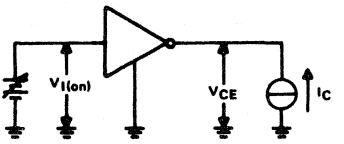


FIGURE 4–$V_{I(on)}$

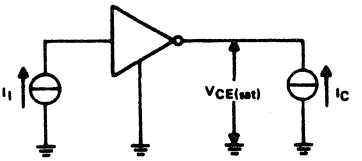
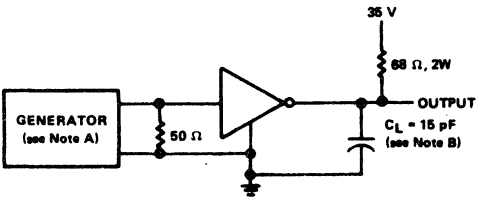
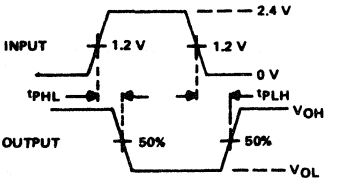


FIGURE 5–$V_{CE(sat)}$



TEST CIRCUITS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

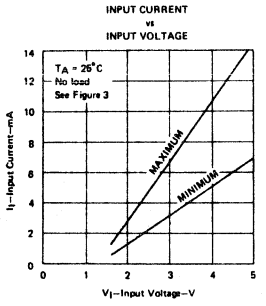


FIGURE 7

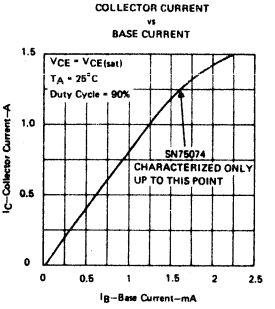


FIGURE 8

THERMAL INFORMATION

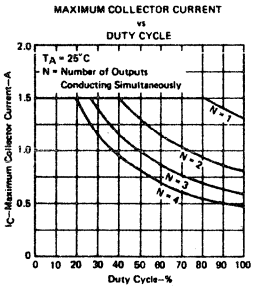


FIGURE 9

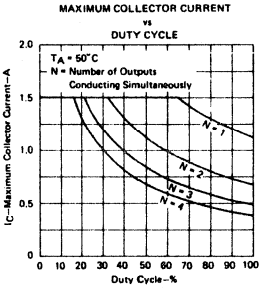


FIGURE 10

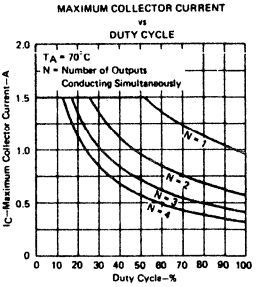


FIGURE 11

TYPICAL APPLICATION DATA

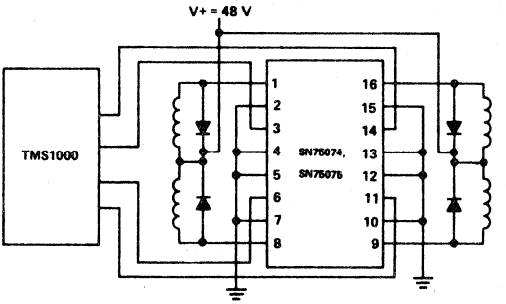


FIGURE 12–RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES

SERIES 75401
DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12239, APRIL 1975 – REVISED DECEMBER 1976

PERIPHERAL DRIVERS
FOR HIGH-VOLTAGE, VERY HIGH-CURRENT DRIVER APPLICATIONS

performance

- 2-W Dissipation Rating
- Characterized for Use to 500 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

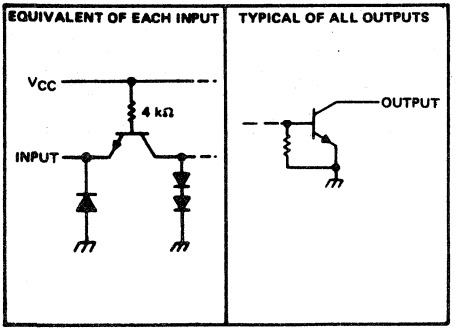
ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltage

description

Series 75401 dual peripheral drivers are a family of versatile devices designed for use in systems that employ DTL or TTL logic. SN75401, SN75402, SN75403, and SN75404 provide AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) and are identical to SN75461 through SN75464 except that the package allows the output current capability to be increased to 500 mA. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 75401 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and output

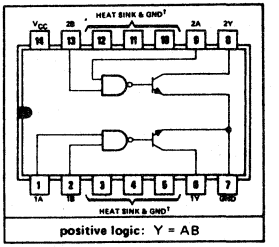


SN75401 — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH AND DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high-level
L = low-level



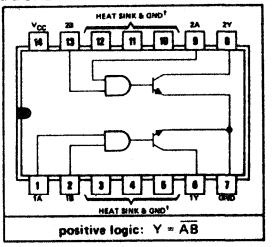
positive logic: $Y = AB$

SN75402 — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NAND DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high-level
L = low-level



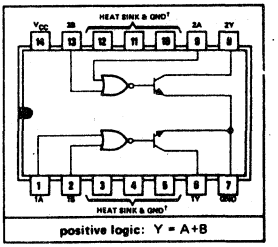
positive logic: $Y = \overline{AB}$

SN75403 — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH OR DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high-level
L = low-level



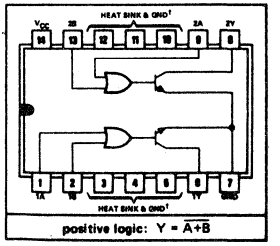
positive logic: $Y = A+B$

SN75404 — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NOR DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high-level
L = low-level



positive logic: $Y = \overline{A+B}$

†Heat-sink pins are internally connected to pin 7.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Off-state output voltage	35 V
Continuous output current (see Note 3)	550 mA
Peak output current ($t_w \leq 10$ ms, duty cycle $\leq 40\%$, see Note 3)	1000 mA
Continuous total power dissipation at (or below) 30°C free-air temperature (see Note 4)	2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

4

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
4. For operation above 30°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

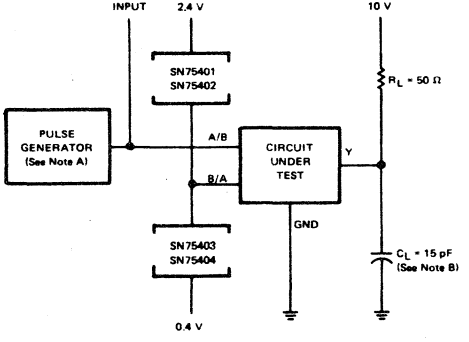
PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 35 V			100	μA
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	
				I_{OL} = 500 mA		0.5	1	
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V,	V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	SN75401	V_{CC} = 5.25 V	V_I = 5 V		8	11	mA
		SN75402		V_I = 0		13	17	
		SN75403		V_I = 5 V		8	11	
		SN75404		V_I = 0		14	19	
I_{CCL}	Supply current, outputs low	SN75401	V_{CC} = 5.25 V	V_I = 0		61	76	mA
		SN75402		V_I = 5 V		65	76	
		SN75403		V_I = 0		63	76	
		SN75404		V_I = 5 V		72	85	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

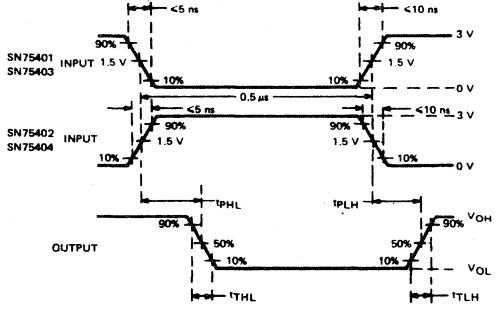
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75401			SN75402			SN75403			SN75404			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\ \Omega$, See Figure 1		30	55		45	65		30	55		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40		30	50		25	40		30	50	ns
t_{TLH}	Transition time, low-to-high-level output			8	20		13	25		8	25		8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20		10	20		10	25		10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx 300$ mA, See Figure 2	V_S-10			V_S-10			V_S-10			V_S-10			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

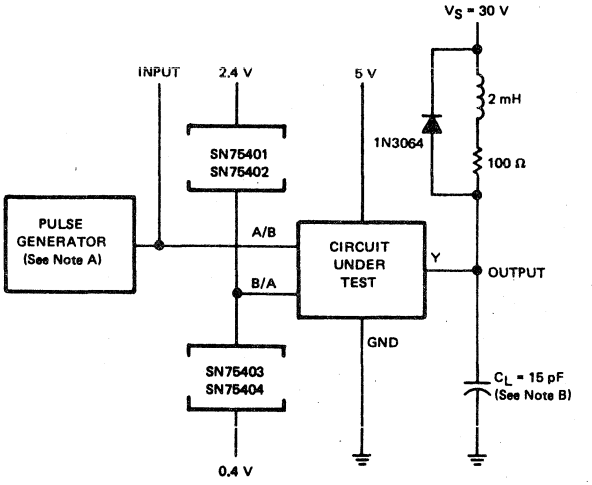


VOLTAGE WAVEFORMS

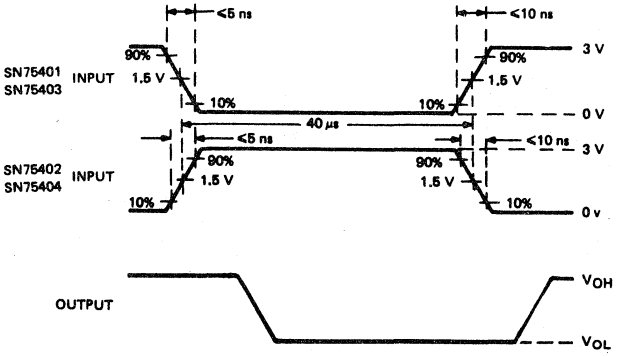
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST

SERIES 75411 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12364, MARCH 1976 – REVISED DECEMBER 1976

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, VERY HIGH-CURRENT DRIVER APPLICATIONS

performance

- 2-W Dissipation Rating
- Characterized for Use to 500 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching

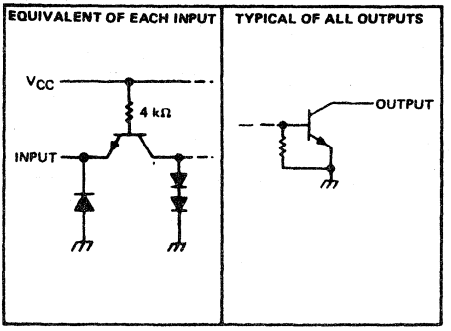
ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltage

description

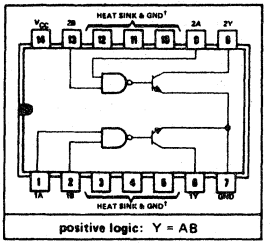
Series 75411 dual peripheral drivers are a family of versatile devices designed for use in systems that employ DTL or TTL logic. SN75411, SN75412, SN75413, and SN75414 provide AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) and are identical to SN75471 through SN75474 except that the package allows the output current capability to be increased to 500 mA. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 75411 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and output



SN75411

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = AB$

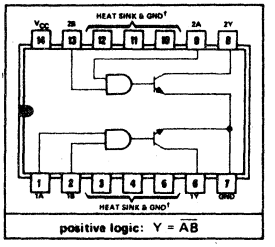
FUNCTION TABLE (EACH AND DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high-level
L = low-level

SN75412

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

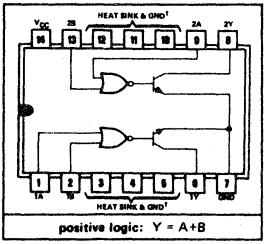
FUNCTION TABLE (EACH NAND DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high-level
L = low-level

SN75413

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A+B$

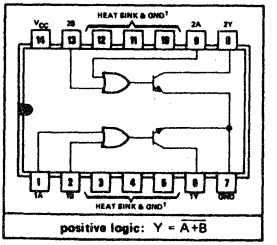
FUNCTION TABLE (EACH OR DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high-level
L = low-level

SN75414

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A+B}$

FUNCTION TABLE (EACH NOR DRIVER)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high-level
L = low-level

†Heat-sink pins are internally connected to pin 7.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Off-state output voltage	70 V
Continuous output current (see Note 3)	550 mA
Peak output current ($t_w \leq 10$ ms, duty cycle $\leq 40\%$, see Note 3)	1000 mA
Continuous total power dissipation at (or below) 30°C free-air temperature (see Note 4)	2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

4

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
4. For operation above 30°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

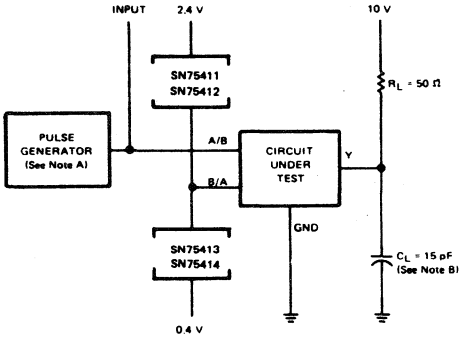
PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	
				I_{OL} = 500 mA		0.5	1	
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V,	V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	SN75411	V_{CC} = 5.25 V	V_I = 5 V		8	11	mA
		SN75412		V_I = 0		13	17	
		SN75413		V_I = 5 V		8	11	
		SN75414		V_I = 0		14	19	
I_{CCL}	Supply current, outputs low	SN75411	V_{CC} = 5.25 V	V_I = 0		61	76	mA
		SN75412		V_I = 5 V		65	76	
		SN75413		V_I = 0		63	76	
		SN75414		V_I = 5 V		72	85	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

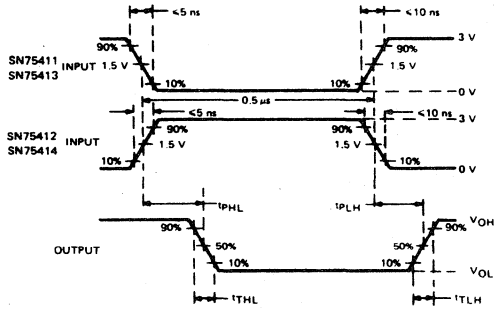
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75411			SN75412			SN75413			SN75414			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\ \Omega$, See Figure 1		30	55		45	65		30	55		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40		30	50		25	40		30	50	ns
t_{TLH}	Transition time, low-to-high-level output			8	20		13	25		8	25		8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20		10	20		10	25		10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S–18			V_S–18			V_S–18			V_S–18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

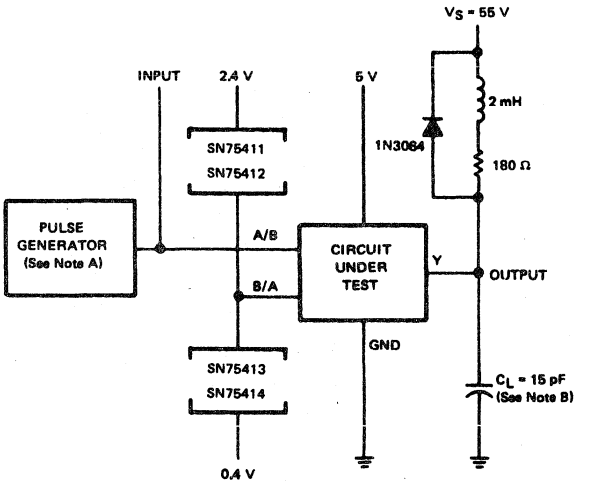


VOLTAGE WAVEFORMS

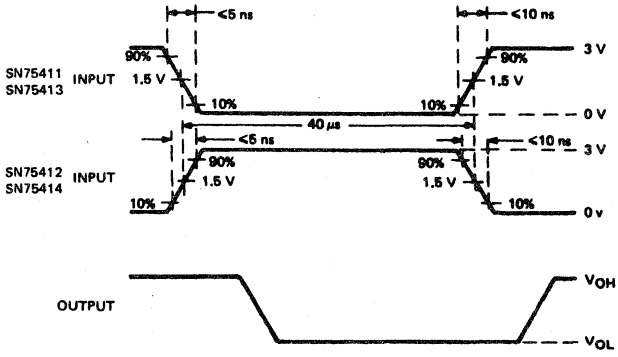
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST

SERIES 75416 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12481, DECEMBER 1976 – REVISED NOVEMBER 1980

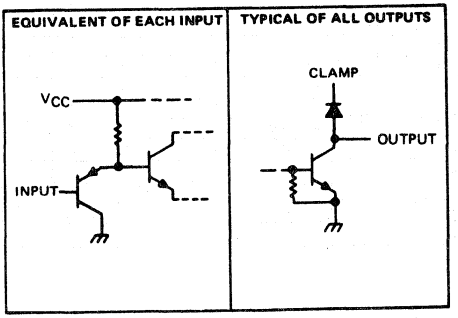
- Characterized for Use to 500 mA
- No Output Latch-Up at 55 V (After Conducting 500 mA)
- High-Voltage Outputs (100 V Typical)
- High-Speed Switching
- Output Clamp Diodes for Transient Suppression (500 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Available in the 14-Pin NE Package
- 2-Watt Power Dissipation Capability

description

Series 75416 dual peripheral drivers are designed for use in systems that require high output voltage, high current, and fast switching times. The SN75416, SN75417, SN75418, and SN75419 provide AND , NAND, OR, and NOR functions respectively. The devices have diode-clamped inputs as well as high-current, high-voltage inductive clamp diodes on the outputs. Each device has a 2-watt power dissipation capability.

Series 75416 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



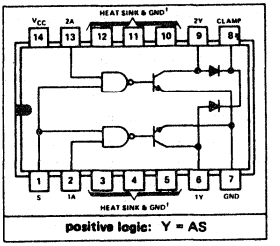
SN75416

FUNCTION TABLE (EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level
L = low level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



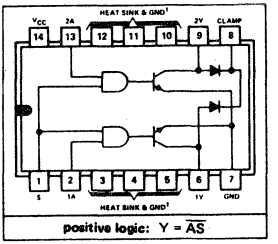
SN75417

FUNCTION TABLE (EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level
L = low level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



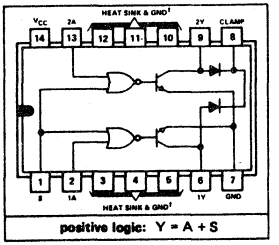
SN75418

FUNCTION TABLE (EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level
L = low level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



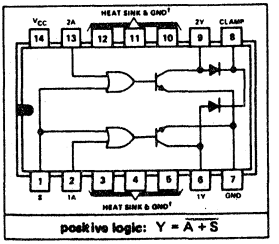
SN75419

FUNCTION TABLE (EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level
L = low level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



†Heat-sink pins are internally connected to pin 7.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 550 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 40\%$ . . . . . 1 A
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 550 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2 W
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

4

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

3. For operation above 25°C free-air temperature, refer to Dissipation Derating curves in the Thermal Information Section, which starts on page 2-1.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

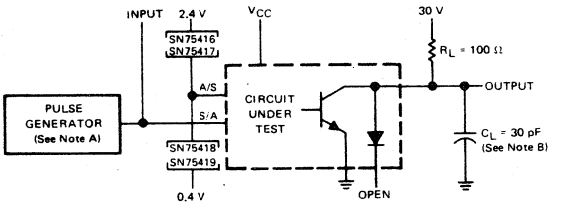
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.95	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V,	$I_{OL} = 100$ mA		0.16	0.3	V
				$I_{OL} = 300$ mA		0.33	0.6	
				$I_{OL} = 500$ mA		0.5	1.1	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.75$ V,	$I_{OH} = 100$ μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.75$ V,	$I_R = 100$ μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.75$ V,	$I_F = 500$ mA	0.8	1.25	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.25$ V,	$V_I = 5.5$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		−80	−110	μA
		Strobe S				−160	−220	
I_{CCH}	Supply current, outputs high	SN75416	$V_{CC} = 5.25$ V	$V_I = 5$ V		20	35	mA
		SN75417		$V_I = 0$		20	35	
		SN75418		$V_I = 5$ V		20	35	
		SN75419		$V_I = 0$		20	35	
I_{CCL}	Supply current, outputs low	SN75416	$V_{CC} = 5.25$ V	$V_I = 0$		75	130	mA
		SN75417		$V_I = 5$ V		75	130	
		SN75418		$V_I = 0$		75	130	
		SN75419		$V_I = 5$ V		75	130	

†All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

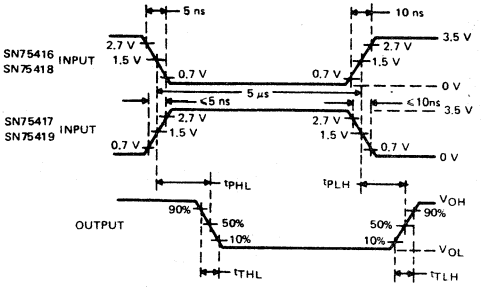
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75416			SN75417			SN75418			SN75419			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 1		100	200		100	200		100	200		100	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	300		200	300		200	300		200	300	ns
t_{TLH}	Transition time, low-to-high-level output			50	100		50	100		50	100		50	100	ns
t_{THL}	Transition time, high-to-low-level output			50	100		50	100		50	100		50	100	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 500 mA, See Figure 2	V_S−11			V_S−11			V_S−11			V_S−11			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

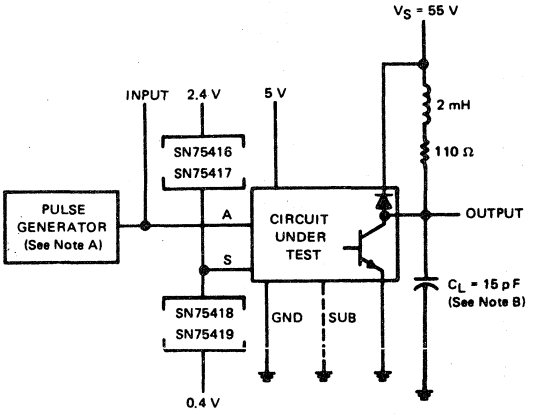


VOLTAGE WAVEFORMS

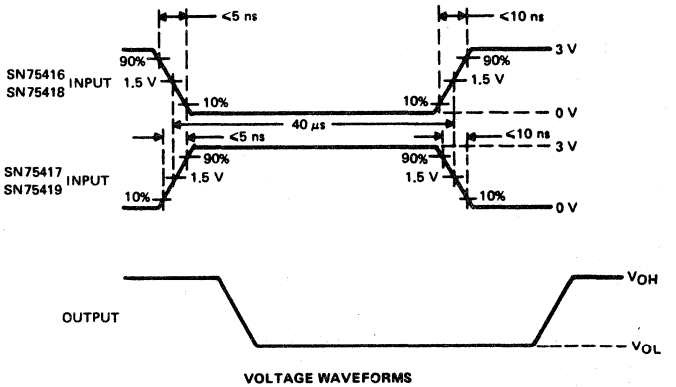
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST

SERIES 75430 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12367, MARCH 1976–REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

performance

- Characterized for Use to 300 mA
- No Output Latch-Up at 15 V (After Conducting 150 mA)
- Very-High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- P-N Junctions Protected by Silicon Nitride
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 75430

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN75430	Positive-AND†	J, N
SN75431	Positive-AND	JG, P
SN75432	Positive-NAND	JG, P
SN75433	Positive-OR	JG, P
SN75434	Positive-NOR	JG, P

†With output transistor base connected externally to output of gate.

4

description

Series 75430 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Diode-clamped inputs simplify circuit design. They are mechanically interchangeable with the popular Series 75450B, Series 75460, and Series 75470 peripheral drivers. Typical applications include very-high-speed logic buffers, line drivers, MOS drivers, memory drivers, and power drivers. Series 75430 drivers are characterized for operation from 0°C to 70°C.

The SN75430 is a unique general-purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. This device offers the system designer the flexibility of tailoring the circuit to the application.

The SN75431, SN75432, SN75433, and SN75434 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN75430	SN75431 SN75432 SN75433 SN75434	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
V_{CC}-to-substrate voltage		15		V
Collector-to-substrate voltage		15		V
Collector-base voltage		15		V
Collector-emitter voltage (see Note 3)		15		V
Emitter-base voltage		5		V
Off-state output voltage			15	V
Continuous collector or output current (see Note 4)		400	400	mA
Peak collector or output current (t_w < 10 ms, duty cycle < 50%, see Note 4)		500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J package	1026		mW
	JG package		825	
	N package	1150		
	P package		1000	
Operating free-air temperature range		0 to 70	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

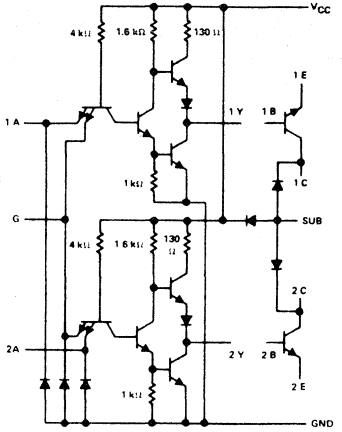
NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J and JG packages, SN75430 through SN75434 chips are glass-mounted.

recommended operating conditions (see Note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

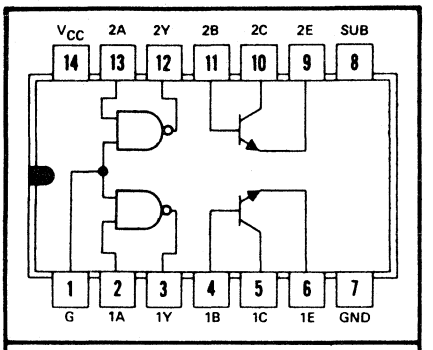
NOTE 6: For the SN75430 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

schematic



Resistor values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G				2	
I_{IH}	High-level input current	input A	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G				80	
I_{IL}	Low-level input current	input A	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G				−3.2	
I_{OS}	Short-circuit output current §		V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		15			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		15			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 7	25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = 0°C		20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 0°C		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	1	C_L = 15 pF, R_L = 400 Ω		9	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				7	13	ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	2	I_C = 100 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω		7	14	ns
t_r	Rise time				10	19	ns
t_s	Storage time				7	15	ns
t_f	Fall time				6	15	ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	I_C ≈ 100 mA, C_L = 15 pF, R_L = 50 Ω		15	26	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	26	ns
t_{TLH}	Transition time, low-to-high-level output				7	12	ns
t_{THL}	Transition time, high-to-low-level output				9	15	ns
V_{OH}	High-level output voltage after switching	4	V_S = 15 V, I_C ≈ 150 mA, R_{BE} = 500 Ω	V_S−10			mV

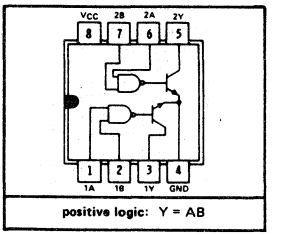
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

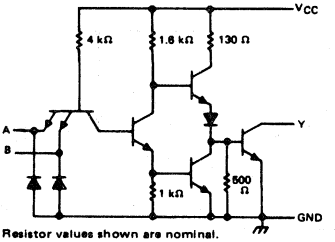
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 15 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		52	65	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	I_O ≈ 100 mA, C_L = 15 pF, R_L = 50 Ω		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				17	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				8	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 15 V, I_O ≈ 150 mA	V_S−10			mV

TYPE SN75432
DUAL PERIPHERAL POSITIVE-NAND DRIVER

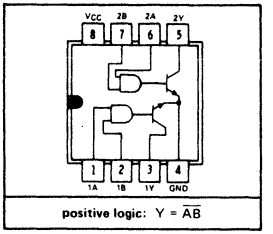
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level

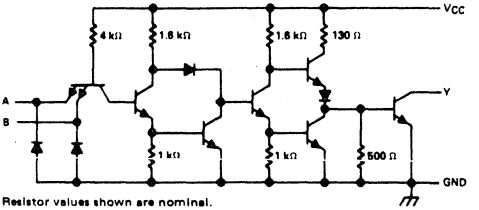
JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 15 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 0		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 5 V		56	71	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	$I_O \approx$ 100 mA, C_L = 15 pF, R_L = 50 Ω		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				19	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				8	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 15 V, $I_O \approx$ 150 mA	V_S−10			mV

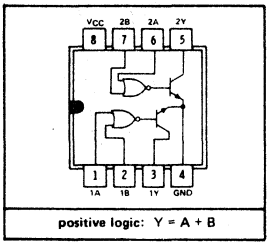
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

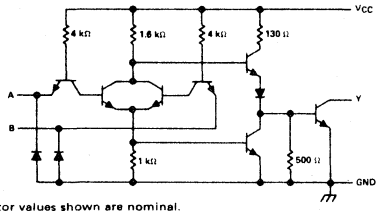
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA			−1.5 V	
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 15 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		54	68	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	$I_O \approx$ 100 mA, C_L = 15 pF, R_L = 50 Ω		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	25	ns
t_{TLH}	Transition time, low-to-high-level output				3	8	ns
t_{THL}	Transition time, high-to-low-level output				9	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 15 V, $I_O \approx$ 150 mA	V_S−10			mV

TYPE SN75434
DUAL PERIPHERAL POSITIVE-NOR DRIVER

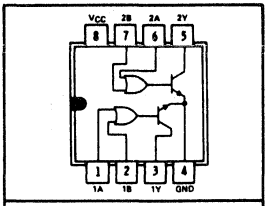
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

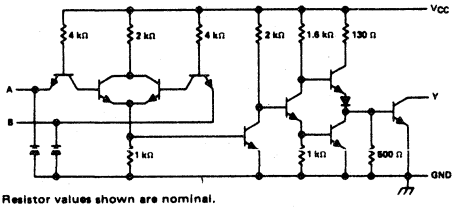
JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

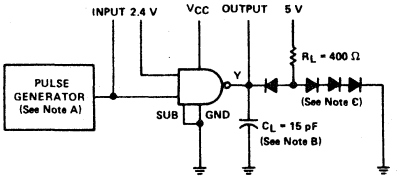
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA			−1.5 V	
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 15 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 0		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 5 V		61	79	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

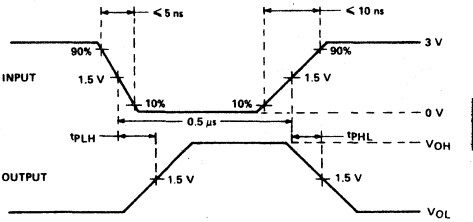
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	$I_O \approx$ 100 mA, C_L = 15 pF, R_L = 50 Ω		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				17	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				8	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 15 V, $I_O \approx$ 150 mA	V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



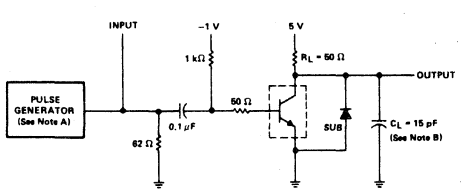
TEST CIRCUIT



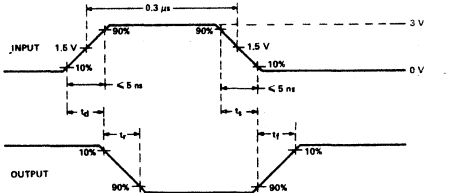
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN75430 ONLY)



TEST CIRCUIT

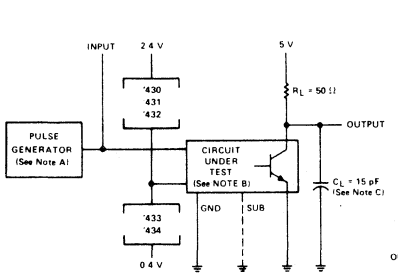


VOLTAGE WAVEFORMS

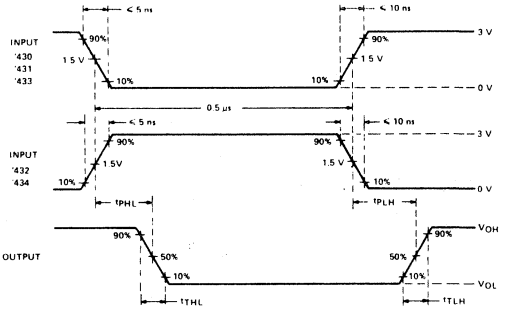
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN75430 ONLY)

PARAMETER MEASUREMENT INFORMATION



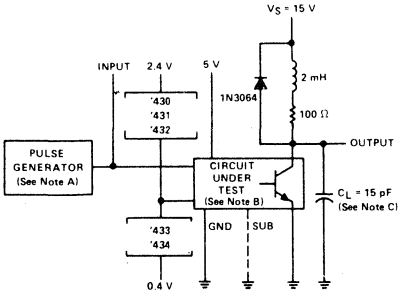
TEST CIRCUIT



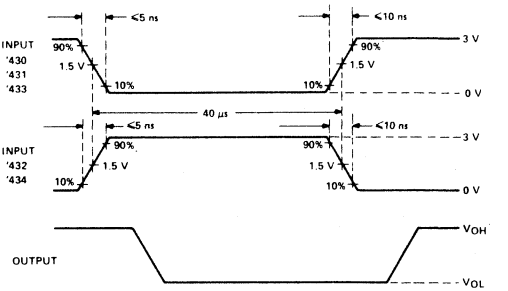
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75430, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
*B. When testing SN75430, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

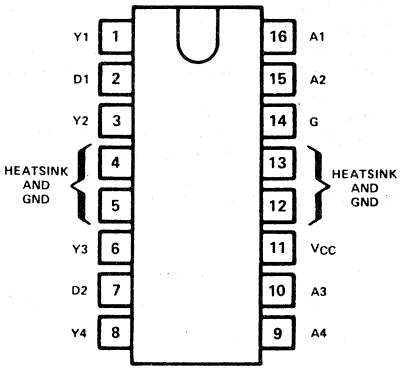
FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

TYPE SN75437
QUADRUPLE PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12795, DECEMBER 1980

- Low Saturation Voltage
- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 500 mA
- No Output Latch-Up at 35 V (After Conducting 500 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (500 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- 2-W Power Package
  - Low $R_{\theta JA}$ . . . 60°C/W
  - Low $R_{\theta JC}$ . . . 10°C/W

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75437 Quad peripheral driver is designed for use in systems that require high current, high voltage, and high power. The SN75437 provides NAND drivers. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs.

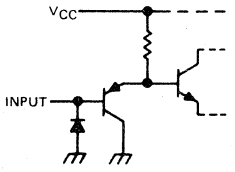
FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

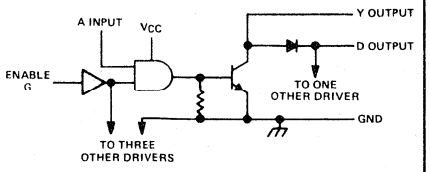
H = high level, L = low level
X = irrelevant

schematic of inputs and functional block diagram

EQUIVALENT OF EACH INPUT



FUNCTIONAL BLOCK DIAGRAM



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 600 mA
Output clamp diode current . . . . . 600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2075 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 250°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. All sections of this quad circuit may conduct rated current simultaneously, however power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

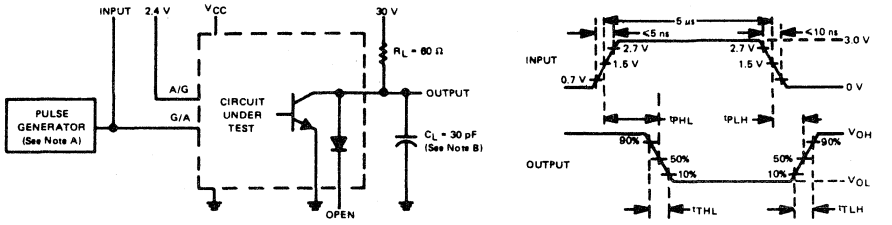
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = 12 mA		0.9	1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 200 mA		0.15	0.5	V
			I_{OL} = 400 mA		0.30	0.6	
			I_{OL} = 500 mA		0.45	0.7	
$V_{(BR)O}$	Output breakdown voltage	V_{CC} = 4.75 V,	I_{OH} = 100 μA	70	100		V
$V_{R(D)}$	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
$V_{F(D)}$	Output clamp diode forward voltage	V_{CC} = 4.75 V,	I_F = 500 mA	0.6	1.2	1.6	V
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		40	65	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		40	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	R_L = 60 Ω,		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output				750		ns
t_{TLH}	Transition time, low-to-high-level output				200		ns
t_{THL}	Transition time, high-to-low-level output				200		ns
V_{OH}	High-level output voltage after switching	V_S = 35 V, See Figure 2	I_O ≈ 500 mA,	V_S−10			mV

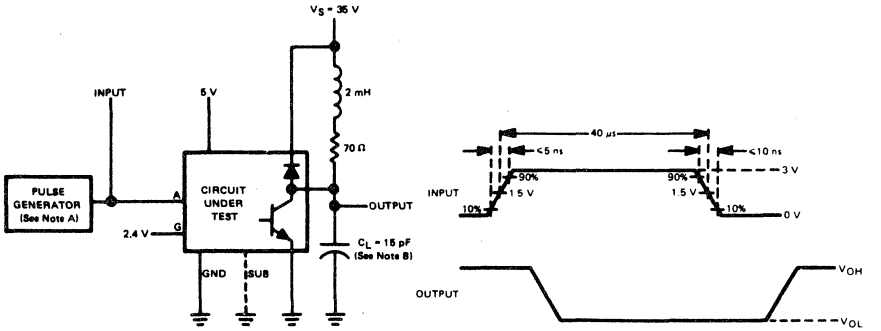
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

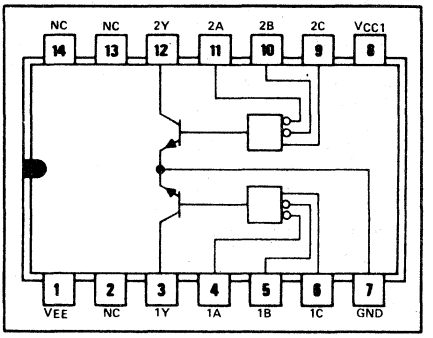
FIGURE 2–LATCH-UP TEST

TYPE SN75441
DUAL ECL-COMPATIBLE PERIPHERAL DRIVER

BULLETIN NO. DL-S 12479, DECEMBER 1976–REVISED AUGUST 1977

- Characterized For Use To 100 mA
- No Output Latch-Up at 20 V (After Conducting 100 mA)
- High-Speed Switching
- Positive OR Logic
- Versatile Interface Circuits for Use Between ECL and High-Current, High-Voltage Systems
- Inputs are Compatible with Series 10000 ECL and Other Similar ECL Families
- Standard Supply Voltages

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC–No internal connection

description

The SN75441 is a monolithic dual ECL-compatible peripheral driver and interface circuit. The device accepts standard input signals from ECL families and provides high-current and high-voltage output levels suitable for driving MOS and TTL circuits. Typical applications include high-speed logic buffers, line drivers, MOS drivers, and memory drivers.

The device has one in-phase and two out-of-phase ECL-compatible inputs per driver. By proper connections of the inputs, the SN75441 may be used three ways: positive-OR gate, differential ECL line receiver, or inverting gate. Some applications require one input per gate to be connected to an externally generated ECL reference voltage, V_{BB}.

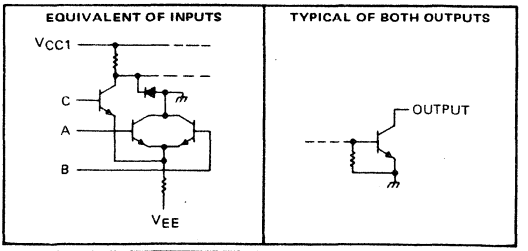
The SN75441 operates from two standard supplies, the TTL V_{CC} supply and the ECL V_{EE} supply, and is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUT
DIFFERENTIAL	LOGIC LEVEL			Y
(More positive of A or B)–C	A	B	C	
H ($V_{ID} \geq 150$ mV)	L	H	L	H
	H	L	L	
	H	H	L	
? (-150 mV $\leq V_{ID} \leq 150$ mV)	X	X	X	INDETERMINATE
L ($V_{ID} \leq -150$ mV)	L	L	H	L

H = high level, L = low level, X = irrelevant
See additional function tables in Figure 3.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{EE}	−7 V to 0.5 V
Negative voltage at V_{CC} with respect to V_{EE}	−0.5 V
Input voltage range	−7 V to 0.5 V
Negative voltage at any input with respect to V_{EE}	−1 V
Differential input voltage	5.5 V
Off-state output voltage	30 V
Output current	150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, the SN75441 chip is glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{EE}	−4.68	−5.2	−5.72	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels (see Note 3)

PARAMETER		B (Least Positive)	A (Most Positive)	UNIT
V_{IH}	High-level input voltage at any input	−1.5	−0.7	V
V_{IL}	Low-level input voltage at any input	V_{EE}	V_{IH}−150 mV	
V_{IDH}	High-level differential input voltage (see Note 3)	150		mV
V_{IDL}	Low-level differential input voltage (see Note 3)		−150	mV

NOTE 3: Differential input voltage is the voltage at the more positive inverting input (A or B) with respect to the noninverting input (C) of the same gate.

electrical characteristics over recommended ranges of V_{CC}, V_{EE}, and operating free-air temperature (unless otherwise noted)

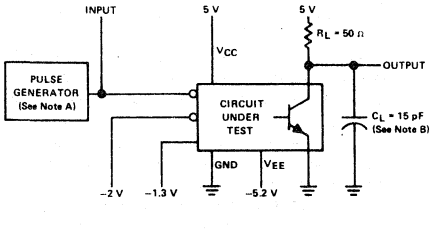
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IDH} = 150 mV, V_{OH} = 30 V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IDL} = −150 mV	I_{OL} = 10 mA		0.15	0.3	V
			I_{OL} = 100 mA		0.35	0.5	
I_{IH}	High-level input current	V_{EE} = −5.72 V, V_I = −0.7 V, All other inputs at −5.72 V			300	800	μA
I_{IL}	Low-level input current	V_{EE} = −5.72 V, All other inputs at −0.7 V	V_I = −2 V			−10	μA
			V_I = −5.72 V			−100	
$I_{CC(H)}$	Supply current from V_{CC}, all outputs high	V_{CC} = 5.25 V, V_{EE} = −5.72 V, All A and B inputs at −0.7 V, Both C inputs at −2 V, No load, T_A = 25°C			15	22	mA
$I_{EE(H)}$	Supply current from V_{EE}, all outpus high				−21	−30	
$I_{CC(L)}$	Supply current from V_{CC}, all outpus low	V_{CC} = 5.25 V, V_{EE} = −5.72 V, All A and B inputs at −2 V, Both C inputs at −0.7 V, No load, T_A = 25°C			40	56	mA
$I_{EE(L)}$	Supply current from V_{EE}, all outputs low				−21	−30	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, and T_A = 25°C.

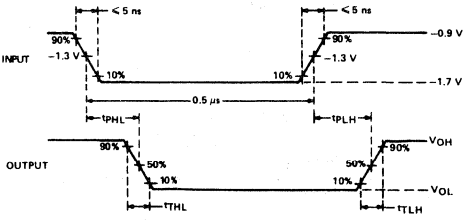
switching characteristics, V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF, R_L = 50 Ω, I_O ≈ 100 mA, See Figure 1		7	12	ns
t_{THL}	Transition time, high-to-low-level output			11	16	ns
t_{PLH}	Propagation delay time, low-to-high-level output			19	25	ns
t_{PHL}	Propagation delay time high-to-low-level output			22	30	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, I_O ≈ 100 mA, See Figure 2	V_S−20			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

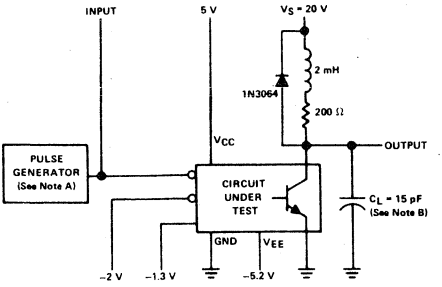


VOLTAGE WAVEFORMS

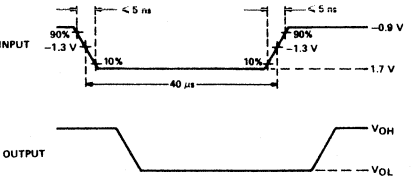
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1 – SWITCHING TIMES, EACH DRIVER

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



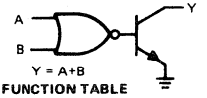
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST, EACH DRIVER

TYPICAL APPLICATION DATA

positive-OR gate

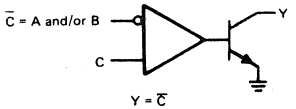


Y = A+B

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
C at V_{BB}	L	L	V_{BB}	L
	H	X	V_{BB}	H
	X	H	V_{BB}	H

differential ECL line receiver



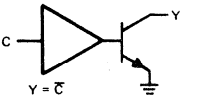
$Y = \overline{C}$

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B connected together	H	H	L	H
	L	L	H	L
A not used but connected low	L	H	L	H
	L	L	H	L
B not used but connected low	H	L	L	H
	L	L	H	L

H = high level, L = low level, X = irrelevant
V_{BB} = Reference Supply voltage for SN10000 Series ECL.

inverting gate



$Y = \overline{C}$

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	H
	V_{BB}	V_{BB}	H	L
A at V_{BB}, B connected low	V_{BB}	L	L	H
	V_{BB}	L	H	L
B at V_{BB}, A connected low	L	V_{BB}	L	H
	L	V_{BB}	H	L

The one in-phase (C) and two out-of-phase (A and B) inputs per driver permit much flexibility when using the SN75441. By connecting the correct input to an externally generated V_{BB} (ECL reference supply voltage), positive-OR gate or inverting gate functions may be obtained. The V_{BB} reference voltage may be generated by connecting the output of any ECL gate to its out-of-phase input, by using the V_{BB} pin of certain ECL devices such as SN10115, or by other methods. By driving the correct inputs differentially, these devices may be used as differential ECL line receivers and no V_{BB} reference voltage is required. An unused out-of-phase input may be connected low or connected to the other out-of-phase input of the same gate in many applications.

FIGURE 3–FUNCTIONS

SERIES 75446
DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12630, DECEMBER 1978 – REVISED NOVEMBER 1980

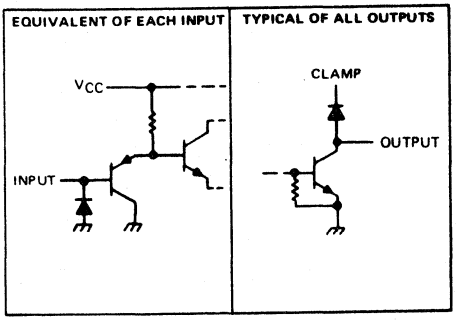
- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

description

Series 75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series 75446 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

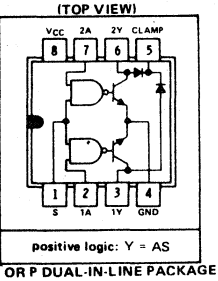


SN75446
FUNCTION TABLE
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

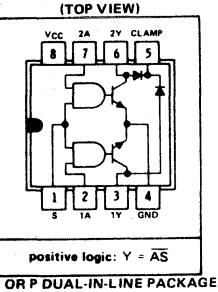


SN75447
FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

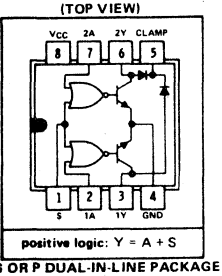


SN75448
FUNCTION TABLE
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

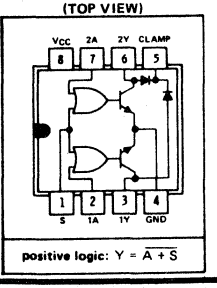


SN75449
FUNCTION TABLE
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 400 mA
Output clamp diode current . . . . . 400 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

4

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 11. In the JG package, SN75446 through SN75449 chips are glass-mounted.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

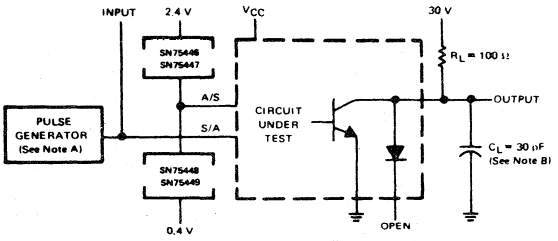
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −12 mA			−0.9	−1.5	V
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	μA
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA		0.10	0.3	V
				I_{OL} = 200 mA		0.22	0.45	
				I_{OL} = 300 mA		0.45	0.65	
				I_{OL} = 350 mA		0.55	0.75	
$V_{(BR)O}$	Output breakdown voltage		V_{CC} = 4.75 V,	I_{OH} = 100 μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		V_{CC} = 4.75 V,	I_F = 350 mA	0.6	1.2	1.6	V
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	μA
I_{IL}	Low-level input current	A input	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	μA
		Strobe S				−1	−20	
I_{CCH}	Supply current, outputs high	SN75446	V_{CC} = 5.25 V,	V_I = 5 V		11	18	mA
		SN75447		V_I = 0		11	18	
		SN75448		V_I = 5 V		18	25	
		SN75449		V_I = 0		18	25	
I_{CCL}	Supply current, outputs low	SN75446	V_{CC} = 5.25 V	V_I = 0		11	18	mA
		SN75447		V_I = 5 V		11	18	
		SN75448		V_I = 0		18	25	
		SN75449		V_I = 5 V		18	25	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

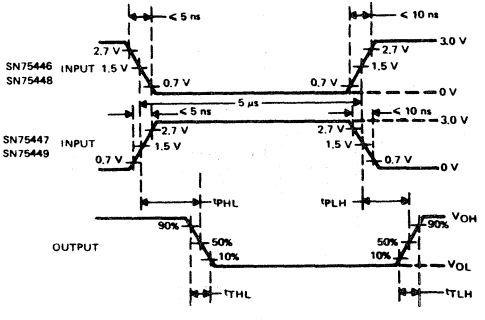
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN75446			SN75447			SN75448			SN75449			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 1		300	750		300	750		300	750		300	750	ns
t_{PHL} Propagation delay time, high-to-low-level output			200	500		200	500		200	500		200	500	ns
t_{TLH} Transition time, low-to-high-level output			50	100		50	100		50	100		50	100	ns
t_{THL} Transition time, high-to-low-level output			50	100		50	100		50	100		50	100	ns
V_{OH} High-level output voltage after switching	V_S = 55 V, I_O = 300 mA, See Figure 2	V_S–18			V_S–18			V_S–18			V_S–18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



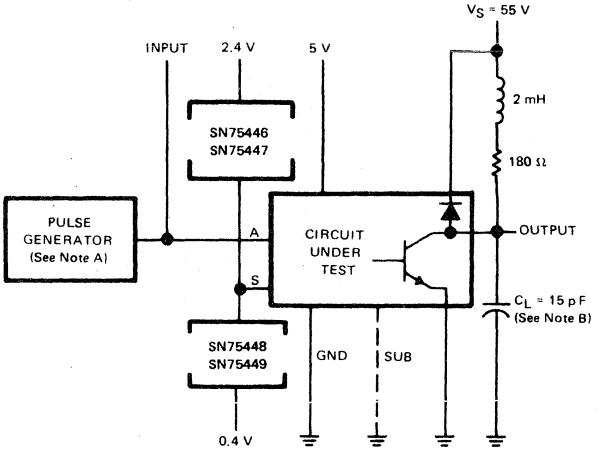
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

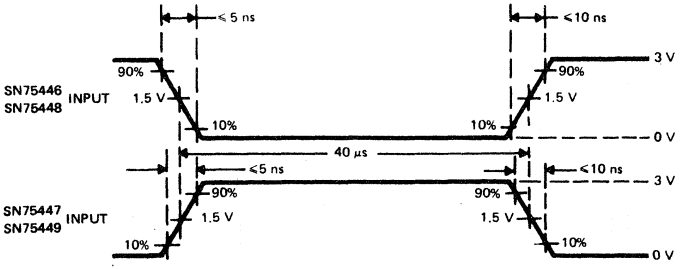
FIGURE 1–SWITCHING CHARACTERISTICS

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST

SERIES 55450B/75450B DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12424, DECEMBER 1976 – REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55450/75450

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55450B	AND†	J
SN55451B	AND	JG
SN55452B	NAND	JG
SN55453B	OR	JG
SN55454B	NOR	JG
SN75450B	AND†	J, N
SN75451B	AND	JG, P
SN75452B	NAND	JG, P
SN75453B	OR	JG, P
SN75454B	NOR	JG, P

†With output transistor base connected externally to output of gate.

description

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The SN55450B and SN75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55450B	SN55451B SN55452B SN55453B SN55454B	SN75450B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		35		35		V
Collector-to-substrate voltage		35		35		V
Collector-base voltage		35		35		V
Collector-emitter voltage (see Note 3)		30		30		V
Emitter-base voltage		5		5		V
Off-state output voltage			30		30	V
Continuous collector or output current (see Note 4)		400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J package	1375		1025		mW
	JG package		1050		825	
	N package			1150		
	P package				1000	
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

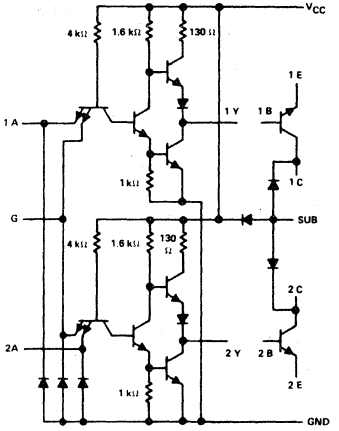
NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J and JG packages, SN55450B through SN55454B chips are alloy-mounted; SN75450B through SN75454B chips are glass-mounted.

recommended operating conditions (see Note 6)

	SERIES 55450B			SERIES 75450B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

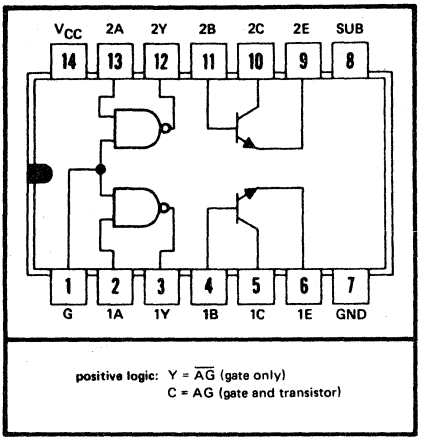
NOTE 6: For the SN55450B and SN75450B only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

schematic



Resistor values shown are nominal.

SN55450B . . . J
SN75450B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS†	SN55450B			SN75450B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		input G				2			2	
I_{IH}	High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		input G				80			80	
I_{IL}	Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		input G				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, V_I = 0		28	4		28	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55450B MIN	SN55450B TYP‡	SN55450B MAX	SN75450B MIN	SN75450B TYP‡	SN75450B MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 7	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 7: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15	ns

output transistors

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		8	15	ns
t_r	Rise time			12	20	ns
t_s	Storage time			7	15	ns
t_f	Fall time			6	15	ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	30	ns
t_{TLH}	Transition time, low-to-high-level output			7	12	ns
t_{THL}	Transition time, high-to-low-level output			9	15	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−6.5			mV

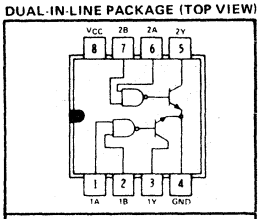
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

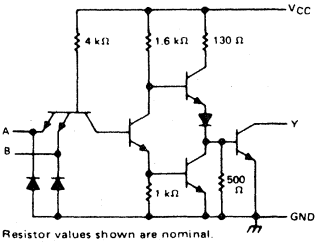
H = high level, L = low level

SN55451B . . . JG
SN75451B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55451B			SN75451B			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	25	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 4	V_S−6.5			mV

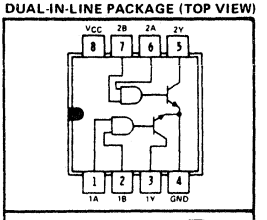
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

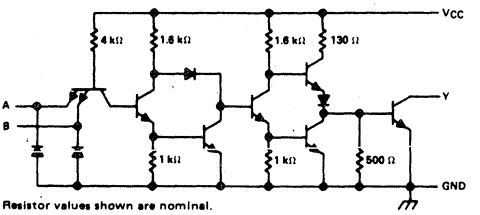
H = high level, L = low level

SN55452B . . . JG
SN75452B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55452B			SN75452B			UNIT
				MIN	TYP†	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IL} = 0.8 V,			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = 2 V,		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = 2 V,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0 V		11	14		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5V		56	71		56	71	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			24	35	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 4	V_S−6.5			mV

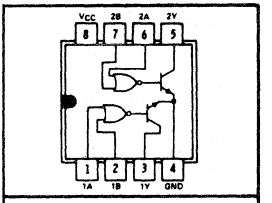
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

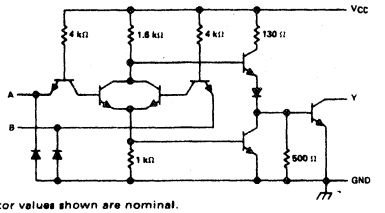
H = high level, L = low level

SN55453B . . . JG
SN75453B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55453B			SN75453B			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		54	68		54	68	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			16	25	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, I_O ≈ 300 mA, See Figure 4	V_S−6.5			mV

TYPES SN55454B, SN75454B
DUAL PERIPHERAL POSITIVE-NOR DRIVERS

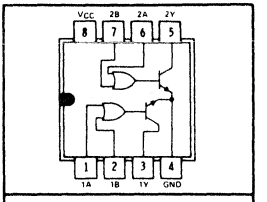
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

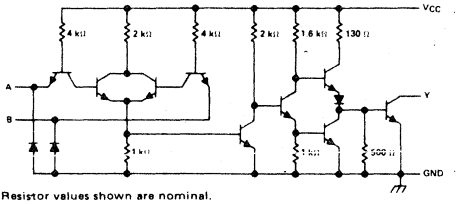
SN55454B . . . JG
SN75454B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

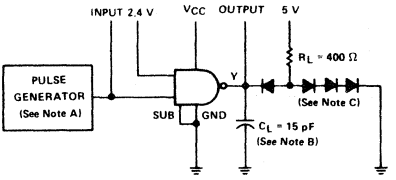
PARAMETER		TEST CONDITIONS†	SN55454B			SN75454B			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	79		61	79	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

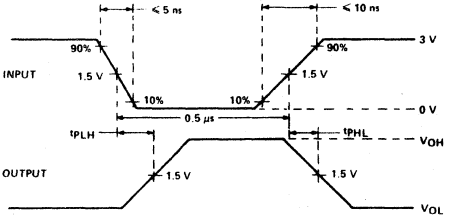
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			24	35	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 4	V_S−6.5			mV

PARAMETER MEASUREMENT INFORMATION



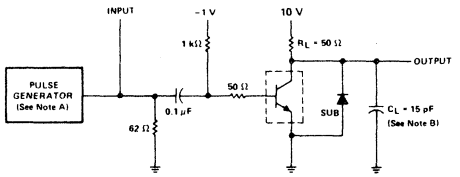
TEST CIRCUIT



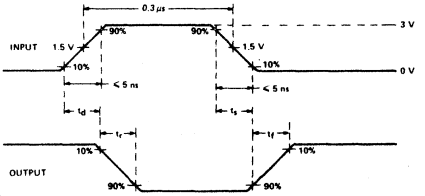
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55450B and SN75450B ONLY)



TEST CIRCUIT

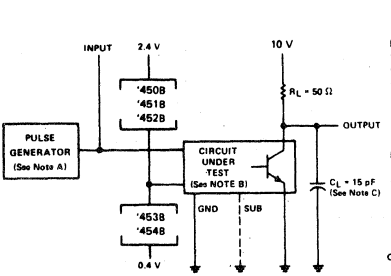


VOLTAGE WAVEFORMS

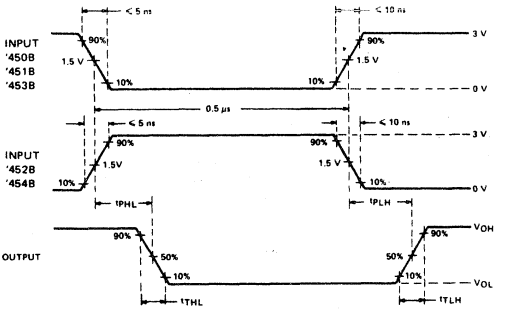
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55450B AND SN75450B ONLY)

PARAMETER MEASUREMENT INFORMATION



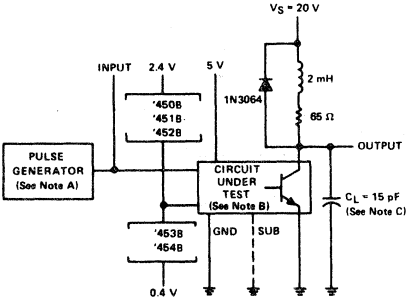
TEST CIRCUIT



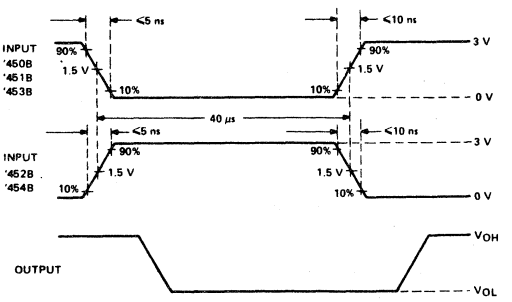
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55450B or SN75450B, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing SN55450B or SN75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

SN554508, SN754508
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

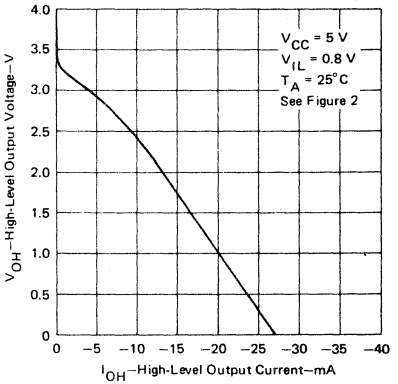


FIGURE 5

SN554508, SN754508
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

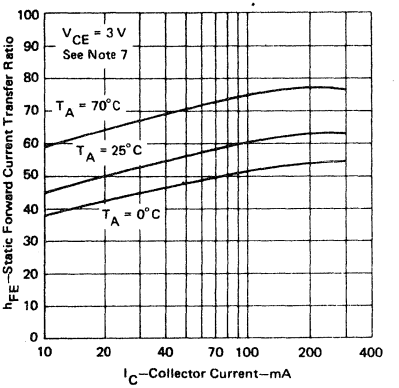


FIGURE 6

SN554508, SN754508
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

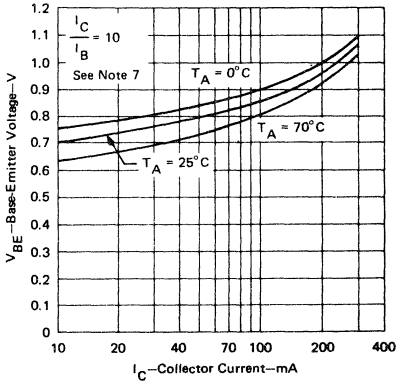


FIGURE 7

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

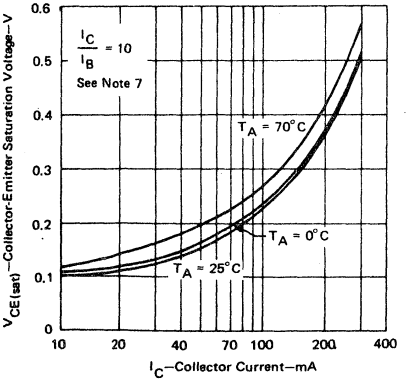


FIGURE 8

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12425, DECEMBER 1976—REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55460/75460

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55460	AND†	J
SN55461	AND	JG
SN55462	NAND	JG
SN55463	OR	JG
SN55464	NOR	JG
SN75460	AND†	J, N
SN75461	AND	JG, P
SN75462	NAND	JG, P
SN75463	OR	JG, P
SN75464	NOR	JG, P

†With output transistor base connected externally to output of gate

description

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75460 drivers are characterized for operation from 0°C to 70°C.

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55460	SN55461 SN55462 SN55463 SN55464	SN75460	SN75461 SN75462 SN75463 SN75464	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		40		40		V
Collector-to-substrate voltage		40		40		V
Collector-base voltage		40		40		V
Collector-emitter voltage (see Note 3)		40		40		V
Collector-emitter voltage (see Note 4)		25		25		V
Emitter-base voltage		5		5		V
Off-state output voltage			35		35	V
Continuous collector or output current (see Note 5)		400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5)		500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375		1025		mW
	JG package		1050		825	
	N package			1150		
	P package				1000	
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

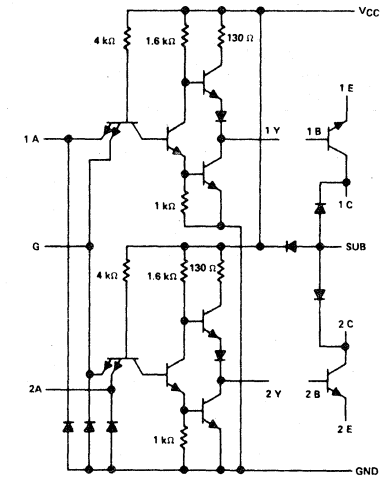
NOTES 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J and JG packages, SN55460 through SN55464 chips are alloy-mounted; SN75460 through SN75464 chips are glass-mounted.

recommended operating conditions (see Note 7)

	SERIES 55460			SERIES 75460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

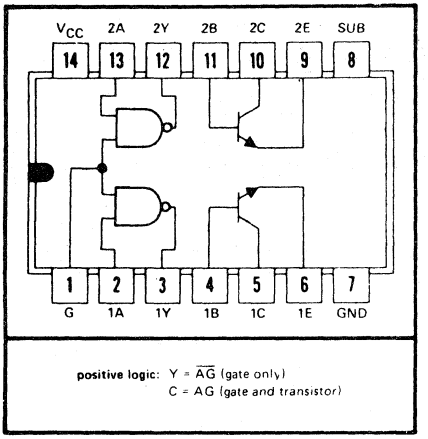
NOTE 7: For SN55460 and SN75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

schematic



Resistor values shown are nominal.

SN55460 . . . J
SN75460 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS†	SN55460 MIN	SN55460 TYP‡	SN55460 MAX	SN75460 MIN	SN75460 TYP‡	SN75460 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		input G				2			2	
I_{IH}	High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		input G				80			80	
I_{IL}	Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		input G				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, V_I = 0		2.8	4		2.8	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55460 MIN	SN55460 TYP†	SN55460 MAX	SN75460 MIN	SN75460 TYP‡	SN75460 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			40			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0, See Note 8		25			25			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			40			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25 C	See Note 8	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25 C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25 C.
NOTE 8: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output			8		ns

output transistors

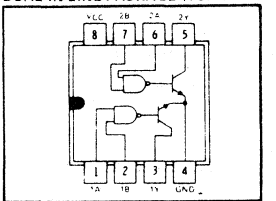
PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		10		ns
t_r	Rise time			16		ns
t_s	Storage time			23		ns
t_f	Fall time			14		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−10			mV

SN55461 . . . JG
SN75461 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = AB$

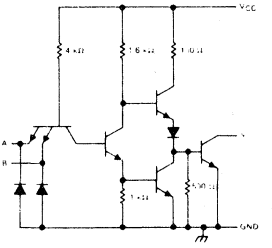
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

schematic (each driver)



Resistor values shown are nominal

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

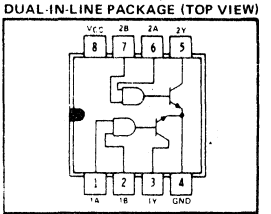
PARAMETER		TEST CONDITIONS†	SN55461 MIN	SN55461 TYP‡	SN55461 MAX	SN75461 MIN	SN75461 TYP‡	SN75461 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_O ≈ 300 mA, See Figure 4	V_S−10			mV

SN55462 . . . JG
SN75462 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

logic

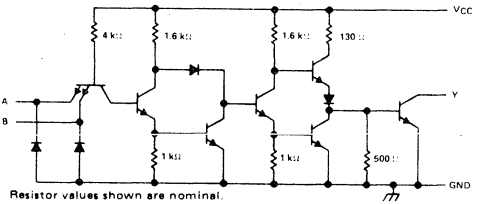
FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN55462			SN75462			UNIT
			MIN	TYP†	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5V		61	76		61	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_O ≈ 300 mA, See Figure 4	V_S−10			mV

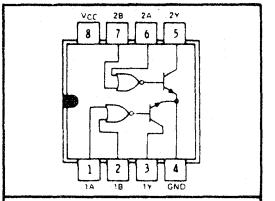
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

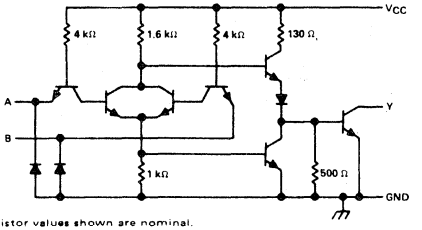
H = high level, L = low level

SN55463 . . . JG
SN75463 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A + B$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	25	ns
t_{THL}	Transition time, high-to-low-level output			10	25	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 4	V_S−10			mV

TYPES SN55464, SN75464
DUAL PERIPHERAL POSITIVE-NOR DRIVERS

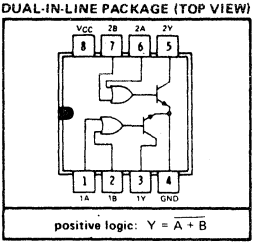
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

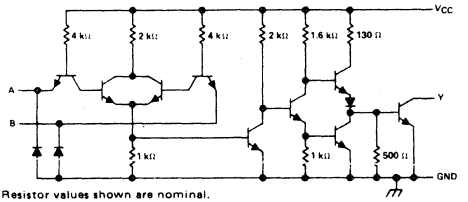
SN55464 . . . JG
SN75464 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

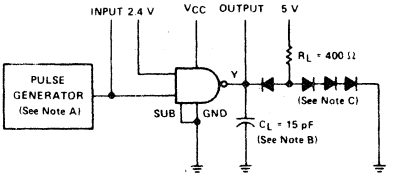
PARAMETER		TEST CONDITIONS†	SN55464			SN75464			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 25 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		14	19		14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		67	85		67	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

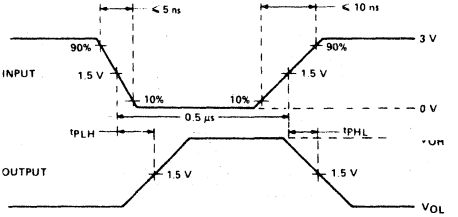
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 4	V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



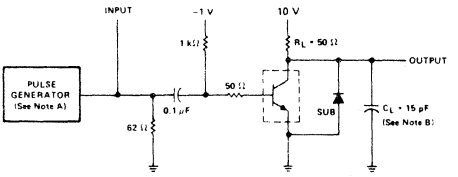
TEST CIRCUIT



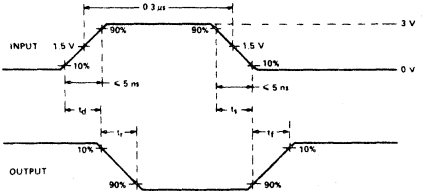
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance
C. All diodes a:e 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55460 AND SN75460 ONLY)



TEST CIRCUIT

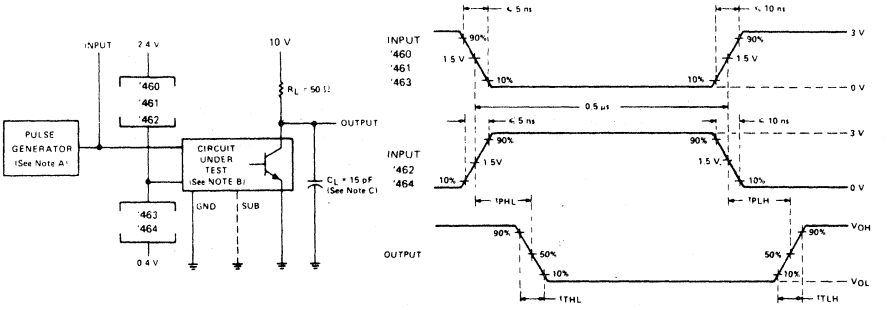


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle < 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55460 AND SN75460 ONLY)

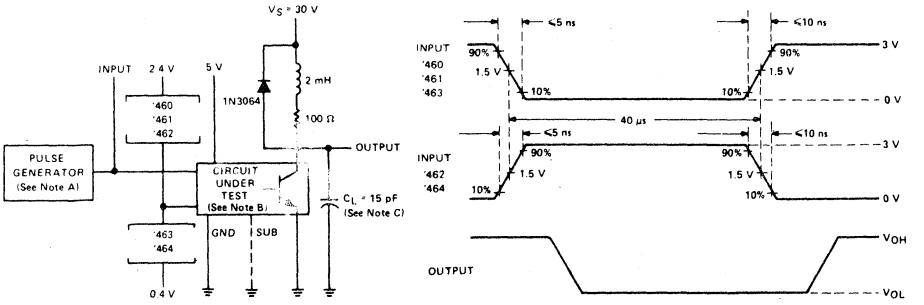
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} ≈ 50 Ω
B. When testing SN55460 or SN75460, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing SN55460 or SN75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

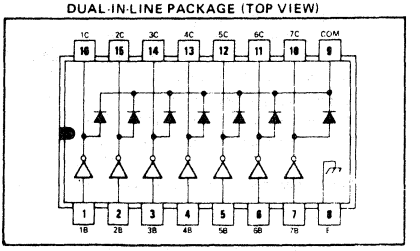
SERIES 75465 DARLINGTON TRANSISTOR ARRAYS

BULLETIN NO. DL-S 12459, DECEMBER 1976 - REVISED DECEMBER 1980

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2005A, ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

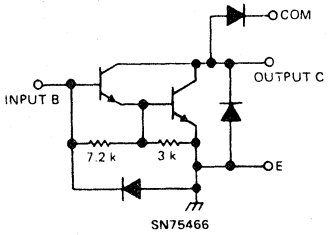


description

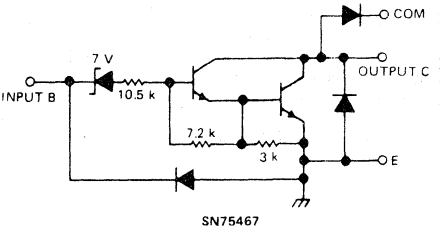
Series 75465 devices are monolithic high-voltage, high-current darlington transistor arrays. Each comprises seven n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75465 has a 1.05-kΩ series base resistor and is especially designed for use with TTL where higher output current is required and loading of the driving source is not a concern. The SN75466 is a general-purpose array and may be used with DTL, TTL, P-MOS, CMOS, etc. The SN75467 is specifically designed for use with 14- to 25-volt P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a 2.7-kΩ series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The SN75469 has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the SN75468 while the required voltage is less than that required by the SN75467.

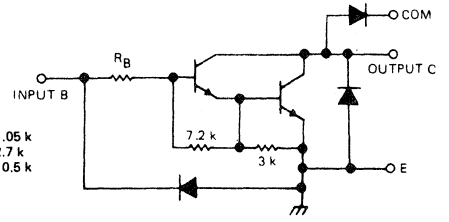
schematics (each darlington pair)



SN75466



SN75467



SN75465: R_B = 1.05 k
SN75468: R_B = 2.7 k
SN75469: R_B = 10.5 k

SN75465, SN75468, SN75469

All resistor values shown are nominal and in ohms.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage . . . . . 100 V
Input voltage (see Note 1): SN75465 . . . . . 15 V
SN75467, SN75468, SN75469 . . . . . 30 V
Peak collector current (see Figures 14 and 15) . . . . . 500 mA
Output clamp diode current . . . . . 500 mA
Continuous input current, SN75466 only . . . . . 25 mA
Total substrate-terminal current: J package . . . . . −500 mA
N package . . . . . −2.5 A
Continuous dissipation (total package) at (or below) 25°C free-air temperature (see Note 2):
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds, N package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75465 through SN75469 chips are glass-mounted.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			SN75465 MIN	SN75465 TYP	SN75465 MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0				50	μA
			V_{CE} = 100 V,	I_I = 0,	T_A = 70°C			100	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 100 V,	I_C = 500 μA,	T_A = 70°C	50	65		μA
I_I	Input current	4	V_I = 3 V				1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 350 mA				2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 μA,	I_C = 100 mA			0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA			1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA			1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V					50	μA
			V_R = 100 V,	T_A = 70°C				100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA				1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz			15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75466 MIN	SN75466 TYP	SN75466 MAX	SN75467 MIN	SN75467 TYP	SN75467 MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	μA
			V_{CE} = 100 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 17 V						0.85	1.3	mA
h_{FE}	Static forward current transfer ratio	6	V_{CE} = 2 V,	I_C = 350 mA	1000						
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V,				50			50	μA
			V_R = 100 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75468 MIN	SN75468 TYP	SN75468 MAX	SN75469 MIN	SN75469 TYP	SN75469 MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	μA
			V_{CE} = 100 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1.0	1.45	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	
			I_I = 350 μA,	I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V				50			50	μA
			V_R = 100 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 305 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		15	25		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V,	R_L = 163 Ω,		130		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 9		20		ns
V_{OH}	High-level output voltage after switching	V_S = 60 V, See Figure 10	I_O = 300 mA,	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

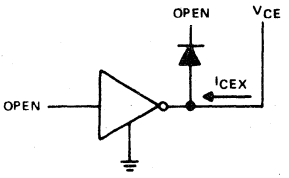


FIGURE 1–I_{CEX}

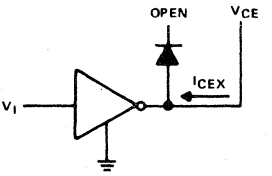


FIGURE 2–I_{CEX}

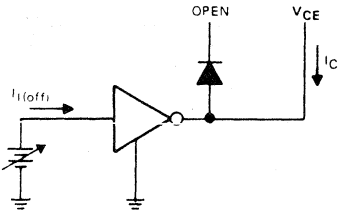


FIGURE 3–$I_{I(off)}$

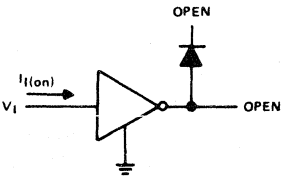


FIGURE 4–I_I

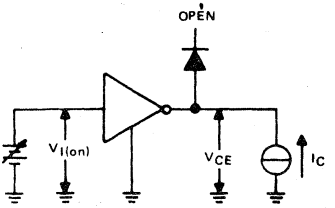
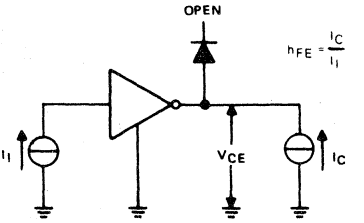


FIGURE 5–$V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 6–h_{FE}, $V_{CE(sat)}$

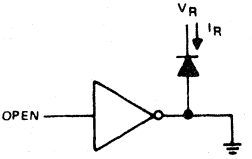


FIGURE 7–I_R

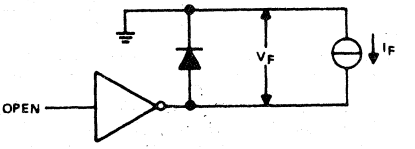
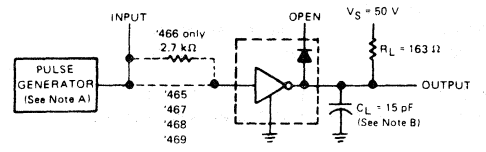
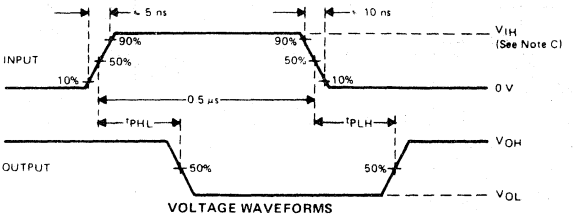


FIGURE 8–V_F

PARAMETER MEASUREMENT INFORMATION



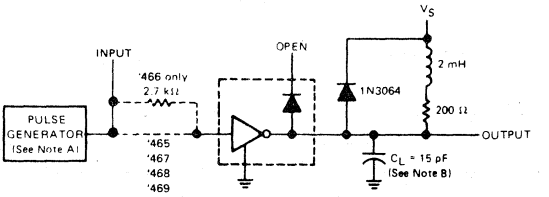
TEST CIRCUIT



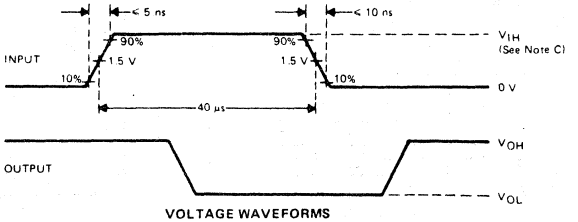
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 9–PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 10–LATCH-UP TEST

4

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

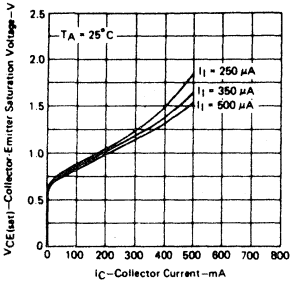


FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

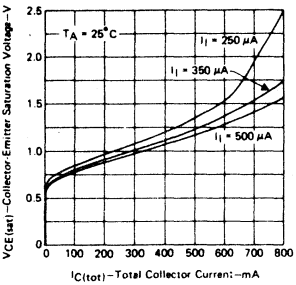


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

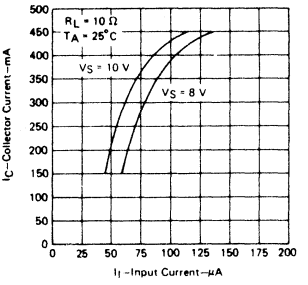


FIGURE 13

THERMAL INFORMATION

J PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

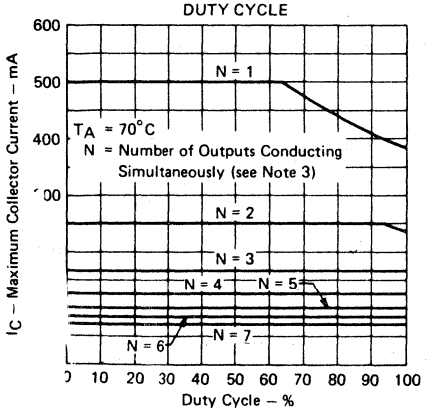


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

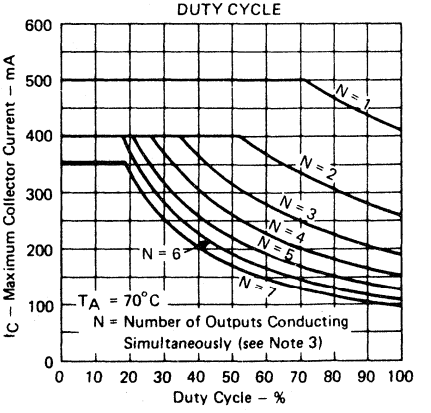
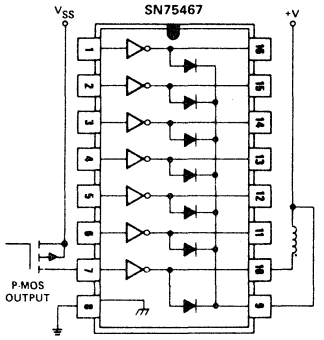


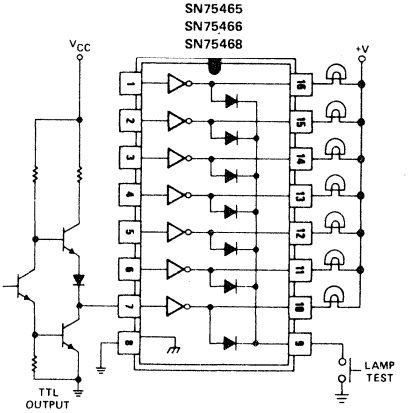
FIGURE 15

NOTE 3: For the J package, N x I_C must not exceed 500 mA (maximum substrate current). For the N package N x I_C must not exceed 2.5 A.

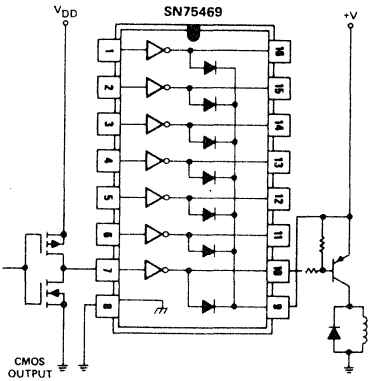
TYPICAL APPLICATION DATA



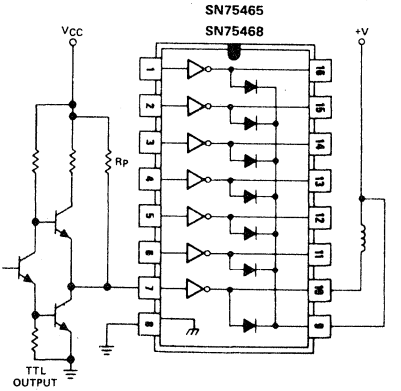
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS



USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

SERIES 55470/75470 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12369, MARCH 1976 – REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55470/75470

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55470	AND†	J
SN55471	AND	JG
SN55472	NAND	JG
SN55473	OR	JG
SN55474	NOR	JG
SN75470	AND†	J, N
SN75471	AND	JG, P
SN75472	NAND	JG, P
SN75473	OR	JG, P
SN75474	NOR	JG, P

†With output transistor base connected externally to output of gate.

description

Series 55470/75470 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 55450B/75450B (limits are the same as Series 55460/75460). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55470 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75470 drivers are characterized for operation from 0°C to 70°C.

The SN55470 and SN75470 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55471/SN75471, SN55472/SN75472, SN55473/SN75473, and SN55474/SN75474 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55470	SN55471 SN55472 SN55473 SN55474	SN75470	SN75471 SN75472 SN75473 SN75474	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		40		40		V
Collector-to-substrate voltage		70		70		V
Collector-base voltage		70		70		V
Collector-emitter voltage (see Note 3)		70		70		V
Collector-emitter voltage (see Note 4)		40		40		V
Emitter-base voltage		5		5		V
Off-state output voltage			70		70	V
Continuous collector or output current (see Note 5)		400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5)		500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375		1025		mW
	JG package		1050		825	
	N package			1150		
	P package				1000	
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	300	C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	C

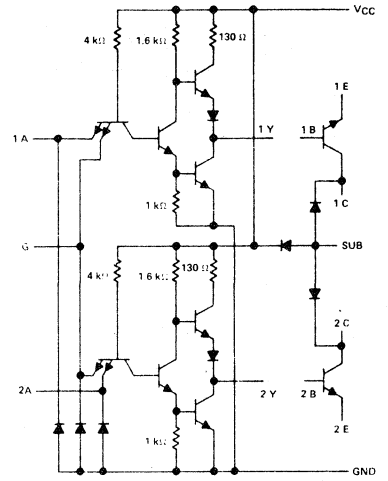
NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J and JG packages, SN55470 through SN55474 chips are alloy-mounted; SN75470 through SN75474 chips are glass-mounted.

recommended operating conditions (see Note 7)

	SERIES 55470			SERIES 75470			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

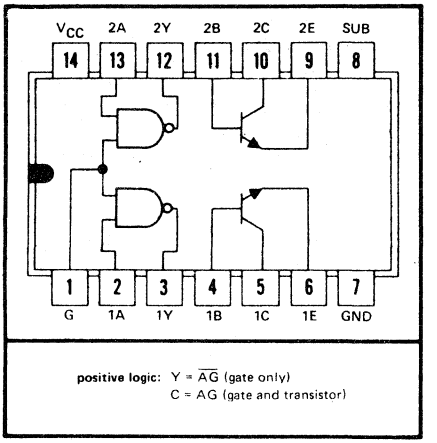
NOTE 7: For SN55470 and SN75470 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

schematic



Resistor values shown are nominal.

SN55470 . . . J
SN75470 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS†	SN55470 MIN	SN55470 TYP‡	SN55470 MAX	SN75470 MIN	SN75470 TYP‡	SN75470 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		input G				2			2	
I_{IH}	High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		input G				80			80	
I_{IL}	Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		input G				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, V_I = 0		28	4		28	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55470 MIN	SN55470 TYP‡	SN55470 MAX	SN75470 MIN	SN75470 TYP†	SN75470 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		70			70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0, See Note 8		40			40			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		70			70			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 8	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 8: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output			8		ns

output transistors

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		10		ns
t_r	Rise time			16		ns
t_s	Storage time			23		ns
t_f	Fall time			14		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−18			mV

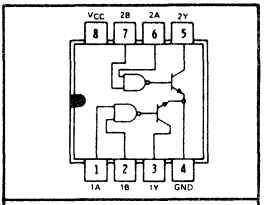
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

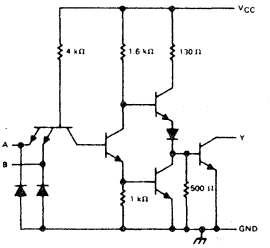
H = high level, L = low level

SN55471 . . . JG
SN75471 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55471			SN75471			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 70 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 4	V_S−18			mV

TYPES SN55472, SN75472
DUAL PERIPHERAL POSITIVE-NAND DRIVERS

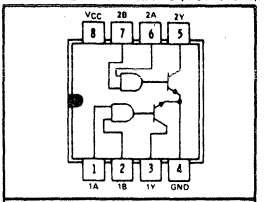
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level

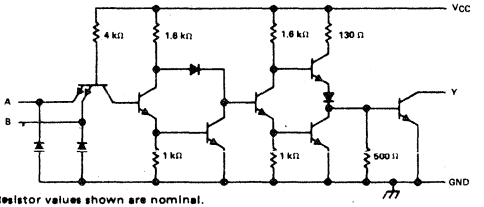
SN55472 . . . JG
SN75472 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN55472			SN75472			UNIT
			MIN	TYP†	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 70 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5V		61	76		61	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 4	V_S−18			mV

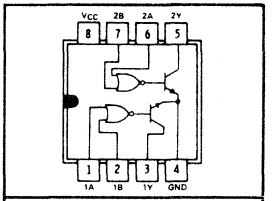
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

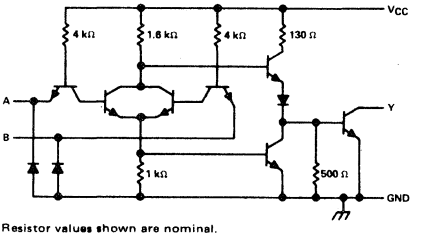
H = high level, L = low level

SN55473 . . . JG
SN75473 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55473			SN75473			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 70 V				300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA			0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA			0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 0		58	76		58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	25	ns
t_{THL}	Transition time, high-to-low-level output			10	25	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 4	V_S−18			mV

TYPES SN55474, SN75474
DUAL PERIPHERAL POSITIVE-NOR DRIVERS

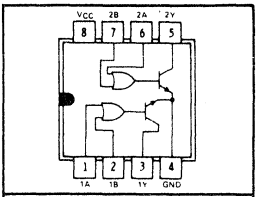
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

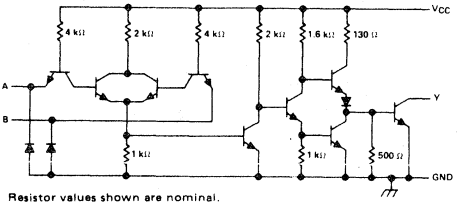
SN55474 . . . JG
SN75474 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

4

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

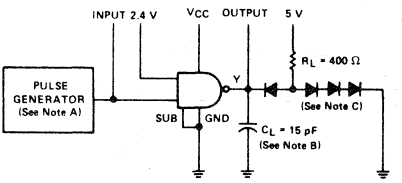
PARAMETER		TEST CONDITIONS†		SN55474			SN75474			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 70 V	V_{IL} = 0.8 V,			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = 2 V,		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = 2 V,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0 V		14	19		14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V		67	85		67	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

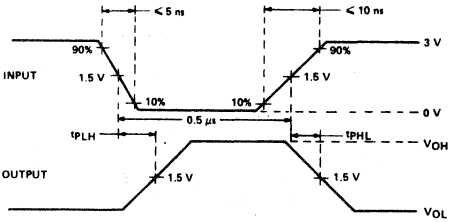
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 3		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	ns
t_{TLH}	Transition time, low-to-high-level output				8	20	ns
t_{THL}	Transition time, high-to-low-level output				10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 4	$I_O \approx$ 300 mA,	V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



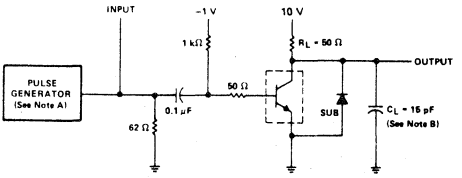
TEST CIRCUIT



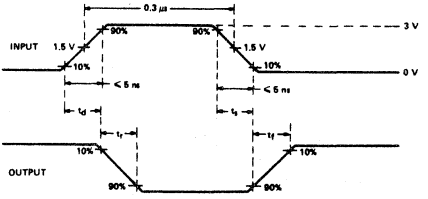
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55470 AND SN75470 ONLY)



TEST CIRCUIT

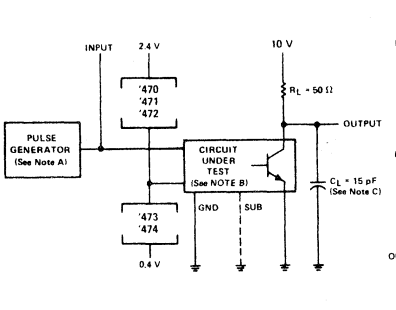


VOLTAGE WAVEFORMS

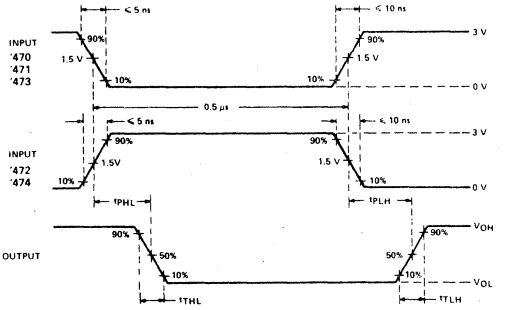
NOTES: A. The pulse generator has the following characteristics: duty cycle < 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55470 AND SN75470 ONLY)

PARAMETER MEASUREMENT INFORMATION



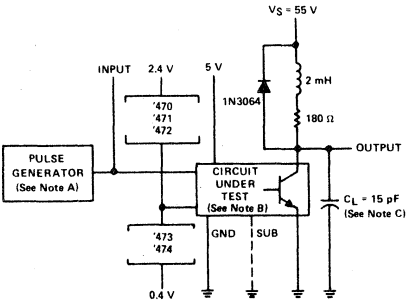
TEST CIRCUIT



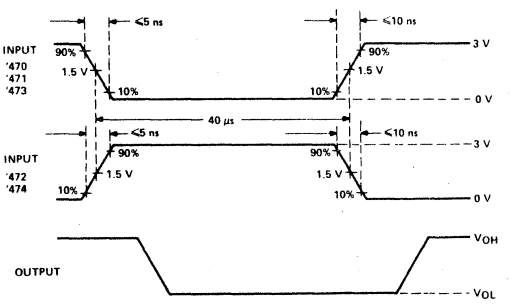
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55470 or SN75470, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} = 50\ \Omega$.
B. When testing SN55470 or SN75470, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

SERIES 75476 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12480, DECEMBER 1976 – REVISED AUGUST 1977

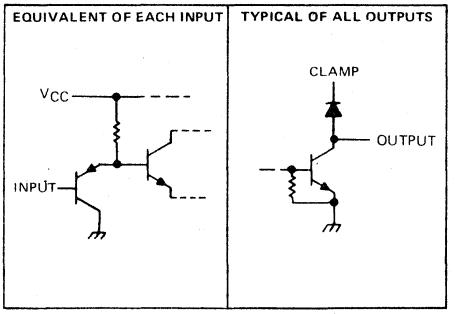
- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typical)
- High-Speed Switching
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

description

Series 75476 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series 75476 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

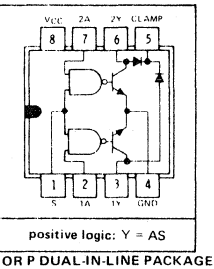


SN75476
FUNCTION TABLE
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

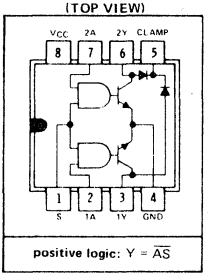


SN75477
FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

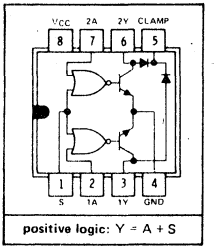


SN75478
FUNCTION TABLE
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

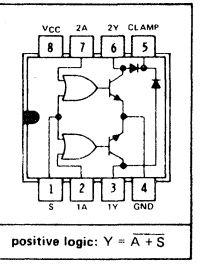


SN75479
FUNCTION TABLE
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 400 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

4

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75476 through SN75479 chips are glass-mounted.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

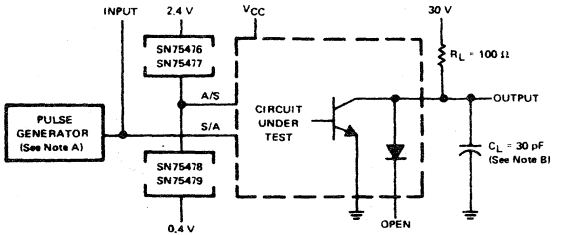
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.95	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.5$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.16	0.3	V
				$I_{OL} = 175$ mA		0.22	0.5	
				$I_{OL} = 300$ mA		0.33	0.6	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.5$ V,	$I_{OH} = 100$ μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.5$ V,	$I_R = 100$ μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.5$ V,	$I_F = 300$ mA	0.8	1.15	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.5$ V,	$V_I = 0.8$ V		−80	−110	μA
		Strobe S				−160	−220	
I_{CCH}	Supply current, outputs high	SN75476	$V_{CC} = 5.5$ V	$V_I = 5$ V		10	17	mA
		SN75477		$V_I = 0$		10	17	
		SN75478		$V_I = 5$ V		10	17	
		SN75479		$V_I = 0$		10	17	
I_{CCL}	Supply current, outputs low	SN75476	$V_{CC} = 5.5$ V	$V_I = 0$		54	75	mA
		SN75477		$V_I = 5$ V		54	75	
		SN75478		$V_I = 0$		54	75	
		SN75479		$V_I = 5$ V		54	75	

†All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

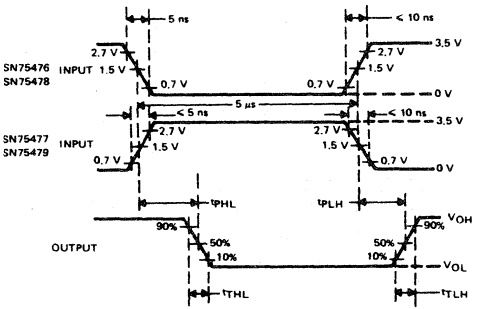
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75476			SN75477			SN75478			SN75479			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 1		100	200		100	200		100	200		100	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	300		200	300		200	300		200	300	ns
t_{TLH}	Transition time, low-to-high-level output			50	100		50	100		50	100		50	100	ns
t_{THL}	Transition time, high-to-low-level output			50	100		50	100		50	100		50	100	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O ≈ 300 mA, See Figure 2	V_S−18			V_S−18			V_S−18			V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



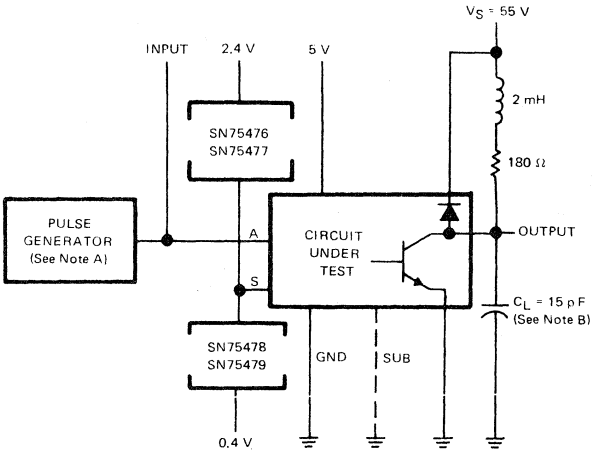
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

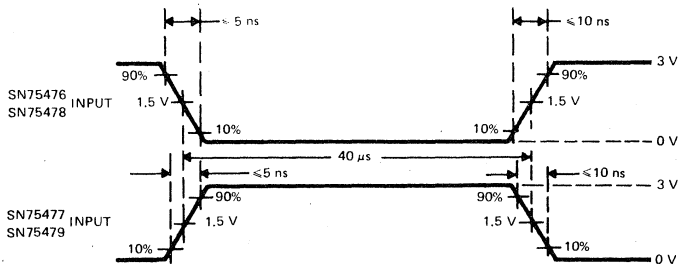
FIGURE 1–SWITCHING CHARACTERISTICS

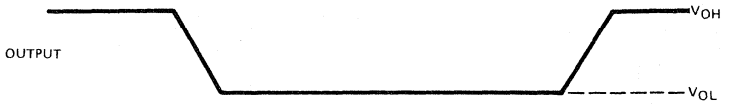
4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT





VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

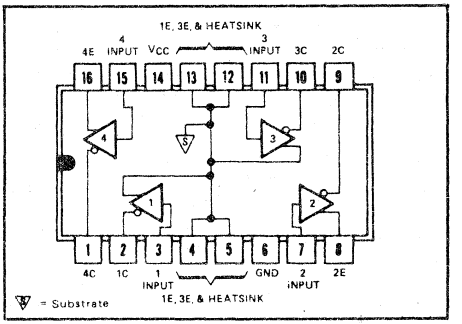
FIGURE 2–LATCH-UP TEST

TYPES UDN2841, UDN2845
QUADRUPLE HIGH-CURRENT DARLINGTON DRIVERS

BULLETIN NO. DL-S 12791, DECEMBER 1980

- For Use with Negative Supplies
- Current Sink . . . UDN2841
- Sink or Source Combination . . . UDN2845
- Output Current Capability . . . 1.5 A
- High Output-Voltage Capability . . . 50 V
- Preamplifier for High Current Gain
- Inputs Compatible With TTL, DTL, and 5-V CMOS
- Reliable Monolithic Construction
- Designed to be Interchangeable with Sprague UDN2841 and UDN2845

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)

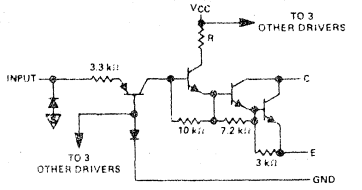


description

The quadruple darlington switches are monolithic bipolar devices especially designed for high-current, high-voltage peripheral driver applications. The devices are designed to offer solutions to interface problems involving electronic-discharge printers, bipolar and unipolar dc motor drivers, telephone relays, LEDs, PIN diodes, and other high-current loads operating from negative power supplies.

The UDN2841 is intended for current-sink applications with the load connected to ground and the device switching the negative supply. The UDN2845 is a sink and source combination for use in bipolar switching applications where both ends of the load are floating. The UDN2841 and UDN2845 each feature inputs that are compatible with standard TTL, DTL, and 5-volt CMOS signals. The p-n-p input transistor serves as a level translator and the first n-p-n transistor stage is designed to provide sufficient current gain to drive the output darlington-connected pair.

schematic diagram (each driver)



= Substrate

UDN2841: R = 15 kΩ each channel

UDN2845: R = 15 kΩ channels 1 and 3, R = 1 kΩ, channels 2 and 4

Resistor values shown are nominal.

Driver channels 2 and 4 have uncommitted collectors and emitters while channels 1 and 3 have emitters internally connected to the substrate. For proper operation these emitters and the substrate must be connected to the most-negative supply voltage.

The UDN2841 and UDN2845 are characterized for operation from 0°C to 70°C.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage	10 V
Substrate voltage	−50 V
Peak output current	1.75 A
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

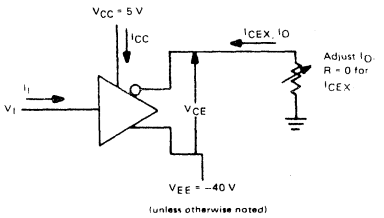
NOTES: 1. All voltage values, except collector-emitter voltage, are with respect to the network ground terminal.
2. For operation above 25°C free-temperature, derate to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted), V_{CC} = 5 V, see figures 1 and 2

PARAMETER		TEST CONDITIONS		UDN2841			UDN2845			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	V_{EE} = −50 V, V_I = 0.4 V, I_O = 100 mA		35	50		35	50		V
I_{CEX}	Collector output cutoff current	V_{EE} = −50 V, V_I = 0.4 V				100			100	μA
		V_{EE} = −50 V, V_I = 0.4 V, T_A = 70°C				500			500	
$I_{I(on)}$	On-state input current	I_O = 0.5 A	Drivers 1 and 3		300	500		300	500	μA
			Drivers 2 and 4		300	500		350	525	
$V_{I(on)}$	On-state input voltage	I_O = 1.5 A, See Note 3				2.4			2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_I = 2.4 V, See Note 3	I_O = 0.5 A			1			1	V
			I_O = 1 A			1.25			1.25	
			I_O = 1.5 A			1.6			1.6	
I_{CC}	Supply current (each driver)	I_O = 0.5 A, See Note 3	Drivers 1 and 3		2.5	3.75		2.5	3.75	mA
			Drivers 2 and 4		2.5	3.75		3.75	7.5	

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

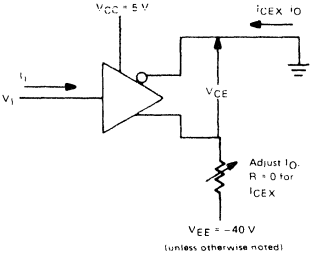
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTE: UDN2841 driver channels 1 through 4 and UDN2845 driver channels 1 and 3 only.

FIGURE 1 – SINK-CURRENT DRIVER



TEST CIRCUIT

NOTE: UDN2845 driver channels 2 and 4 only

FIGURE 2 – SOURCE-CURRENT DRIVER

THERMAL INFORMATION

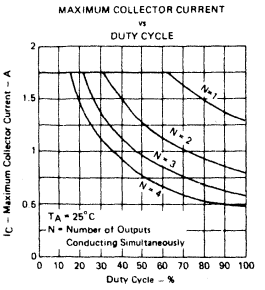


FIGURE 3

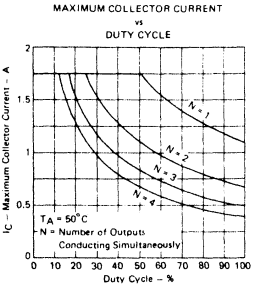


FIGURE 4

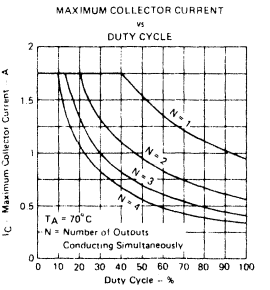


FIGURE 5

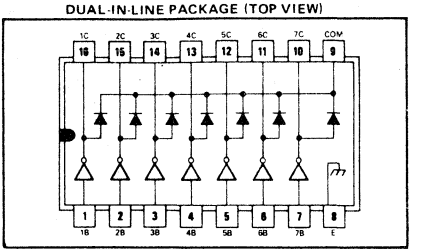
TYPES ULN2001A THRU ULN2005A DARLINGTON TRANSISTOR ARRAYS

BULLETIN NO. DL-S 12467, DECEMBER 1976 – REVISED DECEMBER 1980

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Designed to be Interchangeable with Sprague ULN2001A Series

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

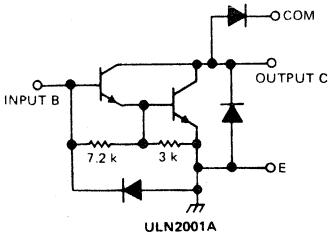


description

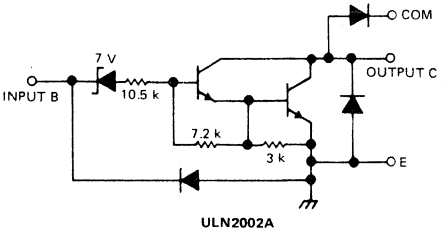
The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current darlington transistor arrays. Each comprises seven n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-volt (otherwise interchangeable) versions, see the SN75465 through SN75469.

The ULN2001A is a general-purpose array and may be used with DTL, TTL, P-MOS, CMOS, etc. The ULN2002A is specifically designed for use with 14- to 25-volt P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The ULN2004A has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the ULN2003A while the required voltage is less than that required by the ULN2002A. The ULN2005A has a 1.05-kΩ series base resistor and is especially designed for use with TTL where higher output current is required and loading of the driving source is not a concern.

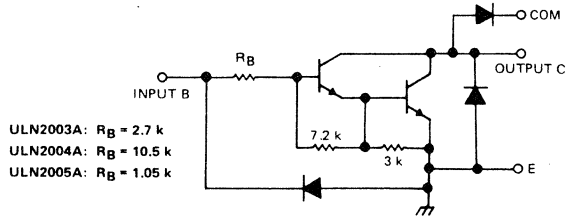
schematics (each darlington pair)



ULN2001A



ULN2002A



ULN2003A: R_B = 2.7 k
ULN2004A: R_B = 10.5 k
ULN2005A: R_B = 1.05 k

ULN2003A, ULN2004A, ULN2005A

All resistor values shown are nominal and in ohms.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage . . . . . 50 V
Input voltage (see Note 1): ULN2002A, ULN2003A, ULN2004A . . . . . 30 V
ULN2005A . . . . . 15 V
Peak collector current (see Figures 14 and 15) . . . . . 500 mA
Continuous input current, ULN2001A only . . . . . 25 mA
Total substrate-terminal current: J package . . . . . −500 mA
N package . . . . . −2.5 A
Continuous dissipation (total package) at (or below)
25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds, J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds, N package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, ULN2001A through ULN2005A chips are glass-mounted.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2001A			ULN2002A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	μA
			V_{CE} = 50 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V				50			50	μA
			V_R = 50 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A MIN	ULN2003A TYP	ULN2003A MAX	ULN2004A MIN	ULN2004A TYP	ULN2004A MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	μA
			V_{CE} = 50 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1.0	1.45	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	
			I_I = 350 μA,	I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V,				50			50	μA
			V_R = 50 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 305 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2005A MIN	ULN2005A TYP	ULN2005A MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50	μA
			V_{CE} = 50 V,	I_I = 0, T_A = 70°C			100	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V,	I_C = 500 μA, T_A = 70°C	50	65		μA
I_I	Input current	4	V_I = 3 V			1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 350 mA			2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1.0	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V				50	μA
			V_R = 50 V,	T_A = 70 C			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2	V
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to high-level output	See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 10	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

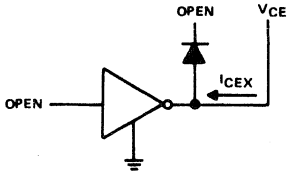


FIGURE 1–I_{CEX}

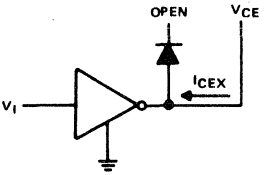


FIGURE 2–I_{CEX}

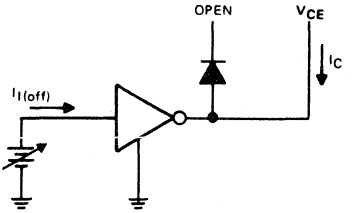


FIGURE 3–$I_{I(off)}$

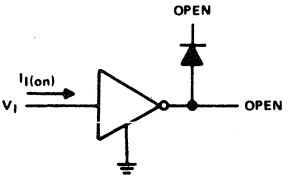
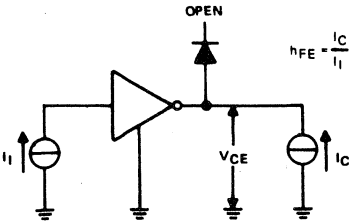


FIGURE 4–I_I



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 5–h_{FE}, $V_{CE(sat)}$

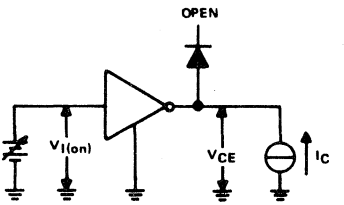


FIGURE 6–$V_{I(on)}$

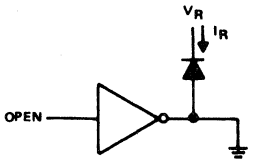


FIGURE 7–I_R

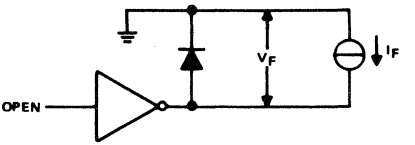
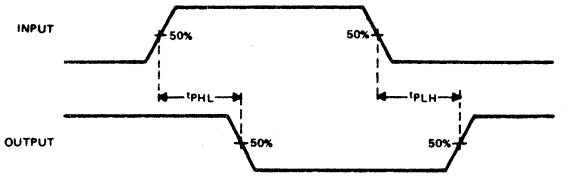


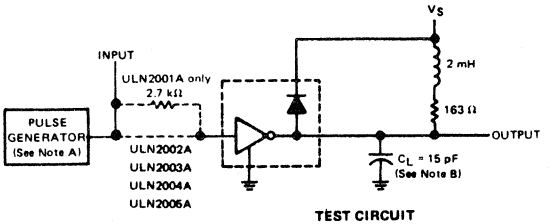
FIGURE 8–V_F

PARAMETER MEASUREMENT INFORMATION

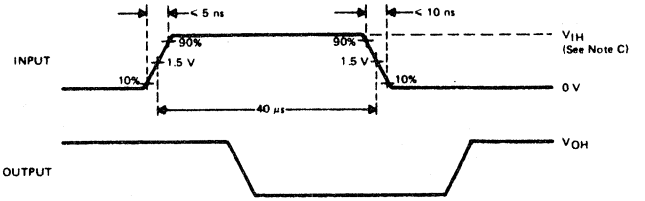


VOLTAGE WAVEFORMS

FIGURE 9–PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A, ULN2003A and the ULN2005A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

FIGURE 10–LATCH-UP TEST

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

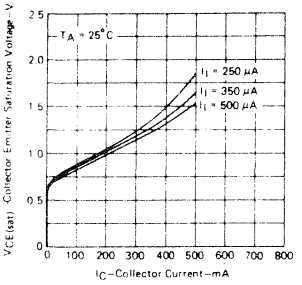


FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

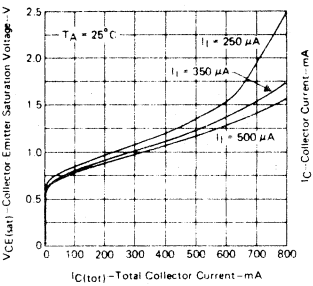


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

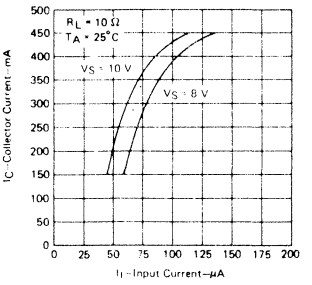


FIGURE 13

THERMAL INFORMATION

J PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

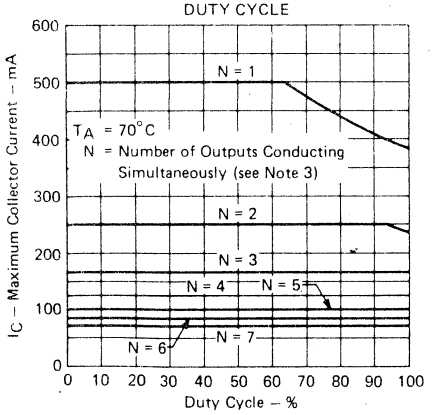


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

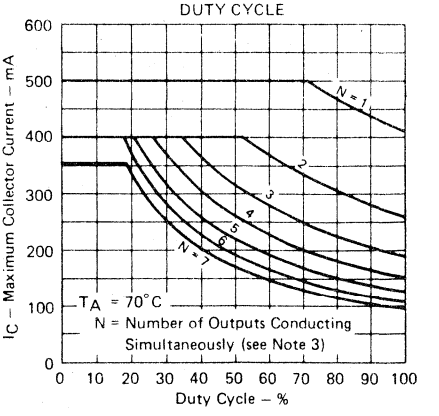
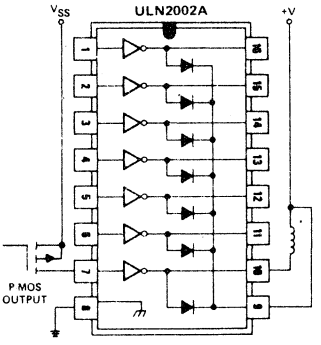


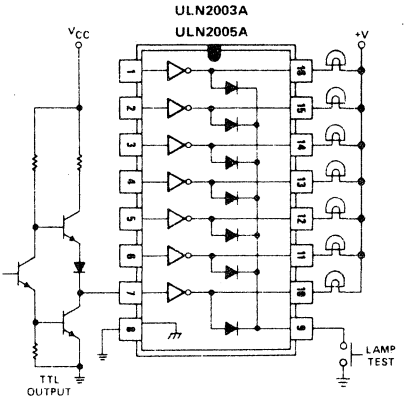
FIGURE 15

NOTE 3: For the J package, N x I_C must not exceed 500 mA (maximum substrate-terminal current). For the N package N x I_C must not exceed 2.5 A.

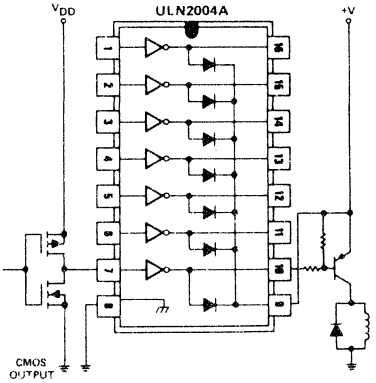
TYPICAL APPLICATION DATA



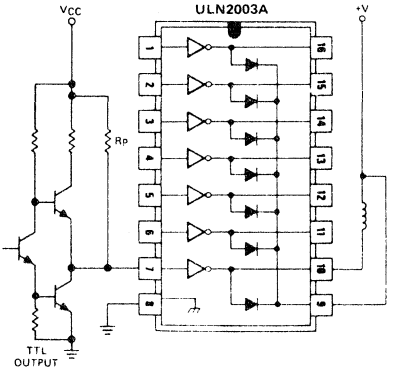
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS



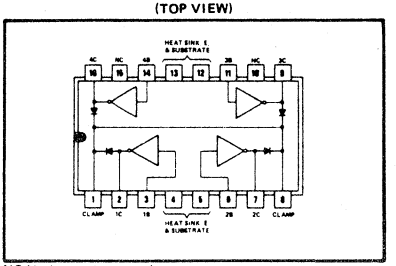
USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

TYPES ULN2064, ULN2065, ULN2066, ULN2067
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12681, DECEMBER 1979 – REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- ULN2064 and ULN2065 Have TTL- and DTL-Compatible Inputs
- ULN2066 and ULN2067 Have CMOS- and PMOS-Compatible Inputs
- Designed for Interchangeability with Sprague ULN2064 thru ULN2067, Respectively

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



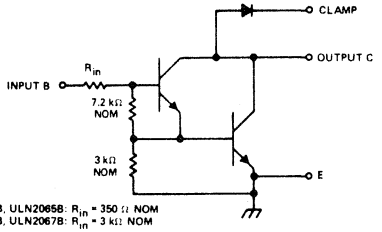
NC-No internal connection

description

The ULN2064, ULN2065, ULN2066, and ULN2067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The ULN2064 and ULN2065 are intended for use with TTL, DTL, and 5-volt MOS logic. The ULN2066 and ULN2067 are intended for use with PMOS and higher voltage CMOS logic. The ULN2064, ULN2065, ULN2066, and ULN2067 are characterized for operations from 0°C to 70°C.

schematic (each darlington pair)



ULN2064B, ULN2065B: R_{in} = 350 Ω NOM
ULN2066B, ULN2067B: R_{in} = 3 kΩ NOM

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2064	ULN2065	ULN2066	ULN2067	UNIT
Collector-emitter voltage	50	80	50	80	V
Input voltage (see Note 1)	15	15	30	30	V
Peak collector current (see Figures 12, 13, and 14)	1.5	1.5	1.5	1.5	A
Input current	25	25	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

4

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2064		ULN2065		ULN2066		ULN2067		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100				100			μA
			V_{CE} = 50 V, T_A = 70°C		500				500			
			V_{CE} = 80 V				100				100	
			V_{CE} = 80 V, T_A = 70°C				500				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3					mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6					
			V_I = 5 V					0.9	1.8	0.9	1.8	
			V_I = 12 V					2.75	5.2	2.75	5.2	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2		6.5		6.5	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.5		2.5		10		10	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.1		1.1		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 3		1.4				1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 3				1.5				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50				50			μA
			V_R = 50 V, T_A = 70°C		100				100			
			V_R = 80 V				50				50	
			V_R = 80 V, T_A = 70°C				100				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75		1.75		1.75	V
			I_F = 1.5 A, See Note 3		2		2		2		2	

NOTE 3: These parameters must be measured on one output at a time using pulse techniques: t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

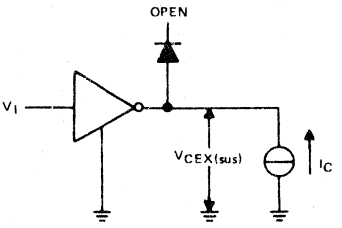


FIGURE 1–$V_{CEX(sus)}$

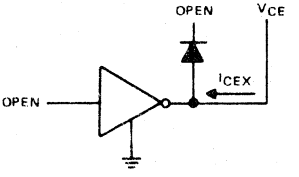


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

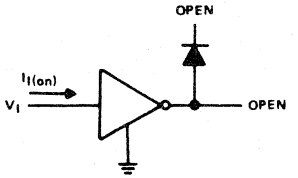


FIGURE 3–$I_{I(on)}$

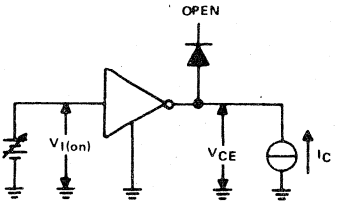


FIGURE 4–$V_{I(on)}$

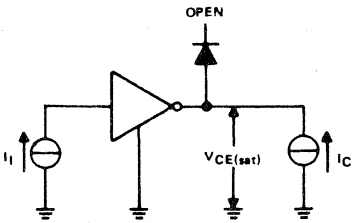


FIGURE 5–$V_{CE(sat)}$

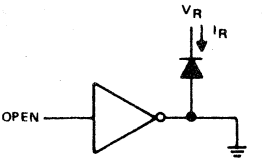


FIGURE 6–I_R

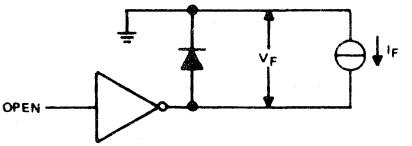
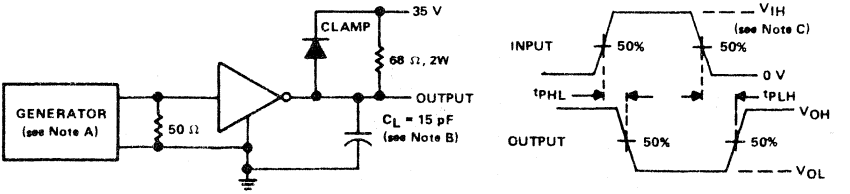


FIGURE 7–V_F



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.
C. V_{IH} = 2.5 V for ULN2064 and ULN2065. V_{IH} = 10 V for ULN2066 and ULN2067.

FIGURE 8 – SWITCHING TIMES

4

ELECTRICAL CHARACTERISTICS

ULN2064, ULN2065
INPUT CURRENT
vs
INPUT VOLTAGE

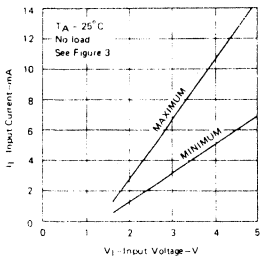


FIGURE 9

ULN2066, ULN2067
INPUT CURRENT
vs
INPUT VOLTAGE

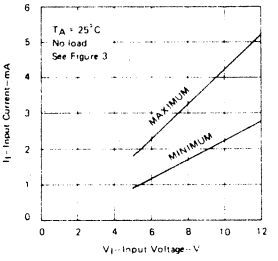


FIGURE 10

COLLECTOR CURRENT
vs
BASE CURRENT

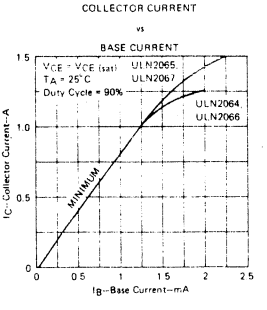


FIGURE 11

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

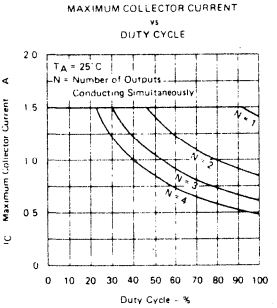


FIGURE 12

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

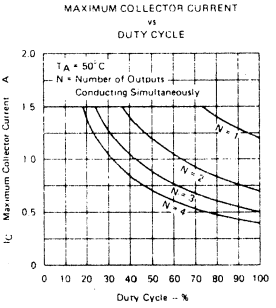


FIGURE 13

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

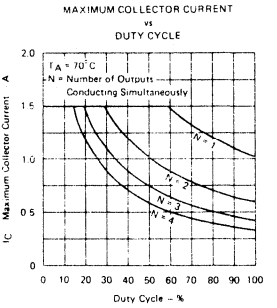


FIGURE 14

TYPICAL APPLICATION DATA

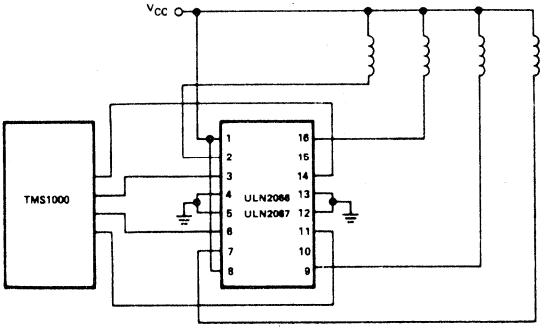


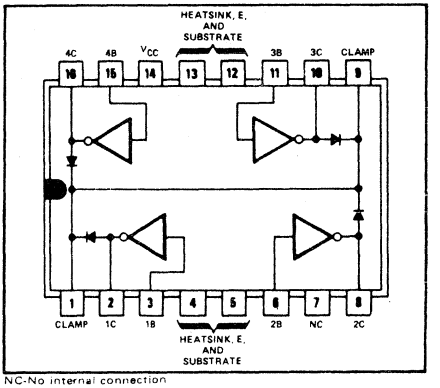
FIGURE 15 – RELAY DRIVER INTERFACE

TYPES ULN2068, ULN2069
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12751, MAY 1980–REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible with TTL and 5-Volt CMOS
- Designed for Interchangeability with Sprague ULN2068 and ULN2069

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



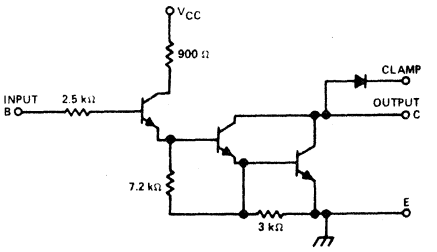
NC-No internal connection

description

The ULN2068 and ULN2069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-volt CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The ULN2068 and ULN2069 can sink up to 1.5 amperes per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge). The ULN2068 and ULN2069 are characterized for operation from 0°C to 70°C.

schematic (each switch)



Resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2068	ULN2069	UNIT
Collector-emitter voltage	50	80	V
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	15	15	V
Peak collector current (see Figures 10, 11, and 12)	1.5	1.5	A
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2068 MIN	ULN2068 MAX	ULN2069 MIN	ULN2069 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V		250		250	μA
			V_I = 3.75 V		1000		1000	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.4		2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	V_I = 2.4 V, I_C = 500 mA		1.1		1.1	V
			V_I = 2.4 V, I_C = 750 mA		1.2		1.2	
			V_I = 2.4 V, I_C = 1 A		1.3		1.3	
			V_I = 2.4 V, I_C = 1.25 A, See Note 3		1.4			
			V_I = 2.4 V, I_C = 1.5 A, See Note 3				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50			μA
			V_R = 50 V, T_A = 70°C		100			
			V_R = 80 V				50	
			V_R = 80 V, T_A = 70°C				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75	V
			I_F = 1.5 A, See Note 3		2		2	
I_{CC}	Supply current (only one switch conducting)	8	V_I = 2.4 V, I_C = 500 mA		6		6	mA

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

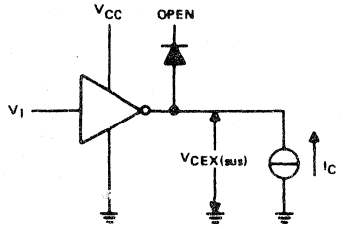


FIGURE 1–$V_{CEX(sus)}$

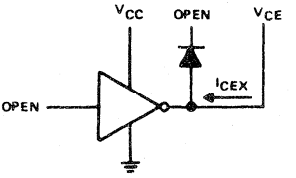


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

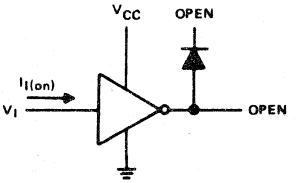


FIGURE 3–$I_{I(on)}$

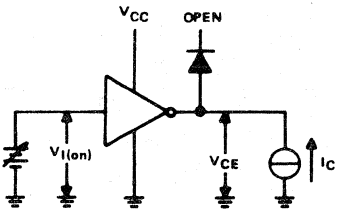


FIGURE 4–$V_{I(on)}$

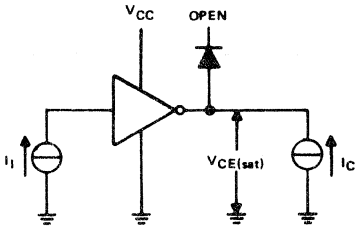


FIGURE 5–$V_{CE(sat)}$

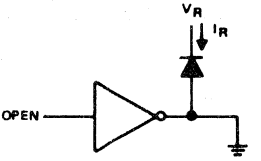


FIGURE 6–I_R

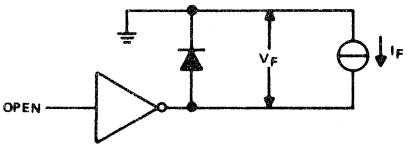


FIGURE 7–V_F

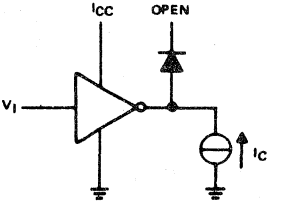
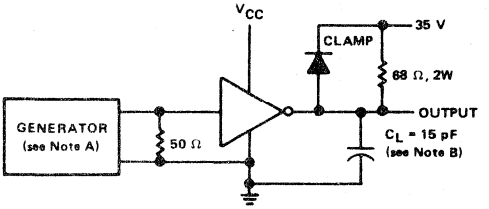
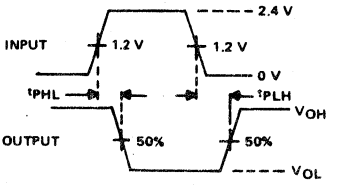


FIGURE 8–I_{CC}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 9–SWITCHING TIMES

THERMAL INFORMATION

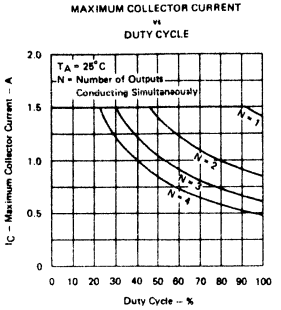


FIGURE 10

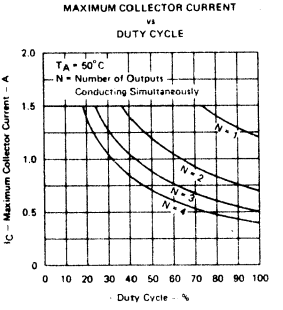


FIGURE 11

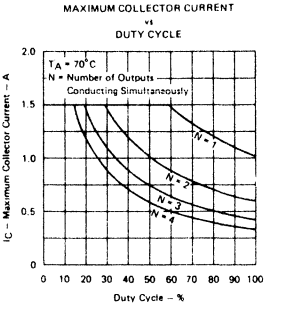


FIGURE 12

TYPICAL APPLICATION DATA

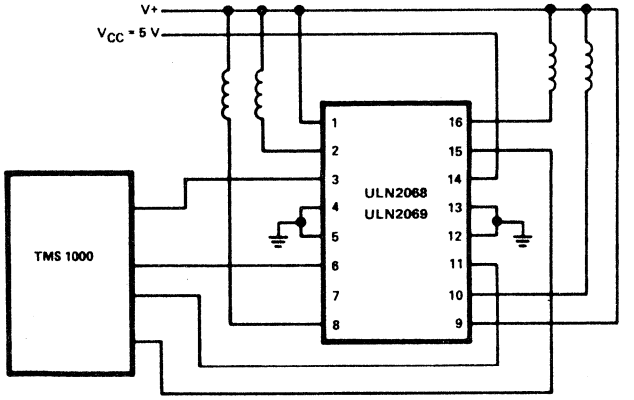


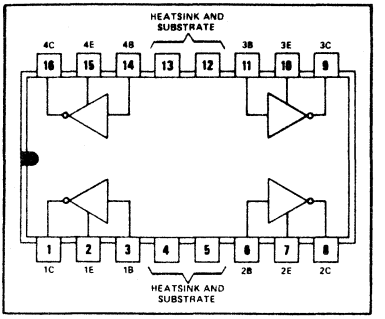
FIGURE 13–RELAY DRIVER INTERFACE

TYPES ULN2074, ULN2075
QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12750, MAY 1980 – REVISED FEBRUARY 1981

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible With TTL or 5-V CMOS
- Designed for Interchangeability with Sprague ULN2074 and ULN2075

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

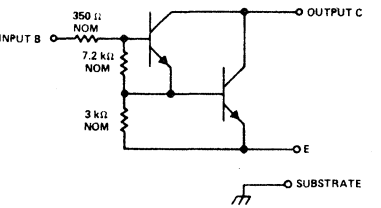
The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 amperes for each darlington pair.

The ULN2074 and ULN2075 are unique general-purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

For proper operation, the substrate must be connected to the most negative voltage.

The ULN2074 and ULN2075 are characterized for operation from 0°C to 70°C.

schematic (each switch)



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2074	ULN2075	UNIT
Collector-emitter voltage	50	80	V
Input voltage with respect to substrate	30	60	V
Peak collector current (see Figures 9, 10, and 11)	1.5	1.5	A
Input current	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2075	2075	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2074 MIN	ULN2074 MAX	ULN2075 MIN	ULN2075 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3	mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 2		2.5		2.5	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 2		1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 2				1.5	

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

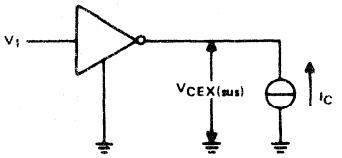


FIGURE 1–$V_{CEX(sus)}$

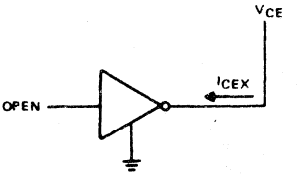


FIGURE 2–I_{CEX}

PARAMETER MEASUREMENT INFORMATION

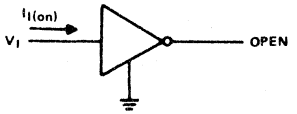


FIGURE 3–$I_{I(on)}$

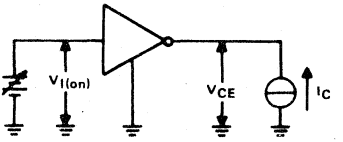


FIGURE 4–$V_{I(on)}$

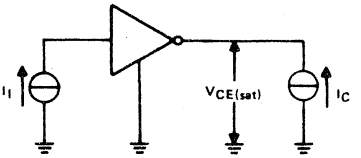
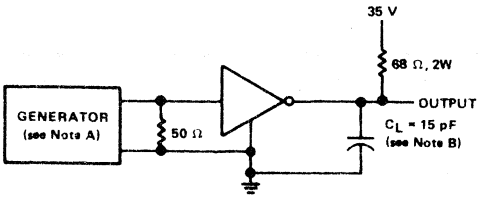
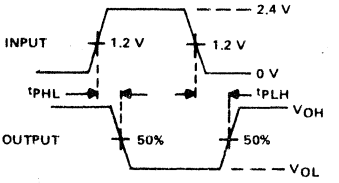


FIGURE 5–$V_{CE(sat)}$



TEST CIRCUITS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 6--SWITCHING CHARACTERISTIC

ELECTRICAL CHARACTERISTICS

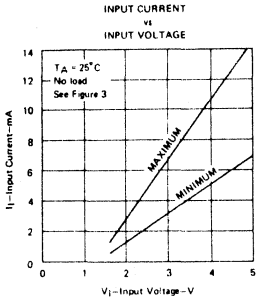


FIGURE 7

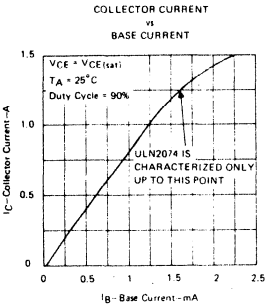


FIGURE 8

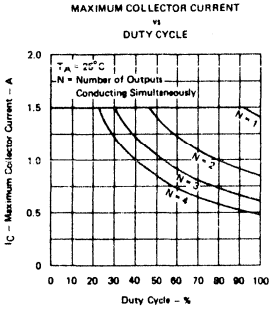


FIGURE 9

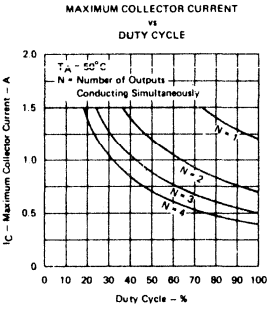


FIGURE 10

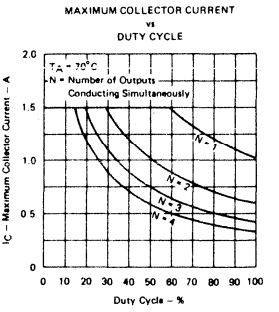


FIGURE 11

TYPICAL APPLICATION DATA

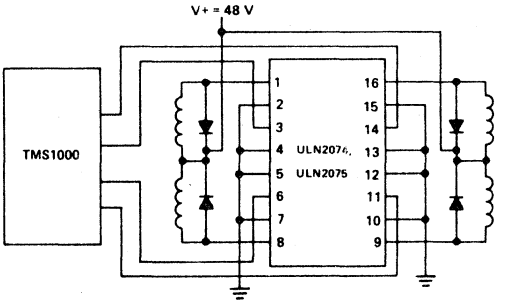


FIGURE 12–RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES

general

The applications have been divided into several categories. Even though a particular device is shown in a given application, that does not mean it is the only device that can be used. For example, the SN75451B is shown as a lamp driver. Depending on the voltage and current requirements, other devices may be used such as the SN75401, SN75411, SN75431, SN75461, SN75471, and so forth.

The categories into which the applications have been divided are as follows:

Lamp drivers
Relay/solenoid drivers
Hammer drivers
Core memory driver and inhibit control
Digital comparators
Detectors
TTL-to-MOS and MOS-to-TTL drivers
Inverting buffers for high-current loads
Miscellaneous applications

lamp drivers

Figures 1 and 2 show basic lamp driver applications.

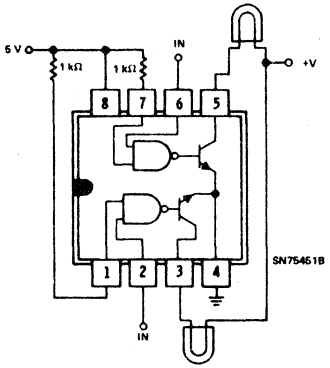


FIGURE 1 – LAMP DRIVER

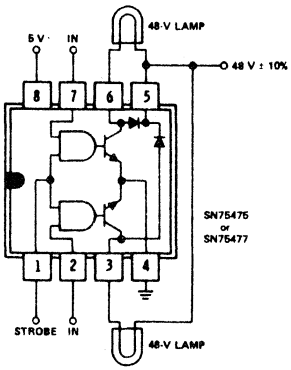


FIGURE 2 – HIGH-VOLTAGE LAMP DRIVER WITH INDUCTIVE CLAMP-DIODE PROTECTION

Note that in any lamp-driver application the turn-on surge current of a cold lamp may be as much as 10 times the normal on current; a 100-mA lamp may have a 1-amp turn-on surge. Peripheral drivers can handle 100-mA operating currents, but a 1-amp surge is far more demanding. The normal maximum continuous collector current rating is 300 or 500 mA, although a 500 or 1000 mA (maximum) surge current may be sustained for duty cycles not to exceed 50% or 40%, respectively, with on time less than 10 milliseconds. Current peaks exceeding these maximums may cause device deterioration.

lamp drivers (continued)

Several methods can be employed to limit surge currents when using peripheral drivers. These methods allow 200- to 300-mA lamps to be driven without exceeding the surge limits of the devices. One method that can be used employs "keep alive" resistors as shown in Figure 3. These resistors maintain off-state current at approximately 10%. This will reduce the surge current.

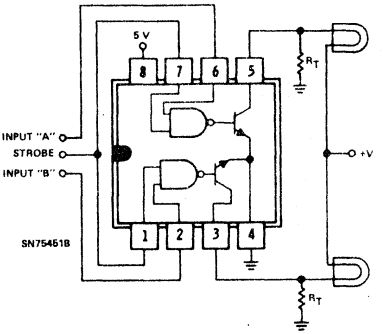


FIGURE 3 – LAMP DRIVERS WITH "KEEP ALIVE" RESISTORS

With the basic SN75450B, SN75460, or SN75470, the availability of the gate output and base leads, as well as the emitter lead, allows use of several methods of current limiting. One method is to place a current-limiting resistor between the gate output and the transistor base, as shown in Figure 4. With an operating load current of 100 mA, a typical h_{FE} of 50 for the output transistor, and selecting 250 mA as the peak surge, the value of the base resistor can be determined from the following equation:

$$R = \frac{V_{OH} - V_{BE}}{I_B \text{ (limit)}}$$

where:

V_{OH} = 3.3 V (typical)

V_{BE} = 0.85 V (typical)

$$I_B \text{ (limit)} = \frac{I_C \text{ (limit)}}{h_{FE}} = \frac{250 \text{ mA}}{50} = 5 \text{ mA}$$

Therefore:

$$R = \frac{3.3 - 0.85}{0.005} \approx 500\ \Omega$$

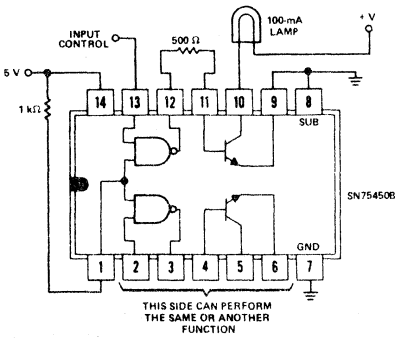


FIGURE 4 – LAMP DRIVER WITH BASE RESISTOR SURGE LIMITING

This method is not the best because of lack of control over critical parameters. A worst-case condition of low V_{BE}, high h_{FE}, and high gate output would result in peak surges in excess of 500 mA.

Figure 5 shows a configuration that is less susceptible to variations in parameters. The emitter resistor is small enough to be of little significance at the steady-state on level, but will limit the peak levels. In this example, a GE1815 lamp was used and the actual steady-state current was 191 mA. With a typical gate V_{OH} of 3.3 volts and a V_{BE} of 0.95 volt, (at 200 mA) the transistor will saturate and limit when its emitter voltage reaches $V_{OH} - V_{BE}$, or 2.35 volts; this occurs at V_E/R_E, or about 345 mA. Figure 6 shows the output current waveform.

lamp drivers (continued)

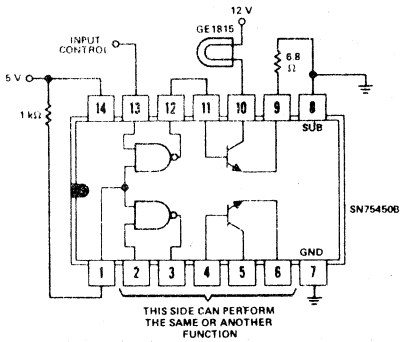


FIGURE 5 – LAMP DRIVER WITH EMITTER RESISTOR SURGE LIMITING

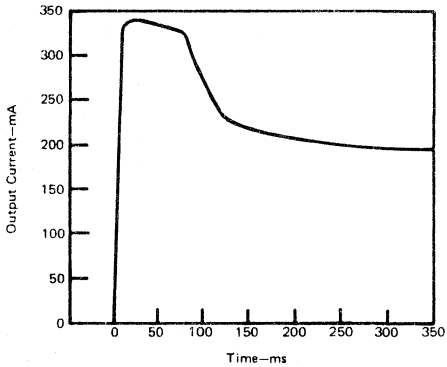


FIGURE 6 – OUTPUT CURRENT vs TIME FOR CIRCUIT IN FIGURE 5

In this example the peak surge is sustained for about 150 milliseconds. As the lamp warms, its impedance rises and the load current drops rapidly to the steady-state level. Even with worst-case parameters the surge current would be under 500 mA. The efficient performance of this type of current limiting explains its popularity for lamp-driver applications.

Improved accuracy and consistent performance can be achieved by utilizing one of the output transistors as a current-sensing device to clamp the lamp driver as shown in Figure 7. In this circuit the lamp current must flow through the 1.9-ohm resistor in the emitter of the lamp driver. The first advantage is that the resistor is smaller than that required in the previous circuit, and has even less effect on the steady-state operating level. The base-emitter junction of Q2 is connected across the 1.9-ohm resistor, with its collector tied to the base of Q1 in a typical current-limiting mode. A V_{BE} of only about 0.6 volt begins to turn Q2 on, clamping the base drive into Q1. Clamping occurs at an output current equal to $V_{BE}/1.9\ \Omega$, or $0.6\ V/1.9\ \Omega$; the output clamp level is then 316 mA. As in the previous application, the surge current lasts for about 100 milliseconds before decreasing rapidly to the quiescent level of 190 to 200 mA.

Two important precautions should be kept in mind when using this type of surge protection; (1) surge currents should not be allowed to exceed the driver surge rating under any conditions; and (2) current limiting must not take place during steady-state operations, as this would increase driver power dissipation and could cause failure.

lamp drivers (continued)

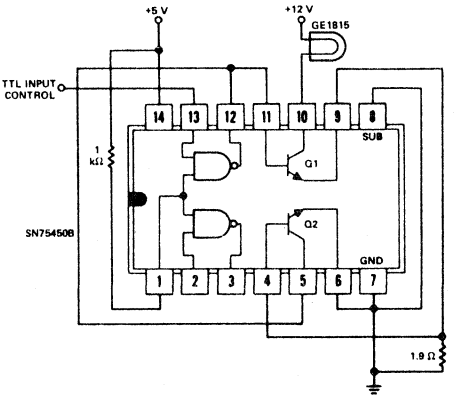


FIGURE 7 – LAMP DRIVER WITH CURRENT-SENSING SURGE PROTECTION

Another method is basically to use two switches; one to turn on the lamp with current limiting and the second to take over, after a delay, without current limiting. This eliminates the effects of parameter variation without reducing the quiescent operating level of the lamp. Such a circuit using the SN75452B is shown in Figure 8. A high-level input turns Q1 on immediately, while Q2 is delayed by the input RC network, allowing about 200 milliseconds of limited-current warm-up before turning the lamp on fully. Figure 9 shows the current levels versus time, and the effect of the warm-up mode on resulting peak levels.

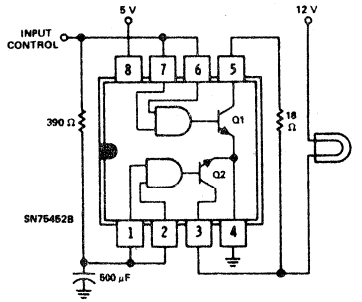


FIGURE 8 – LAMP DRIVER WITH WARM-UP CIRCUIT

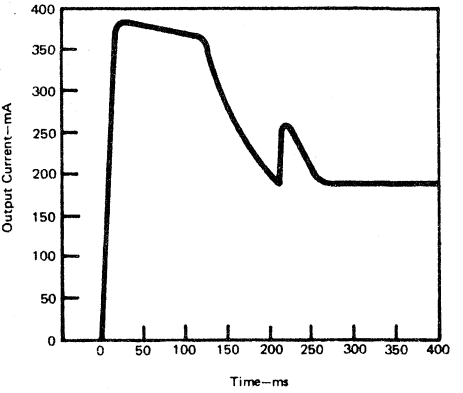


FIGURE 9 – OUTPUT CURRENT vs TIME FOR CIRCUIT IN FIGURE 8

lamp drivers (continued)

Another interesting lamp-driver application is depicted in Figure 10, showing the SN75450B as a panel-light intensity control. Controllable feedback around the gate allows its operation in the linear region, thus providing variable drive to the output transistor. An emitter resistor as shown may be used to limit initial turn-on surges. In this application a large amount of power will be dissipated in the output transistor at half-power operating levels.

Care must be taken not to exceed the total power-dissipation capability of the drivers. In a typical application the gate output will be only about 2.2 volts because of operation within the linear region. A control setting of about 280 ohms puts the gate in its linear region. A control setting of 100 to 150 ohms turns off the lamp, and a setting of 700 to 800 ohms will yield a full-on condition.

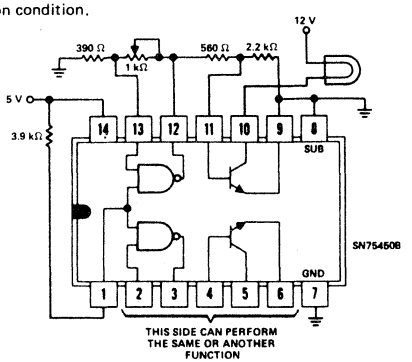


FIGURE 10 – PANEL-LIGHT INTENSITY CONTROL

relay/solenoid drivers

Figures 11 and 12 show typical relay/solenoid driver applications. Note that when using drivers that do not have output clamp diodes provided internally, these diodes should be provided externally across the inductive load as shown in Figure 12.

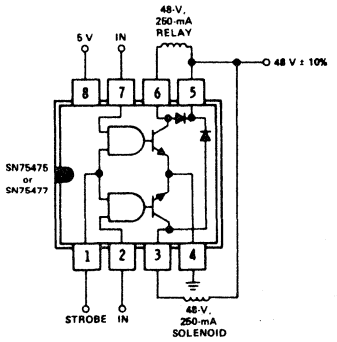


FIGURE 11 – HIGH-VOLTAGE RELAY/SOLENOID DRIVER

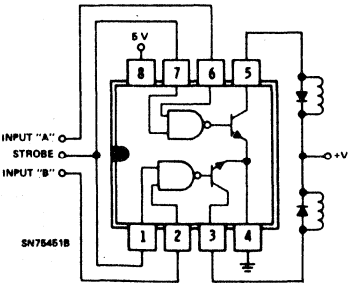


FIGURE 12 – RELAY/SOLENOID DRIVER WITH EXTERNAL CLAMP DIODES

TYPICAL APPLICATIONS

relay/solenoid drivers (continued)

In some applications involving the switching of inductive loads, the fast rise time and high-voltage transient occurring during turn-off can force the output transistor into a secondary breakdown condition. In such cases the collector voltage reaches V_{CC2} levels within a few nanoseconds. To prevent undesired breakdown, the collector-voltage slew rate should be reduced to 1 volt per nanosecond or less. This gives the gate sufficient time to provide a low base-to-ground impedance before the collector voltage is extremely high, and collector-to-emitter breakdown is prevented. To accomplish this, a 500- to 1000-pF capacitor from the collector of the output transistor to ground is usually adequate (see Figure 13).

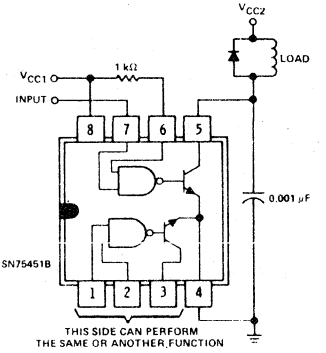


FIGURE 13–CAPACITOR PREVENTS PREMATURE COLLECTOR-TO-EMITTER BREAKDOWN

In some systems, power-supply failure or sequencing may result in the output V_{CC2} collector supply being on while the gate supply V_{CC1} is off. Under this condition the collector-to-emitter breakdown is generally lower because of the increase in base-terminating impedance resulting from the gate being off. Figure 14 shows a practical method of preventing complete loss of gate power while V_{CC2} is on; the zener diode yields a 4- to 5-volt supply level to the gate during V_{CC1} power failure.

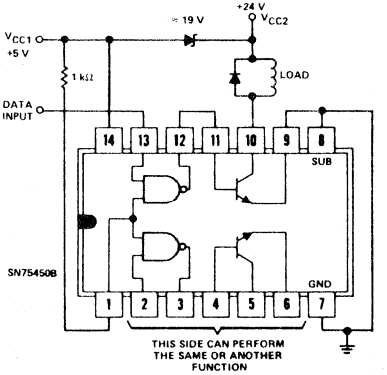


FIGURE 14–PROTECTION AGAINST LOSS OF V_{CC1}

hammer drivers

Figure 15 shows a typical hammer-driver application. If the type of driver used does not have internal output clamp diodes, a 1N3064 or similar diode should be connected across the inductive load in order to provide this protection.

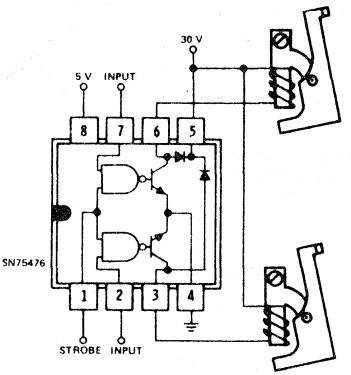
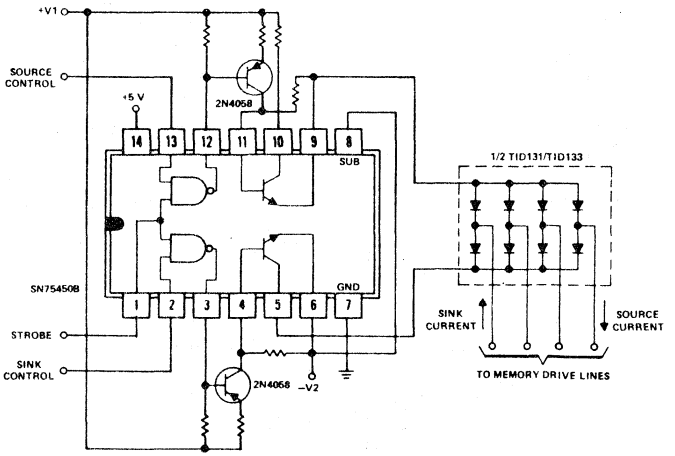


FIGURE 15 – DUAL HAMMER DRIVER

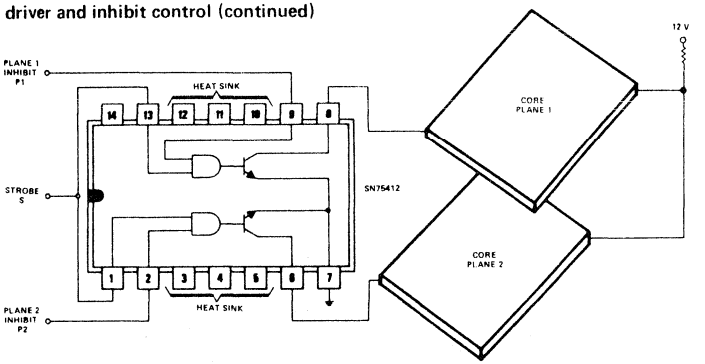
core memory driver and inhibit control



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2$ V)

FIGURE 16 – CORE MEMORY DRIVER

core memory driver and inhibit control (continued)



FUNCTION TABLE

INPUTS			OUTPUTS	
P1	P2	S	PLANE 1	PLANE 2
X	X	L	Enabled	Enabled
H	L	H	Inhibited	Enabled
L	H	H	Enabled	Inhibited
H	H	H	Inhibited	Inhibited
L	L	H	Enabled	Enabled

H = high level, L = low level, X = irrelevant

FIGURE 17–CORE MEMORY INHIBIT CONTROL

digital comparators

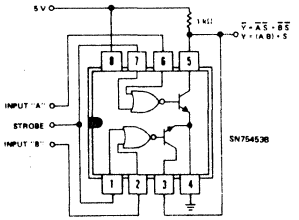


FIGURE 18–LOGIC SIGNAL COMPARATOR

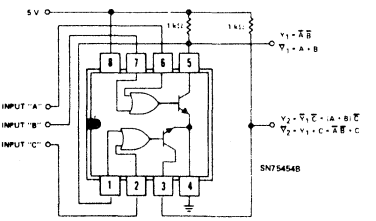


FIGURE 19–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

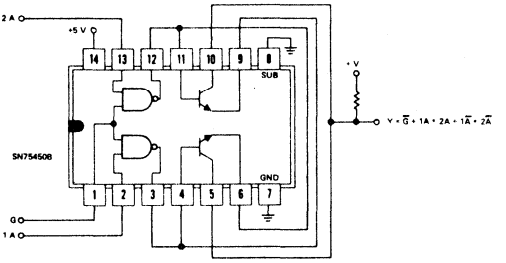
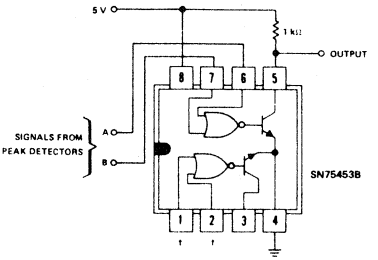
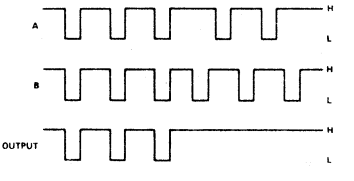


FIGURE 20–GATED COMPARATOR

detectors





Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 21—IN-PHASE DETECTOR

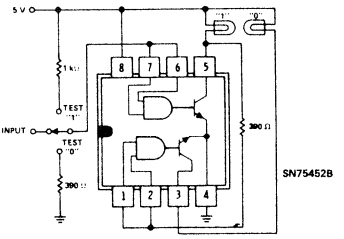
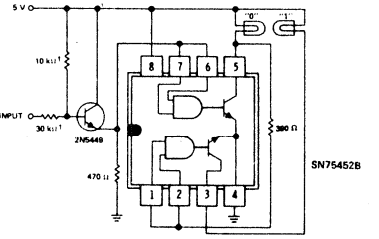


FIGURE 22—TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR



†The two input resistors must be adjusted for the level of MOS input.

FIGURE 23—MOS NEGATIVE-LOGIC-LEVEL DETECTOR

TTL-to-MOS and MOS-to-TTL drivers

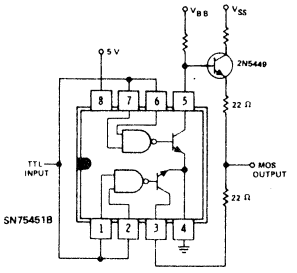
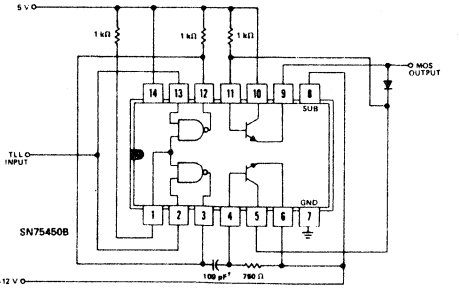


FIGURE 24—TTL-TO-MOS CLOCK DRIVER



†Value of coupling capacitor may need to be adjusted for frequency of operation.

FIGURE 25—TTL-TO-MOS CLOCK DRIVER

TTL-to-MOS and MOS-to-TTL drivers (continued)

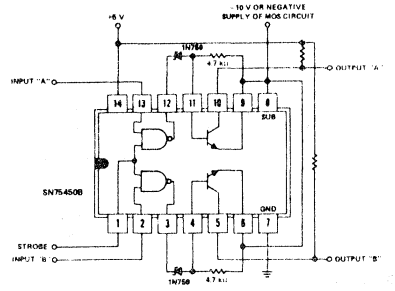


FIGURE 26–DUAL TTL-TO-MOS DRIVER

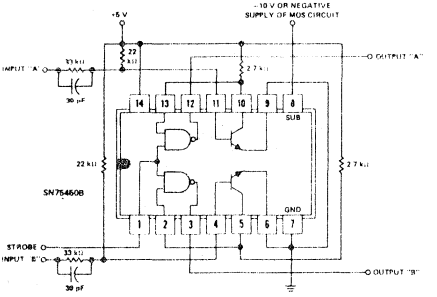


FIGURE 27–DUAL MOS-TO-TTL DRIVER

inverting buffers for high-current loads

SN75467
or
ULN2002A

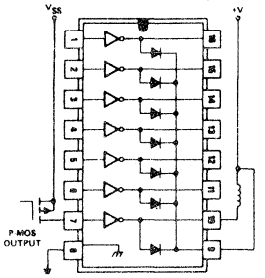


FIGURE 28–P-MOS TO LOAD

SN75468
or
ULN2003A

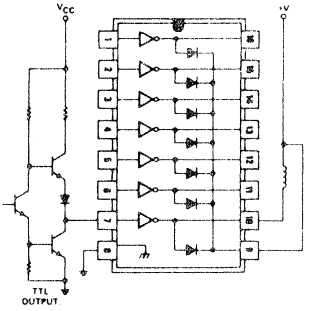


FIGURE 29–TTL TO LOAD

SN75469
or
ULN2004A

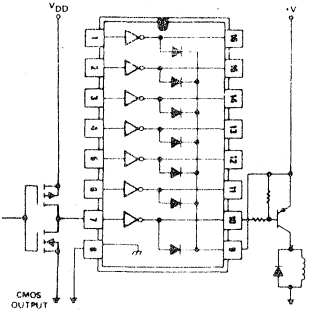


FIGURE 30–CMOS TO HIGHER CURRENT LOAD

miscellaneous applications

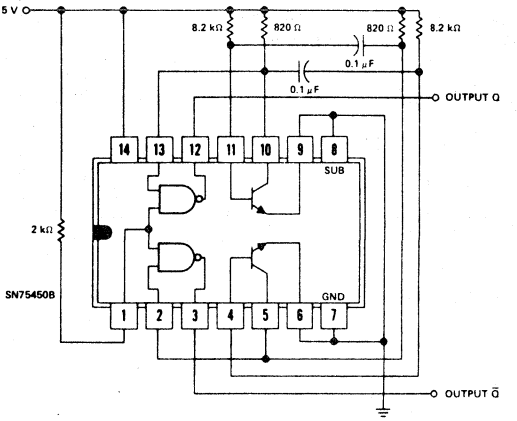


FIGURE 31–SQUARE-WAVE GENERATOR

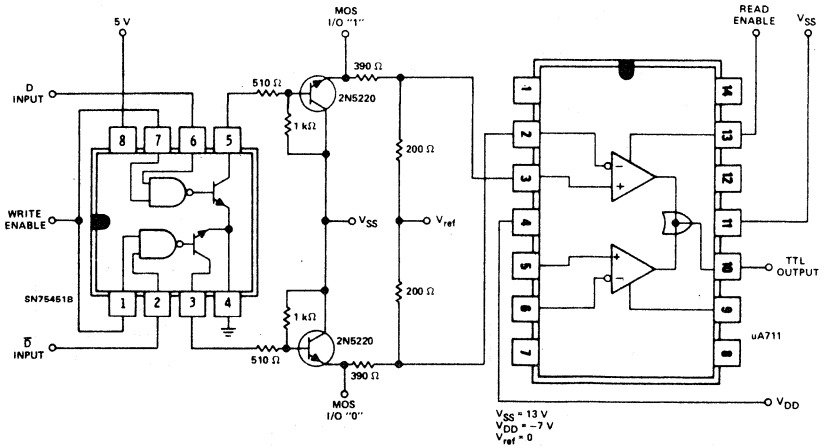


FIGURE 32–TTL COMPATIBLE DRIVER AND SENSE AMPLIFIER INTERFACE TO MOS MEMORY I/O LINES

TYPICAL APPLICATIONS

miscellaneous applications (continued)

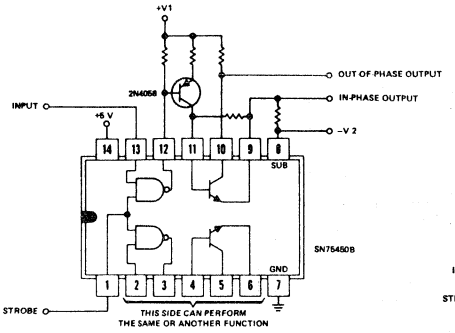


FIGURE 33–FLOATING SWITCH

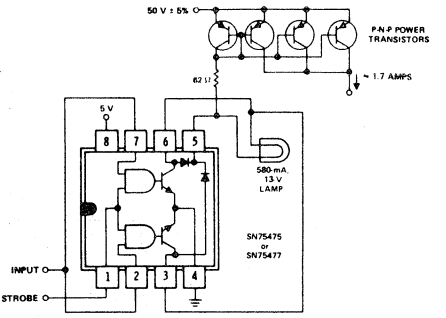


FIGURE 34–SWITCHABLE CURRENT SOURCE WITH INDICATOR LAMP

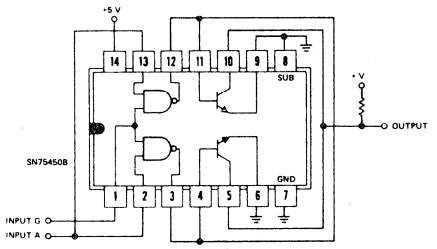


FIGURE 35–500-mA SINK

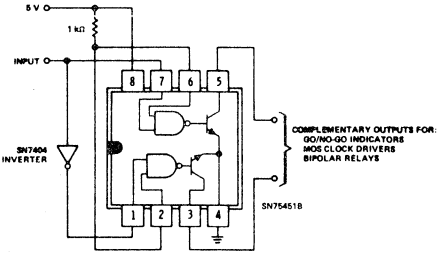
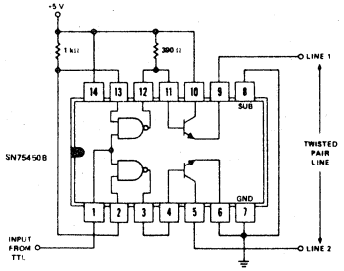


FIGURE 36–COMPLEMENTARY DRIVER



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_o/2$;
Line 2 is terminated to +5 volts through $Z_o/2$;
where Z_o is the line impedance.

FIGURE 37–BALANCED LINE DRIVER

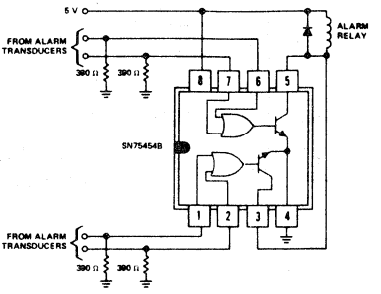


FIGURE 38–ALARM DETECTOR

5

5

APPLICATION	OUTPUT	DRIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	2	SN55158, SN75158	5–162
			SN75159	5–166
			uA9638C	5–258
		4	AM26LS31C	5–11
			MC3487	5–39
			SN55151, SN75151	5–139
			SN55153, SN75153	5–139
			SN75172	5–187
			SN75174	5–197
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	4	SN75172	5–187
			SN75174	5–197
EIA Standard RS-423A	Single-Ended	2	SN75156†	5–158
			uA9636AC	5–251
		4	SN75186†	5–234
			SN75187†	5–235
EIA Standard RS-232C	Single-Ended	2	SN75150	5–135
			SN75156†	5–158
			uA9636AC	5–251
		4	SN75186	5–234
IBM 360/370	Single-Ended	2	SN75123	5–101
			SN75126†	5–111
			SN75130†	5–116
General Purpose	Single-Ended	2	SN55121, SN75121	5–95
			SN75361A	7–30
			SN55450B, SN75450B	4–51
			SN55451B, SN75451B	4–51
		4	DS7831, DS8831	5–25
			DS7832, DS8832	5–25
	Differential	2	DS7831, DS8831	5–25
			DS7832, DS8832	5–25
			SN55109A, SN75109A	5–61
			SN55110A, SN75110A	5–61
			SN55113, SN75113	5–69
			SN55114, SN75114	5–69
			SN55183, SN75183	5–223
			SN55450B, SN75450B	4–51
			SN75112	5–61

†Future Products.

LINE RECEIVER SELECTION GUIDE

APPLICATION	INPUT	RECEIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	2	SN75157	5–159
			uA9637AC	5–255
		4	AM26LS32AC	5–15
			AM26LS33AC	5–15
			MC3486	5–35
			SN75173	5–192
			SN75175	5–202
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	4	SN75173	5–192
			SN75175	5–202
EIA Standard RS-423A	Single-Ended	2	SN75157	5–159
			uA9637AC	5–255
		4	AM26LS32AC	5–15
			AM26LS33AC	5–15
			MC3486	5–35
			SN75173	5–192
			SN75175	5–202
EIA Standard RS-232C	Single-Ended	2	SN75152	5–146
			SN75154	5–153
		4	SN75189	5–241
			SN75189A	5–241
IBM 360/370	Single-Ended	3	SN75124	5–101
		7	SN75125	5–107
			SN75127	5–107
		8	SN75128	5–112
			SN75129	5–112
General Purpose	Single-Ended	2	SN55122, SN75122	5–95
			SN55140, SN75140	5–127
			SN55141, SN75141	5–127
			SN55142A, SN75142A	5–127
			SN55143A, SN75143A	5–127
	Differential	2	SN55107A, SN75107A	5–49
			SN55107B, SN75107B	5–49
			SN55108A, SN75108A	5–49
			SN55108B, SN75108B	5–49
			SN55115, SN75115	5–69
			SN55182, SN75182	5–223
			SN75207	5–245
			SN75207B	5–245
			SN75208	5–245
			SN75208B	5–245

APPLICATION	BUS I/O	TRANSCEIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	1	SN75176	5–207
			SN75177	5–215
			SN75178	5–215
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	1	SN75176	5–207
			SN75177	5–215
			SN75178	5–215
IEEE Standard 488 GPIB	Single-Ended	4	MC3446	5–31
		8	SN75160A	5–171
			SN75161A	5–177
			SN75162A	5–177
General Purpose	Single-Ended	4	AM26S10M, AM26S10C	5–21
			AM26S11M, AM26S11C	5–21
			N8T26	5–43
			N8T26A	5–43
			SN75136	5–117
			SN55138, SN75138	5–121
		8	SN75163A	5–184
	Differential	1	SN55116, SN75116	5–87
			SN55117, SN75117	5–87
			SN55118, SN75118	5–87
			SN55119, SN75119	5–87

†Future products.

INTERFACING TO IEEE STANDARD 488 GPIB

Interfacing to IEEE Standard 488 GPIB

Because of the large number of manufacturers building programmable instruments that must be easily and economically interfaced, there is an overwhelming need for industry-wide standardization. For this reason the General-Purpose Interface Bus (GPIB) defined by IEEE Standard 488 has received wide acceptance in a short time with, at present, an estimated 500 commercially available instruments utilizing the GPIB. IEEE Std 488 has standardized the interface system used to interconnect programmable and non-programmable instruments, computers, and peripherals necessary to build an instrumentation system. This allows a user to purchase instruments from many different manufacturers and then connect them together using off-the-shelf cable. The GPIB uses a 16-line bidirectional bus that carries data at rates of up to 1 megabytes/second on eight lines, and hand-shaking and bus-management signals on the others. Up to 15 instruments can be tied together with a maximum line length of 20 meters. A typical interface arrangement is shown in Figure 1.

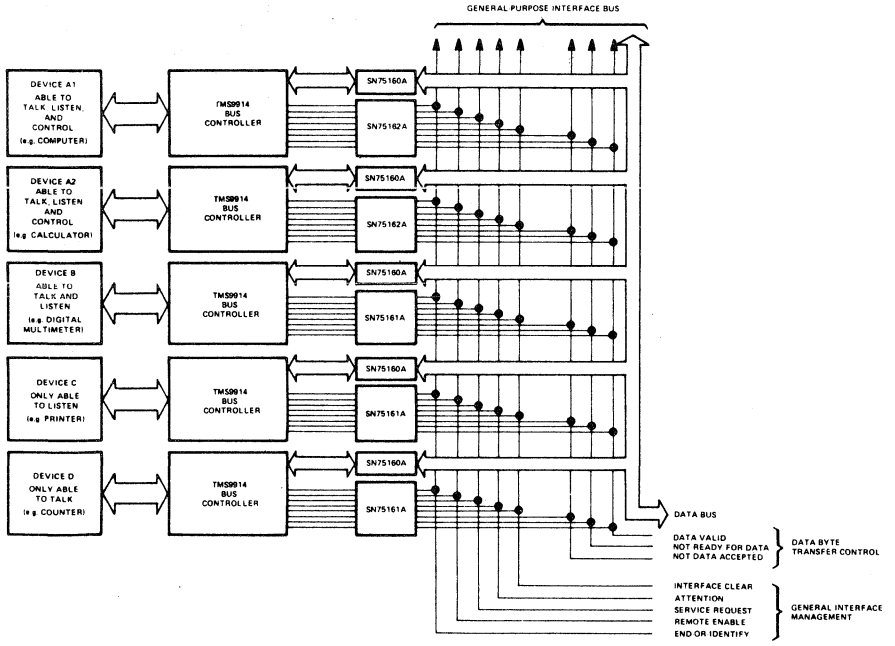


FIGURE 1–TYPICAL INTERFACE ARRANGEMENT

The TI SN75160 family of bus transceivers is designed to provide the interface between the GPIB (bus) and the bus controller. These transceivers may be used with the TMS 9914 bus controller or any of the other commercially available bus controllers. They provide the simplest method of interfacing because each part is tailored to either the 8-line data bus or the 8-line control bus and they require no extra logic or complicated board layout. All the transceivers in the SN75160 family have several features in common. Each driver output has a built-in termination network required by IEEE Std 488 designed so that, when power is removed from the transceiver, the output presents a high-impedance to the bus. Also, each receiver has a minimum of 400 millivolts hysteresis for additional noise margin. With the SN75160 family it takes only two 20-pin DIP packages to get on the GPIB.

The SN75160A is designed to implement the 8-line data bus and is pin-for-pin compatible with the original SN75160 series but with lower power and faster speeds as illustrated in Figure 2. The direction of data flow is controlled by the Talk Enable (TE) input. All eight channels are simultaneously in the receive mode when TE is low, and data is received from the bus and transferred to the bus controller. When TE is in the high state, all eight channels go to the transmit mode, and data will be transmitted onto the bus. Each driver features a totem-pole output which can actively drive the bus high or low to give the fastest data rates possible. The SN75160A has a Pull-up Enable (PE) input which, when taken low, disables the upper stage of all eight driver outputs to turn them into open-collector-type outputs. The open-collector-output mode does not allow data rates as fast as is possible with the totem-pole, but it does allow more than one instrument to be transmitting on the bus at the same time. This feature is used in parallel polling where up to eight instruments may be polled simultaneously, each responding on a single line of the eight-line data bus, thus greatly speeding up the polling process. They may then be switched back to the totem-pole mode for regular data transmission.

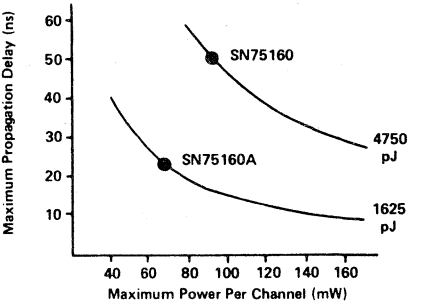


FIGURE 2

The SN75161A is used to implement the eight-line control bus. It includes with the Talk-Enable (TE) and Direction-Control (DC) inputs the necessary logic to enable each channel in the correct direction for the exchange of bus-management and hand-shaking signals. Three of the channels, (NDAC, NRFD, and SRQ) have open-collector driver outputs as required by the IEEE Std 488. These lines are always used in a Wired-OR configuration. The other five channels have totem-pole outputs.

The SN75162A offers an alternate method of implementing the eight-line control bus. It is identical to the SN75161A except that the direction of the REN and IFC channels is controlled by a separate input called the System Controller (SC). With this additional flexibility, control of the entire bus system may be transferred from one instrument to another in multiple-controller systems. Because of this extra input the SN75162A is packaged in a 22-pin DIP.

EIA Standards

There are two basic methods for electronic communication between components of a data processing system: single-ended transmission, which uses only one signal line, and differential transmission, which uses two signal lines. Single-ended transmission is used only for short distances and slower data rates since, as line length increases, it is difficult to distinguish between a valid data signal and invalid signals, such as ground shifts and noise, introduced by the environment. Differential data transmission overcomes these problems. Unwanted signals appear as common-mode levels and are rejected by the differential line receiver.

The Electronic Industries Association (EIA) has developed several specifications to standardize the interface system in data communications. Table 1 shows the key aspects of each of these specifications.

RS-232 was introduced in 1962 and has been widely used throughout the industry. It was developed for single-ended transmission over short distances at slow data rates. Today's higher-performance systems, demanding data transmission at faster rates over longer distances, are rapidly making RS-232 inadequate. The newer standard for single-ended systems, RS-423, extends the maximum data rate to 100 kilobits per second (up to 300 feet) and the maximum distance to 4000 feet (up to 1 kb/s). It also provides wave shaping dependent on data rate and wire length to control reflections and radiated emission or cross-talk. Another improvement of RS-423 is the requirement for high-impedance outputs when component power is off to avoid loading the transmission line.

For data rates over 100 kb/s and for long distances, differential transmission should be used to nullify effects of ground shifts and noise signals, which appear as common-mode voltages on the bus. EIA Standard RS-422 defines a differential interface that allows data rates up to 10 Mb/s (up to 40 feet) and line lengths up to 4000 feet (up to 100 kb/s). Line drivers designed to meet this standard are capable of transmitting a 2-V-minimum differential signal on a twisted-pair line terminated in 100 Ω. The receivers are capable of detecting ±200-mV differential signals in the presence of common-mode levels from −7 V to 7 V.

TABLE 1

SPECIFICATION		RS-232C	RS-423A	RS-422A	EIA Committee TR30.1 Draft Standard PN1360
Mode of operation		Single-ended	Single-ended	Differential	Differential
Number of drivers and receivers allowed on one line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers
Maximum cable length		50 feet	4000 feet	4000 feet	4000 feet
Maximum data rate		20 kb/s	100 kb/s	10 Mb/s	10 mb/s
Maximum voltage applied to driver output		±25 V	±6 V	−0.25 V to 6 V	−7 V to 12 V
Driver output signal	Loaded	±5 V	±3.6 V	±2 V	±1.5 V
	Unloaded	±15 V	±6 V	±5 V	±5 V
Driver load		3 kΩ to 7 kΩ	450 Ω min	100 Ω	54 Ω
Maximum driver output current (High-impedance state)	Power on	—	—	—	±100 μA
	Power off	V_{max}/300 Ω	±100 μA	±100 μA	±100 μA
Output slew rate		30 V/μs max	Controls provided	—	—
Receiver input voltage range		±15 V	±12 V	−7 V to 7 V	−7 V to 12 V
Receiver input sensitivity		±3 V	±200 mV	±200 mV	±200 mV
Receiver input resistance		3 kΩ to 7 kΩ	4 kΩ min	4 kΩ min	12 kΩ min

The main limitations of RS-422 occur in systems where output drivers of several components or subassemblies are connected to the same bus line. Ideally, only one driver on a line should be active (high or low) at a time, and all the others should be in a high-impedance state that prevents loading the line even when subassembly power is off. RS-422 does not require that drivers be in a high-impedance state except when the power supply is off, and then only for common-mode bus voltages from –0.25 volts to 6 volts. In systems where large positive and negative common-mode signals can appear on the bus, it is necessary that driver outputs maintain a high impedance over a wide range of common-mode voltage when disabled with power on or when power is off.

Another limitation of RS-422 occurs when more than one driver is enabled. The outputs may be in contention (trying to drive the bus to opposite logic states) or there may be a large difference in common-mode voltages. In either case, relatively large currents can cause excessive power dissipation and possible damage.

EIA Committee TR30.1 is, at the time of this publication, drafting a new standard (Project Number 1360) patterned after RS-422 (See Figure 1) but specified for multipoint interface. It is intended to allow for as many as 32 driver-receiver pairs on a data bus otherwise very similar to that of RS-422. Key features of the new standard are:

- Up to 32 Components Interfaced to One Bus
- Extended Common-Mode Voltage Range with Power On or Off
- Contention Protection for Drivers
- Receiver Sensitivity of ±200 millivolts
- Receiver Input Impedance Increased to 12 kΩ Min

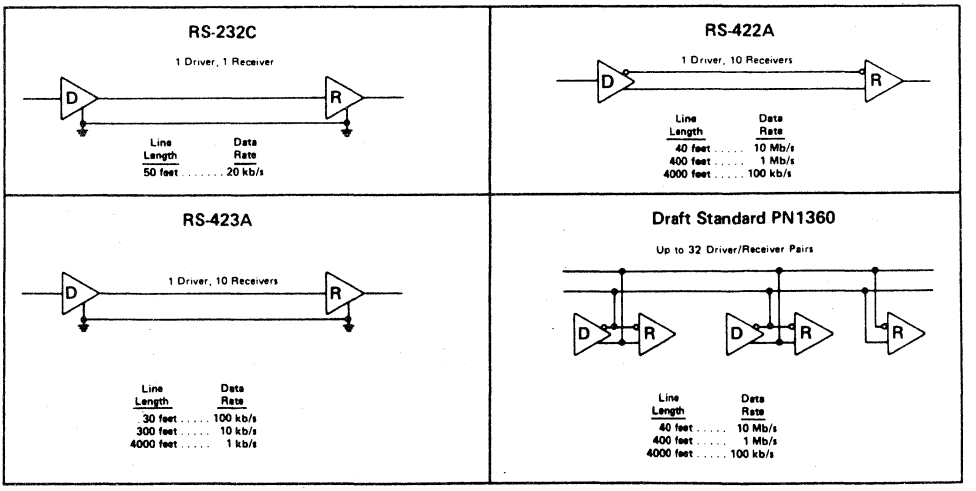


FIGURE 1

The new SN75172 and SN75174 drivers, and SN75173 and SN75175 receivers are available now for systems designed around either RS-422 or present PN1360 requirements. The drivers operate from a single 5-V supply and maintain high output impedance with power on or off. This improved design was achieved without appreciable sacrifice in speed, since they have maximum delay times of 50 ns and rise and fall times of 80 ns, and the data rate can be as high as 4 Mb/s. Also featured is the low maximum power requirement of 79 mW per enabled channel and 53 mW per disabled channel. These drivers provide contention protection through positive- and negative-current limiting and thermal shutdown. Each output is limited to −250 mA sink current and to 500 mA source current over the maximum output voltage range of −7 V to 12 V, and a thermal sensing circuit will cause these devices to go into a disabled state whenever the internal temperature exceeds approximately 150°C.

The SN75173 and SN75175 quadruple receivers are similar to existing RS-422 receivers but have higher input impedance and extended common-mode range without any sacrifice in sensitivity or speed. They feature ±200 mV sensitivity over a common-mode input range of ±12 V, 12 kΩ input impedance, and 35 ns propagation delay. Each receiver has 50 mV input hysteresis for increased noise margin.

Other new devices include the SN75176 transceiver, the equivalent of one SN75172 driver and one SN75173 receiver interconnected (see Figure 2) in a single 8-pin package. The SN75177 and SN75178 transceivers are designed for use as repeaters to extend the maximum cable distance. The enable controls on all these devices are complementary to allow bidirectional data communication.

Figure 1 illustrates how several of these new devices might be combined in a typical bus system. The SN75177 and SN75178 are connected to form a bidirectional repeater to extend the cable length. Other devices interface with terminals or MODEMs and drive peripherals. The twisted-pair line should normally be terminated at each end of the main wire lengths in 120-Ω resistors.

Texas Instruments manufactures a wide variety of integrated circuits designed to meet the requirements of EIA Standards RS-232C, RS-422A, RS-423A, and draft standard PN1360. This variety offers flexibility, choice, and compatibility that will provide cost-effective solutions to many interfacing problems.

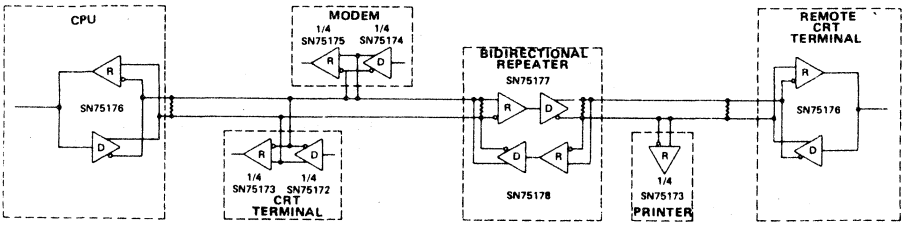


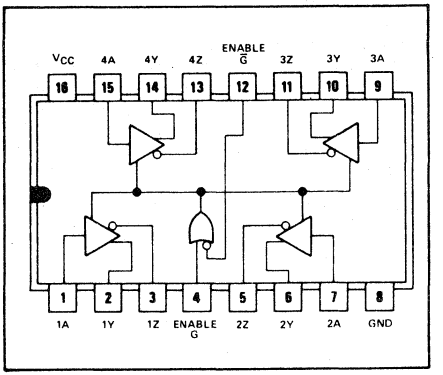
FIGURE 2

TYPES AM26LS31M, AM26LS31C
QUADRUPLE DIFFERENTIAL LINE DRIVERS

BULLETIN NO. DL-S 12671, JANUARY 1979 – REVISED SEPTEMBER 1980

- Meets EIA Standard RS-422A
- Operates from a Single 5-V Supply
- TTL-, DTL-Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output Enable Inputs

AM26LS31M . . . J
AM26LS31C . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The AM26LS31M and AM26LS31C are quadruple complementary-output line drivers designed to meet the requirements of EIA Standard RS-422 and Federal Standard 1020. The three-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers a choice of active-high or active-low inputs. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

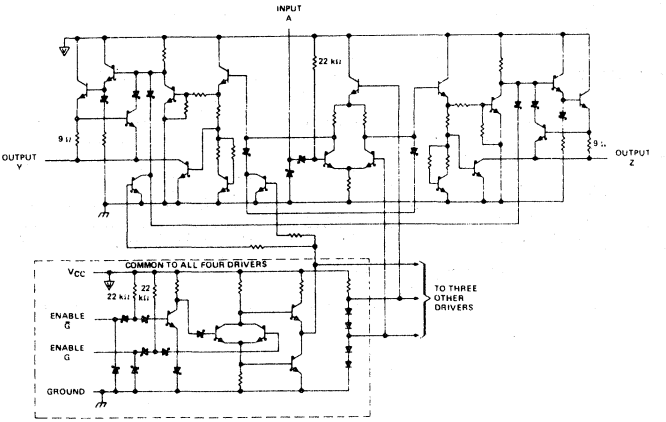
The AM26LS31M is characterized for operation over the full military temperature range of −55°C to 125°C, the AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1 W
Operating free-air temperature range: AM26LS31M . . . . . −55°C to 125°C
AM26LS31C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, AM26LS31M chips are alloy-mounted; AM26LS31C chips are glass-mounted.

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DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	AM26LS31M			AM26LS31C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−20			−20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

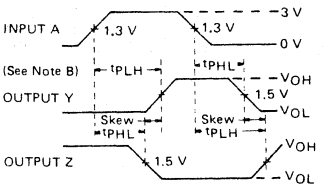
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = −20 mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20 mA			0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX,	All outputs disabled		32	80	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

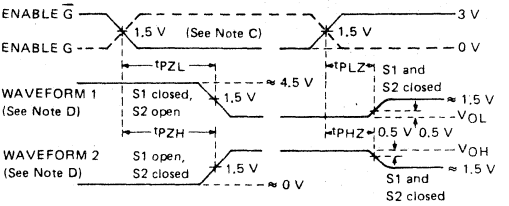
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1, S1 and S2 open		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			14	20	ns
	Output-to-output skew			1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 75 Ω, See Figure 1		25	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 180 Ω, See Figure 1		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, See Figure 1, S1 and S2 closed		21	30	ns
t_{PLZ}	Output disable time from low level			23	35	ns

PARAMETER MEASUREMENT INFORMATION

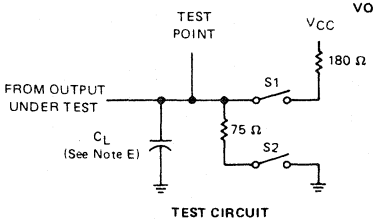


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

B. When measuring propagation delay times and skew, switches S1 and S2 are open.

C. Each enable is tested separately.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS†

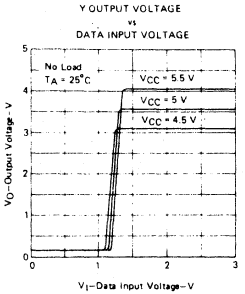


FIGURE 2

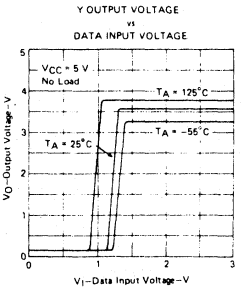


FIGURE 3

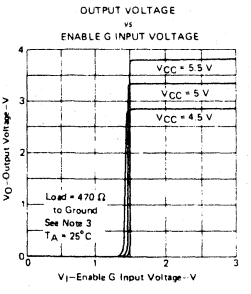


FIGURE 4

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

†Data for temperatures below 0°C and above 70°C are applicable to AM26LS31M circuits only.

TYPICAL CHARACTERISTICS†

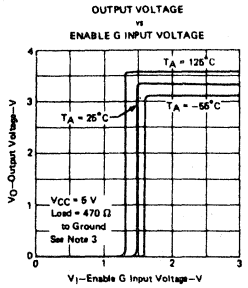


FIGURE 5

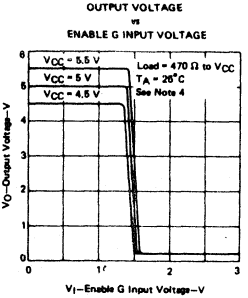


FIGURE 6

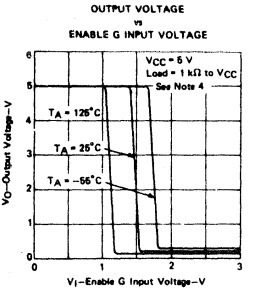


FIGURE 7

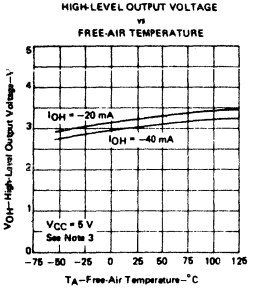


FIGURE 8

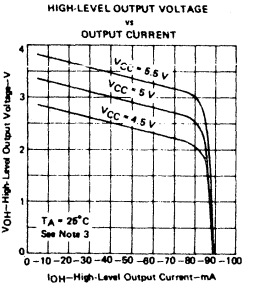


FIGURE 9

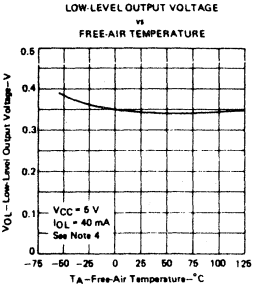


FIGURE 10

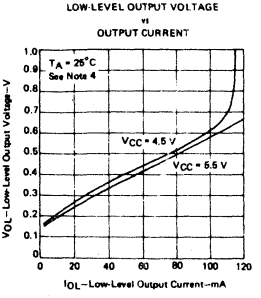


FIGURE 11

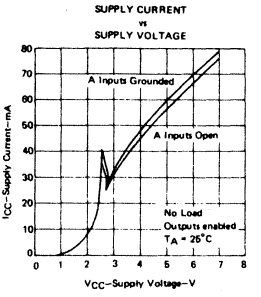


FIGURE 12

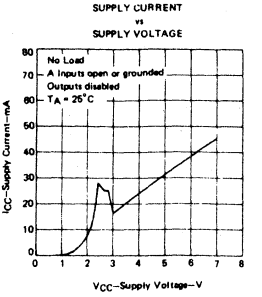


FIGURE 13

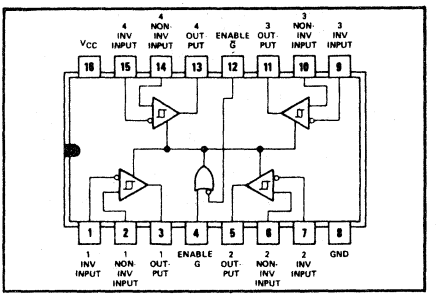
NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.
†Data for temperature below 0°C and above 70°C are applicable to AM26LS31M circuits only.

TYPES AM26LS32AC, AM26LS33AC
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

BULLETIN NO. DL-S 12655, OCTOBER 1980

- AM26LS32AC Meets EIA Standards RS-422A and RS-423A
- AM26LS32AC has ±7-V Common-Mode Range with ±200-mV Sensitivity
- AM26LS33AC has ±15-V Common-Mode Range with ±500 mV Sensitivity
- Input Hysteresis . . . 50 mV Typical
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- Complementary Output Enable Inputs
- Input Impedance . . . 12 kΩ Min
- Designed to be Interchangeable with Advanced Micro Devices AM26LS32C and AM26LS33C

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

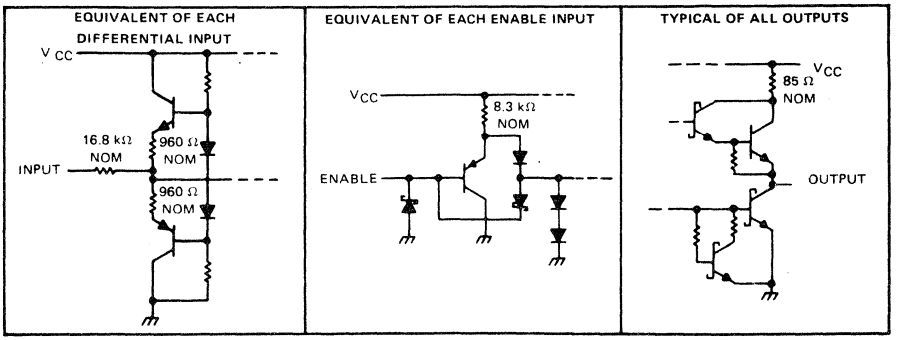
description

The AM26LS32AC and AM26LS33AC are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Compared to the AM26LS32C and the AM26LS33C, the AM26LS32AC and AM26LS33AC incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and the AM26LS33AC are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package the chips are glass-mounted.

5

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	AM26LS32AC			AM26LS33AC			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±15	V
High-level output current, I_{OH}			−440			−440	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	0		70	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	V_{OH} = 2.7 V,	I_{OH} = −440 μA	AM26LS32AC			0.2	V
				AM26LS33AC			0.5	
V_{TL}	Differential input low-threshold voltage	V_{OL} = 0.45 V,	I_{OL} = 8 mA	AM26LS32AC	−0.2‡			V
				AM26LS33AC	−0.5‡			
$V_{T+} - V_{T-}$	Hysteresis§					50		mV
V_{IH}	High-level enable input voltage				2			V
V_{IL}	Low-level enable input voltage						0.8	V
V_{IK}	Enable input clamp voltage	V_{CC} = 4.75 V,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, $V_{I(\overline{G})}$ = 0.8 V,	V_{ID} = 1 V, I_{OH} = −440 μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, $V_{I(\overline{G})}$ = 0.8 V	V_{ID} = −1 V,	I_{OL} = 4 mA			0.4	V
				I_{OL} = 8 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = 5.25 V,		V_O = 2.4 V			20	μA
				V_O = 0.4 V			−20	
I_I	Line input current	V_I = 15 V,	Other input at −10 V to 15 V				1.2	mA
		V_I = −15 V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V					100	μA
I_{IH}	High-level enable current	V_I = 2.7 V					20	μA
I_{IL}	Low-level enable current	V_I = 0.4 V					−0.36	mA
r_i	Input resistance	V_{IC} = −15 V to 15 V,	One input to AC ground		12	15		kΩ
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,			−15		−85	mA
I_{CC}	Supply current	V_{CC} = 5.25 V, All outputs disabled	Data inputs at 0 V,			52	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25° C, and V_{IC} = 0.

‡ The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

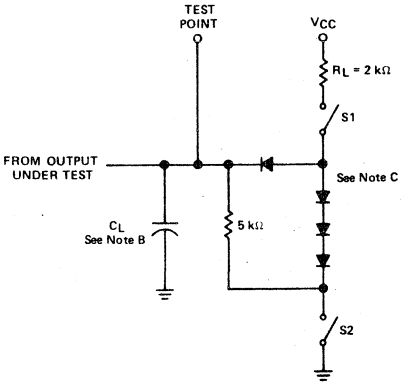
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figures 10 and 11.

¶ Not more than one output should be shorted at a time.

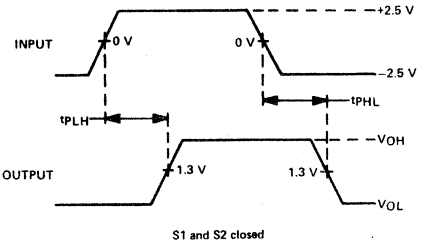
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level				20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level				30	40	ns

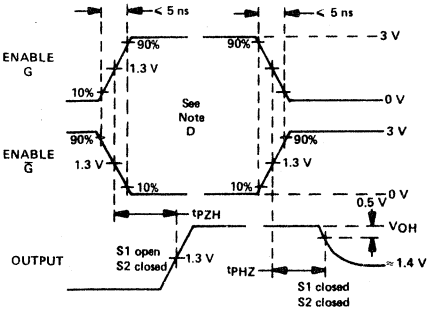
PARAMETER MEASUREMENT INFORMATION



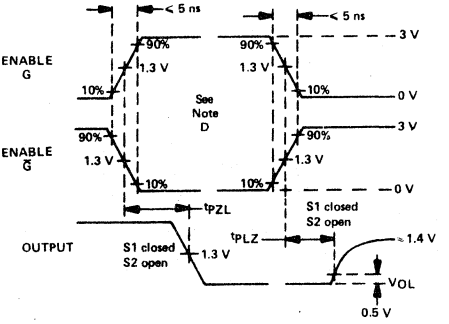
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. The pulse generator has the following characteristics:
Z_{out} = 50 Ω, PRR = 1 MHz, t_w = 0.5 μs.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Enable G is tested with $\overline{G}$ high, $\overline{G}$ is tested with G low.

FIGURE 1

TYPICAL CHARACTERISTICS

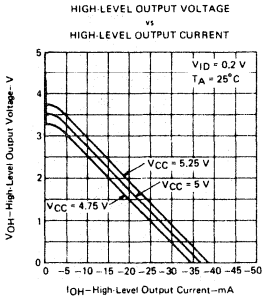


FIGURE 2

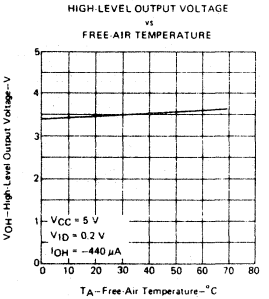


FIGURE 3

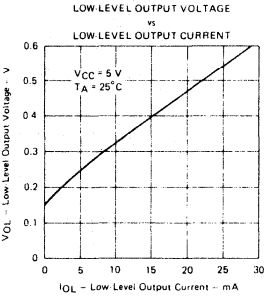


FIGURE 4

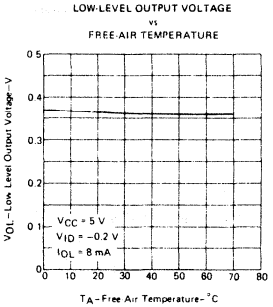


FIGURE 5

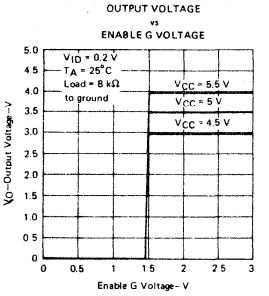


FIGURE 6

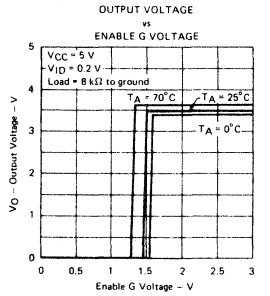


FIGURE 7

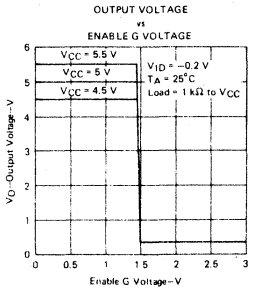


FIGURE 8

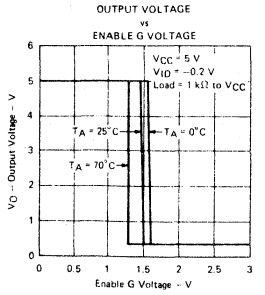


FIGURE 9

TYPICAL CHARACTERISTICS

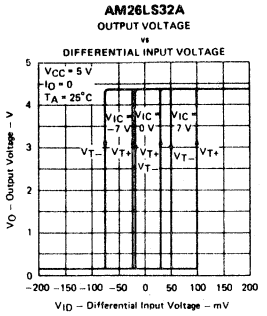


FIGURE 10

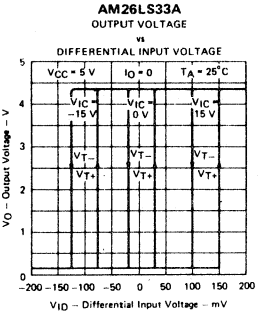


FIGURE 11

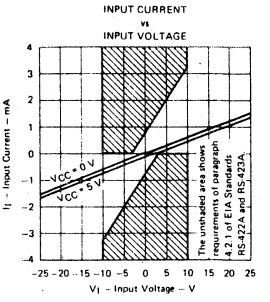
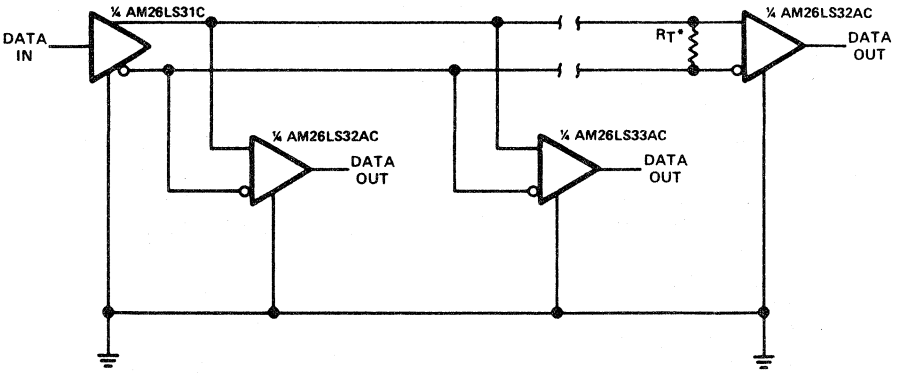


FIGURE 12

TYPICAL APPLICATION



*R_T equals the characteristic impedance of the line.

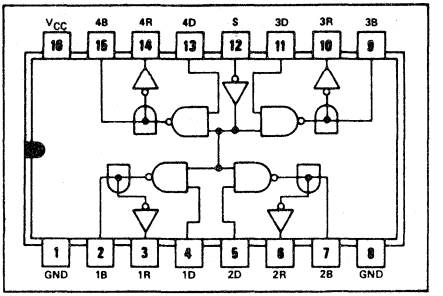
FIGURE 13 – CIRCUIT WITH MULTIPLE RECEIVERS

TYPES AM26S10M, AM26S10C, AM26S11M, AM26S11C QUADRUPLE BUS TRANSCEIVERS

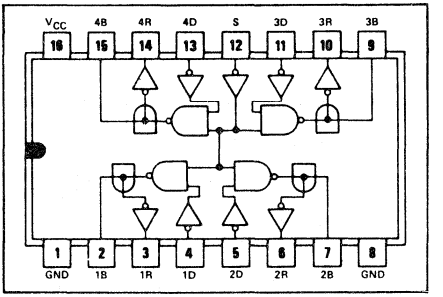
BULLETIN NO. DL-S 12498, JANUARY 1977 – REVISED SEPTEMBER 1980

- Schottky Circuitry† for High Speed, Typical Propagation Delay Time . . . 12 ns
- Drivers Feature Open-Collector Outputs for Party-Line (Data bus) Operation
- Driver Outputs Can Sink 100 mA at 0.8 V Maximum
- P-N-P Inputs for Minimal Input Loading
- Designed to be Interchangeable with Advanced Micro Devices AM26S10 and AM26S11

AM26S10
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



AM26S11
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The AM26S10 and AM26S11 are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use p-n-p transistors to reduce the input loading.

The driver of the AM26S10 is inverting; the driver of the AM26S11 is noninverting. Each device has two ground connections, for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10M and AM26S11M are characterized for operation over the full military temperature range of −55°C to 125°C. The AM26S10C and AM26S11C are characterized for operation over the temperature range of 0°C to 70°C.

AM26S10
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

AM26S11
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	H	L
L	L	L	H

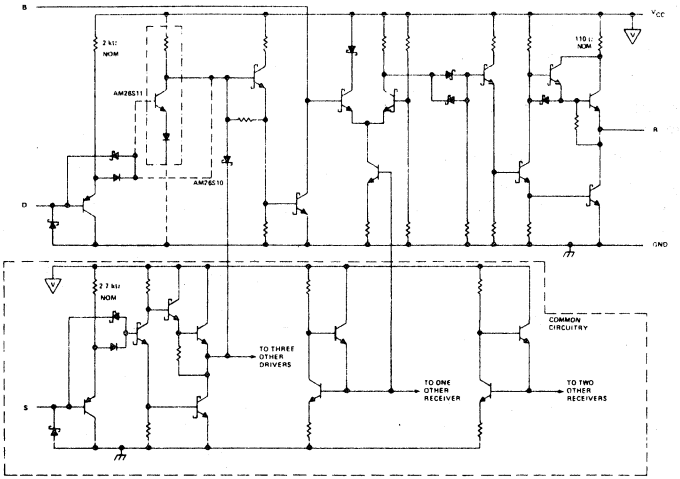
AM26S10 AND AM26S11
FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

schematic (each transceiver)



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	−0.5 V to 7 V
Driver or strobe input voltage	−0.5 V to 5.5 V
Bus voltage, driver output off: AM26S10M, AM26S11M	−0.5 V to 5.5 V
AM26S10C, AM26S11C	−0.5 V to 5.25 V
Driver or strobe input current	−30 mA to 5 mA
Driver output current	200 mA
Receiver output current	30 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range: AM26S10M, AM26S11M	−55°C to 125°C
AM26S11C, AM26S11C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminals connected together.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J package, AM26S10M and AM26S11M chips are alloy-mounted; AM26S10C and AM26S11C chips are glass-mounted.

recommended operating conditions

		AM26S10M AM26S11M			AM26S10C AM26S11C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Receiver high-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}	Driver			100			100	mA
	Receiver			20			20	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

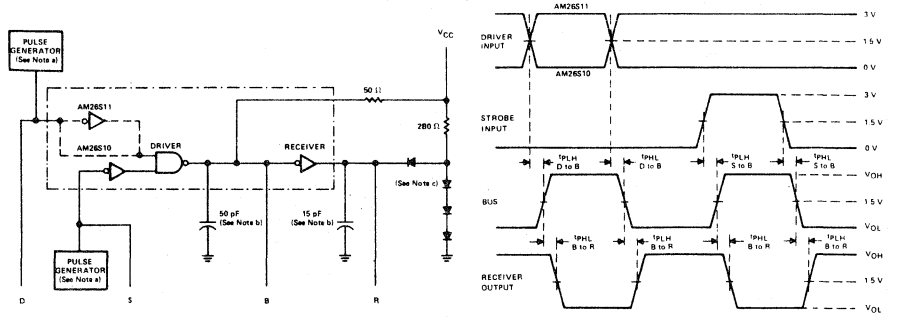
PARAMETER			TEST CONDITIONS†			AM26S10M AM26S11M MIN	AM26S10M AM26S11M TYP‡	AM26S10M AM26S11M MAX	AM26S10C AM26S11C MIN	AM26S10C AM26S11C TYP‡	AM26S10C AM26S11C MAX	UNIT
V_{IH}	High-level input voltage	D or S				2			2			V
		B				2.4			2.25			
V_{IL}	Low-level input voltage	D or S						0.8			0.8	V
		B						1.6			1.75	
V_{IK}	Input clamp voltage	D or S	V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −1 mA			2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	R	V_{CC} = MIN, V_{IH} = V_{IH} min, V_{IL} = 0.8 V		I_{OL} = 20 mA			0.5			0.5	V
		B			I_{OL} = 40 mA		0.33	0.5		0.33	0.5	
					I_{OL} = 70 mA		0.42	0.7		0.42	0.7	
					I_{OL} = 100 mA		0.51	0.8		0.51	0.8	
$I_{O(off)}$	Off-state output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = MAX,	V_O = 0.8 V			−50			−50	μA
				V_{CC} = MAX,	V_O = 4.5 V			200			100	
				V_{CC} = 0,	V_O = 4.5 V			100			100	
I_{IH}	High-level input current	D	V_{CC} = MAX, V_I = 2.7 V					30			30	μA
		S						20			20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = MAX, V_I = 5.5 V					100			100	μA
I_{IL}	Low-level input current	D	V_{CC} = MAX, V_I = 0.4 V					−0.54			−0.54	mA
		S						−0.36			−0.36	
I_{OS}	Short-circuit output current§	R	V_{CC} = MAX			−20		−55	−18		−60	mA
I_{CC}	Supply current	AM26S10	V_{CC} = MAX, Strobe at 0 V, No load,				45	70		45	70	mA
		AM26S11	All driver outputs low					80			80	

†For conditions shown as MIN or MAX, use the appropriate value shown under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	AM26S10 MIN	AM26S10 TYP	AM26S10 MAX	AM26S11 MIN	AM26S11 TYP	AM26S11 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15		12	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		12	19	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18		15	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18		14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: a. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 10 ± 5 ns.
b. Includes probe and jig capacitance.
c. All diodes are 1N916 or equivalent.

FIGURE 1

TYPICAL APPLICATION

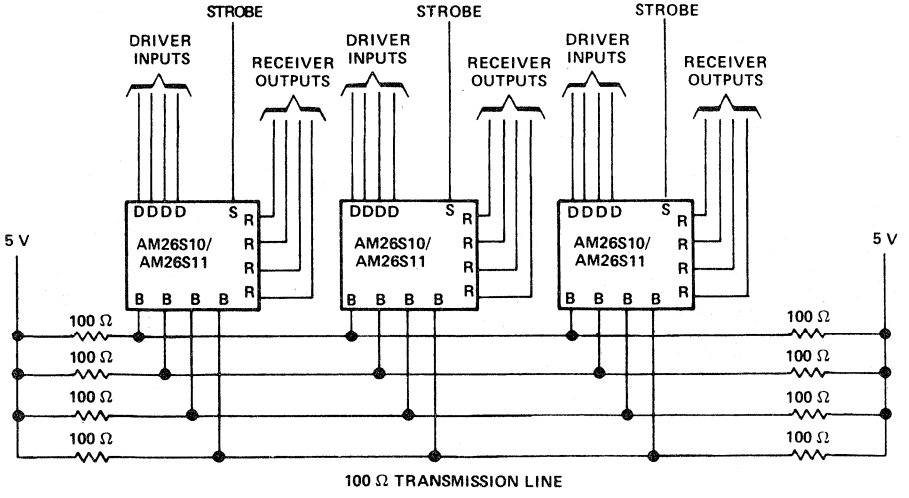


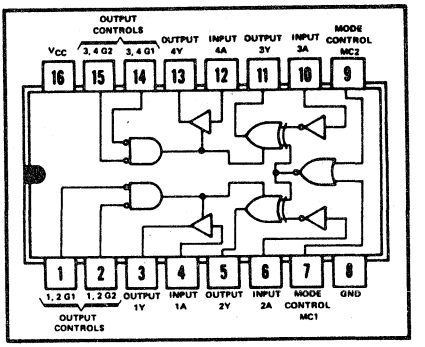
FIGURE 2–PARTY-LINE SYSTEM

TYPES DS7831, DS7832, DS8831, DS8832 LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12496, JANUARY 1977

- TTL Compatible
- Propagation Delay Time . . . 15 ns Typ
- Very Low Output Impedance with High Drive Capability
- 40-mA Sink and Source Capability
- Gating Control to Allow Either Single-Ended or Differential Operation
- Three-State Outputs for Party-Line (Data-Bus) Operation

DS7831, DS7832.....J PACKAGE
DS8831, DS8832.....J OR N PACKAGE
(TOP VIEW)



description

The DS7831, DS7832, DS8831, and DS8832 can be used as either guadruple single-ended line drivers or as dual differential line drivers. This multi-mode operation and simple logic control make these devices especially useful for party-line or bus-organized systems. The DS7831 and DS8831 have output clamp diodes to V_{CC}; the DS7832 and DS8832 do not.

For one of these circuits to operate as four independent single-ended line drivers, both mode-control pins must be low. In this mode, no signal inversion takes place between inputs and outputs. To operate as a dual differential line driver, at least one of the mode control inputs must be high. Inputs 1A and 2A should be connected together as should 3A and 4A. Then signals applied to the inputs will appear noninverted at 1Y and 4Y and inverted at 2Y and 3Y, provided the output control pins are low.

While enabled, these outputs provide good drive capability for capacitive loads, and fast transitions from both low-to-high levels and high-to-low levels.

Taking either of the associated output controls high disables the outputs. When disabled, these three-state outputs neither load nor drive a line and hundreds of these devices may be connected to a common bus line. Only one output should be enabled at a time.

The DS7831 and DS7832 are characterized for operation over the full military temperature range of −55°C to 125°C. The DS8831 and DS8832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OUTPUT CONTROLS		MODE CONTROLS		DATA INPUT	OUTPUT	DATA INPUT	OUTPUT
G1	G2	MC1	MC2	1A/4A	1Y/4Y	2A/3A	2Y/3Y
L	L	L	L	H	H	H	H
L	L	L	L	L	L	L	L
L	L	X	H	H	H	H	L
L	L	H	X	L	L	L	H
H	X	X	X	X	Z	X	Z
X	H	X	X	X	Z	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range: DS78' . . . . . −55°C to 125°C
DS88' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, DS7831 and DS7832 chips are alloy-mounted; DS8831 and DS8832 chips are glass-mounted.

recommended operating conditions

	DS78'			DS88'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_O			5.5			5.5	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −2 mA	DS7831,DS7832	2.4	3.1		V
			I_{OH} = −5.2 mA	DS8831,DS8832	2.4	3.0		
			I_{OH} = −40 mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 32 mA			0.26	0.4	V
			I_{OL} = 40 mA			0.3	0.5	
V_{OK}	Output clamp voltage	V_{CC} = 5 V, T_A = 25°C	I_O = −12 mA				−1.5	V
			I_O = 12 mA	DS7831,DS8831			V_{CC} + 1.5	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, T_A = 25°C	V_O = 2.4 V				40	μA
			V_O = 0.4 V				−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = MAX	−40	−70	−120	mA
I_{CC}	Supply current	V_{CC} = MAX				50	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Only one output should be shorted at a time.

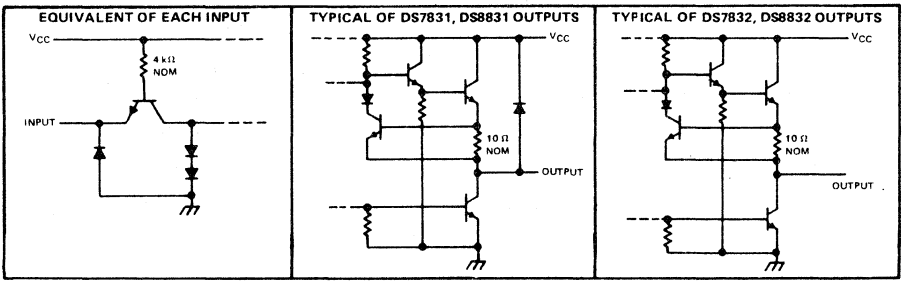
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	2A or 3A	2Y or 3Y (noninverting)	Mode controls low, See Figure 11		10	25	ns
t_{PHL}					12	25	
t_{PLH}	2A or 3A	2Y or 3Y (inverting)	Mode controls high, See Figure 11		12	25	ns
t_{PHL}					15	25	
t_{PLH}	1A or 4A	1Y or 4Y	See Figure 11		9	25	ns
t_{PHL}					11	25	
t_{PZH}	G1 or G2	Any Y	C_L = 50 pF, See Figure 13		12	22	ns
t_{PZL}					14	27	
t_{PHZ}	G1 or G2	Any Y	C_L = 5 pF, See Figure 13		6	12	ns
t_{PLZ}					15	22	

¶ t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

5

schematics of inputs and outputs



TYPICAL CHARACTERISTICS

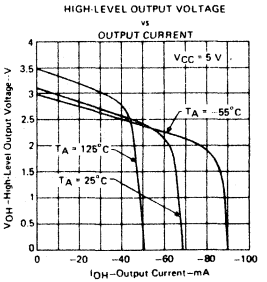


FIGURE 1

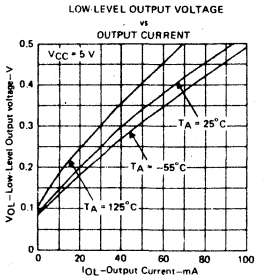


FIGURE 2

TYPICAL CHARACTERISTICS†

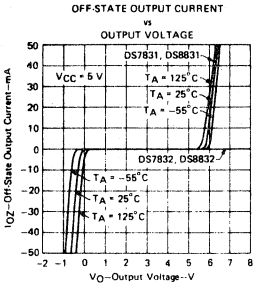


FIGURE 3

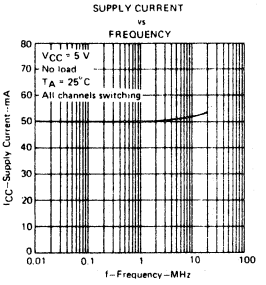


FIGURE 4

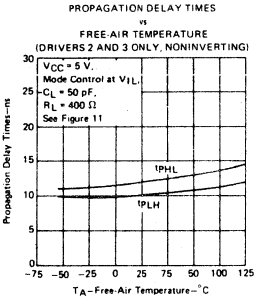


FIGURE 5

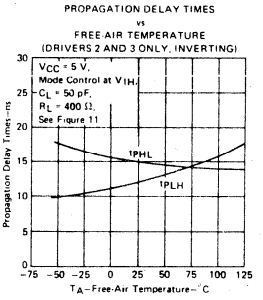


FIGURE 6

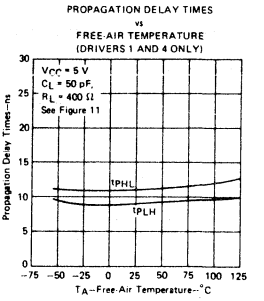


FIGURE 7

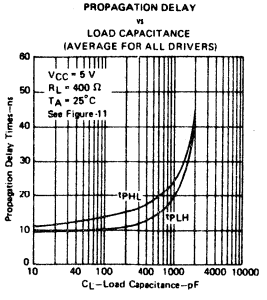


FIGURE 8

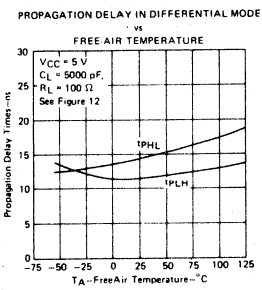


FIGURE 9

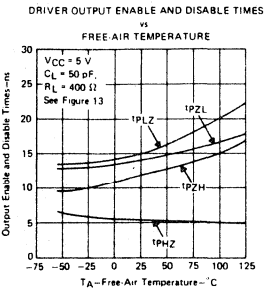
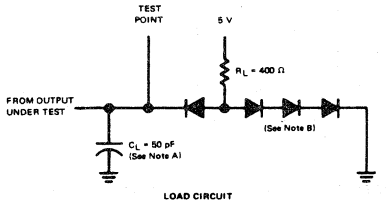
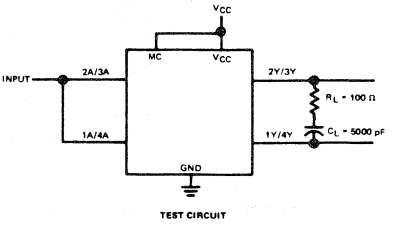


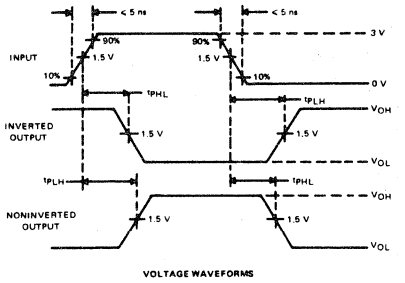
FIGURE 10

† Data for free-air temperature below 0°C and above 70°C are applicable to DS7831 and DS7832 circuits only.

PARAMETER MEASUREMENT INFORMATION







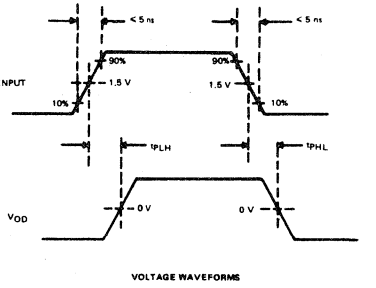
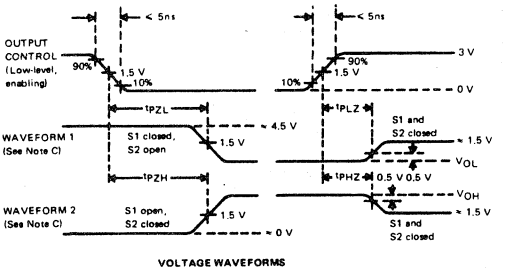


FIGURE 11– t_{PLH} and t_{PHL}, SINGLE-ENDED MODE

FIGURE 12–t_{PLH} and t_{PHL}, DIFFERENTIAL MODE



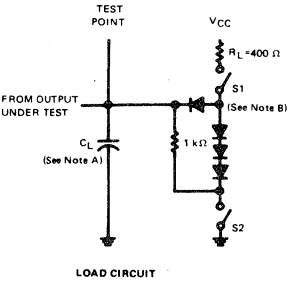


FIGURE 13–ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

TYPICAL APPLICATION DATA

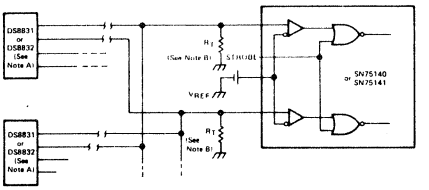


FIGURE 14—PARTY-LINE OPERATION UTILIZING THE SINGLE-ENDED CAPABILITY OF THE DEVICE

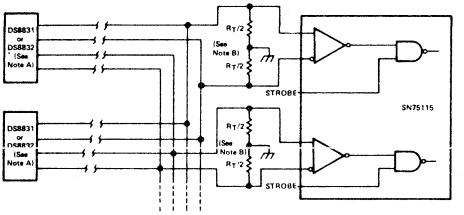


FIGURE 15—PARTY-LINE OPERATION UTILIZING THE DIFFERENTIAL CAPABILITY OF THE DEVICE

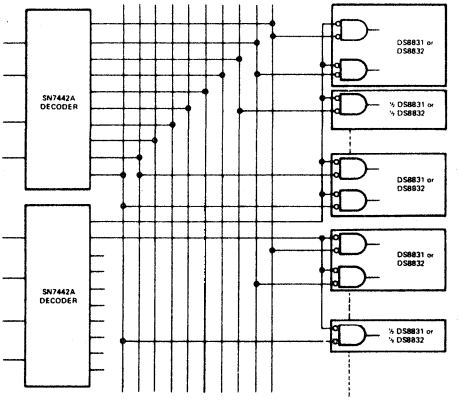


FIGURE 16—USING TWO 4-LINE-TO-10-LINE DECODERS TO CONTROL 100 DRIVER OUTPUTS

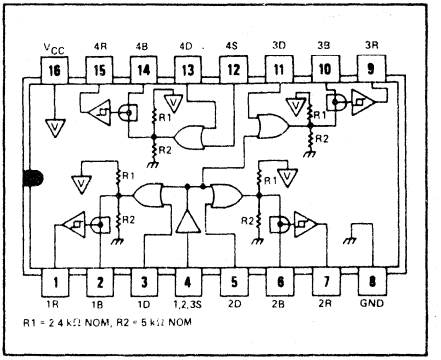
NOTES: A. One device may be driving onto the bus lines, and all other devices should be in the high-impedance state.
B. The value of R_T should be approximately equal to the characteristic impedance of the transmission line.

TYPE MC3446
QUADRUPLE BUS TRANSCEIVER

BULLETIN NO. DL-S 12492, JANUARY 1977 – REVISED AUGUST 1977

- Driver Inputs Compatible with TTL and MOS Circuitry
- Driver Outputs Stay Off During Power Up and Power Down
- Drivers Feature Open-Collector Outputs for Party-Line Operation
- Designed for Interchangeability with Motorola MC3446
- Meets IEEE Standard 488-1975

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These circuits are quadruple, single-ended line transceivers designed for bidirectional flow of data and instructions. The bus terminal characteristic complies with paragraph 3.5.3 of IEEE Standard 488 (see Figure 3). Each driver output is tied to the junction of an internal voltage divider that sets the no-load output voltage and provides bus termination. The driver outputs are guaranteed to be "off" during power up and power down if either input is high. The receivers feature 950 millivolts typical hysteresis for noise immunity.

The MC3446 is characterized for operation from 0°C to 70°C.

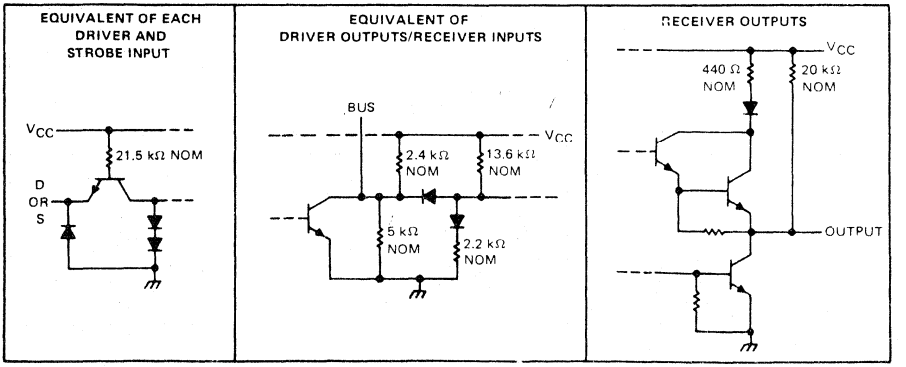
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUT	
S	D	B	R
L	H	H	H
L	L	L	L

FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	H
H	L	X	L

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Driver output current . . . . . 150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 830 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, MC3446 chips are glass-mounted

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Receiver			−0.4	mA
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	D or S		2			V
V_{IL}	Low-level input voltage	D or S				0.8	V
V_{IK}	Input clamp voltage	D or S	I_I = −12 mA			−1.5	V
V_{T+}	Positive-going input threshold voltage	B		1.5	1.8	2	V
V_{T-}	Negative-going input threshold voltage	B		0.6	0.85	1.1	V
$V_{T+} - V_{T-}$	Input hysteresis	B		400	950		mV
V_{OH}	High-level output voltage	B	V_{IH} = 2.4 V, I_{OH} = 0	2.5	3.3	3.7	V
		R	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			
V_{OL}	Low-level output voltage	B	V_{IL} = 0.8 V, I_{OL} = 48 mA			0.4	V
		R	V_{IL} = 0.8 V, I_{OL} = 8 mA			0.4	
$I_{O(bus)}$	Bus current	B	V_{IH} = 2.4 V, V_O = 5.5 V			2.5	mA
			V_{IH} = 2.4 V, V_O = 5 V	0.7			
			V_{IH} = 2.4 V, V_O = 0.4 V	−1.3		−3.2	
V_{OK}	Output clamp voltage	B	I_O = −12 mA			−1.5	V
I_I	Input current at maximum input voltage	D or S	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	D or S	V_{IH} = 2.4 V		5	20	μA
I_{IL}	Low-level input current	D or S	V_{CC} = 5 V, V_{IL} = 0.4 V, T_A = 25°C		0.2	0.36	mA
I_{OS}	Short-circuit output current	R	V_{IH} = 2 V	4		14	mA
I_{CCH}	Supply current, all outputs high		No load		10	19	mA
I_{CCL}	Supply current, all outputs low		No load		32	39	mA

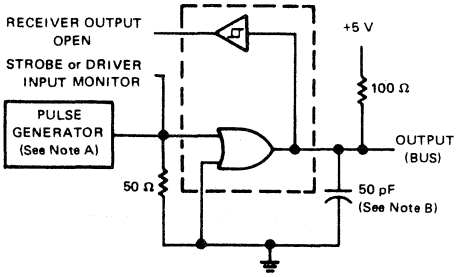
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

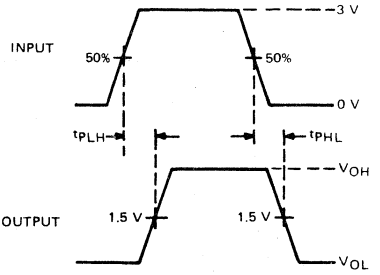
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					50	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output					50	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	See Figure 2		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output					40	

5

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

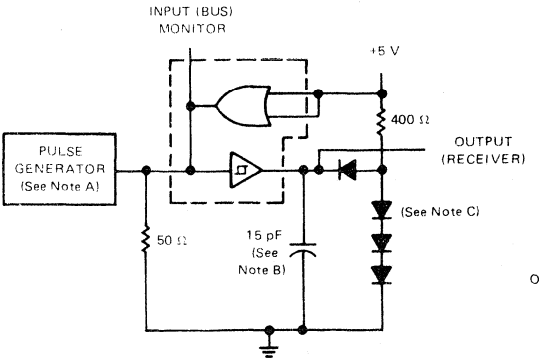


VOLTAGE WAVEFORMS

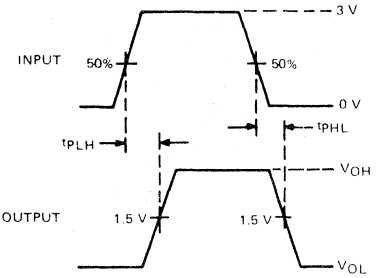
NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 100 ns, PRR = 1 MHz, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_{out} \approx 50\ \Omega$.
B. This value includes probe and jig capacitance.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 100 ns, PRR = 1 MHz, $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_{out} = 50 Ω.
B. This value includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 2

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CHARACTERISTICS†

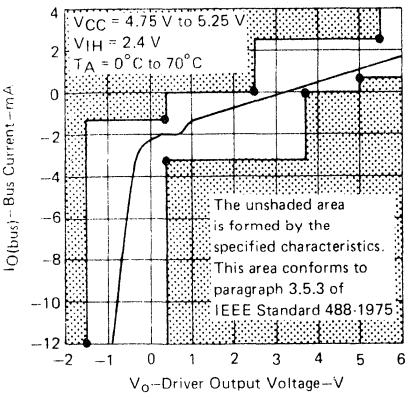


FIGURE 3

†Conditions for typical curve are V_{CC} = 5 V, T_A = 25°C.

RECEIVER TRANSFER CHARACTERISTICS

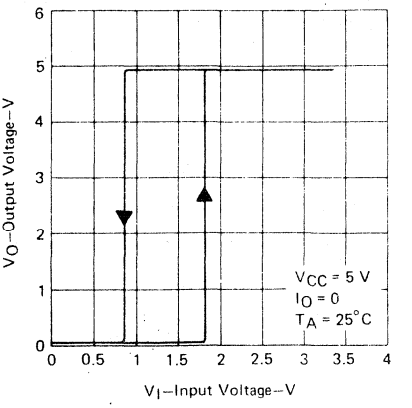


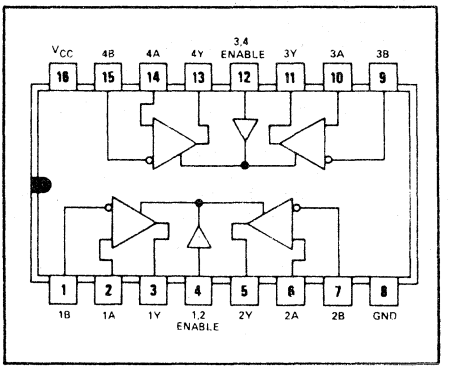
FIGURE 4

TYPE MC3486
QUADRUPLE LINE RECEIVER WITH 3-STATE OUTPUT

BULLETIN NO. DL-S 12748, JUNE 1980

- Meets EIA Standards RS-422A and RS-423A and Federal Standards 1020 and 1030
- Three-State, TTL-Compatible Outputs
- Fast Transition Times
- Operates From Single 5-Volt Supply
- Designed to be Interchangeable with Motorola MC3486

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of EIA Standards RS-422A and RS-423A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize three-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-volt supply.

The MC3486 is characterized for operation from 0°C to 70°C.

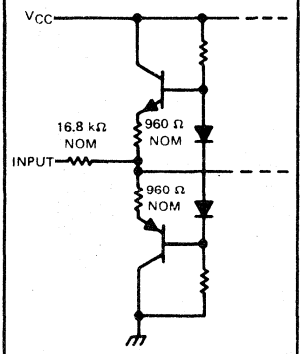
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z

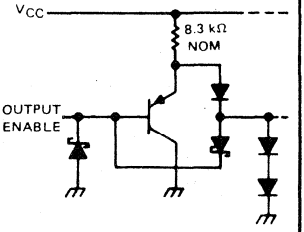
H = high level, L = low level, Z = high-impedance (off),
? = indeterminate

schematics of inputs and outputs

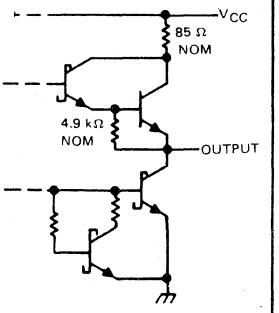
EQUIVALENT OF EACH INPUT EXCEPT OUTPUT ENABLE



EQUIVALENT OF OUTPUT ENABLE



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Input voltage, A or B inputs	±15 V
Differential input voltage (see Note 2)	±25 V
Enable input voltage	8 V
Low-level output current	50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package	1025 mW
N Package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package	260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			+7	V
Differential input voltage, V_{ID}			±6	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA			−0.2†		V
V_{IH}	High-level enable input voltage				2		V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID}* = 0.4 V, I_O = −0.4 mA, See Note 4 and Figure 1			2.7		V
V_{OL}	Low-level output voltage	V_{ID}* = −0.4 V, I_O = 8 mA, See Note 4 and Figure 1				0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = −3 V,		V_O = 2.7 V		40	μA
		V_{IL} = 0.8 V, V_{ID} = 3 V,		V_O = 0.5 V		−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V		V_I = −10 V		−3.25	mA
				V_I = −3 V		−1.5	
				V_I = 3 V		1.5	
				V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V				100	μA
		V_I = 2.7 V				20	
I_{IL}	Low-level enable input current	V_I = 0.5 V				−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V,	V_O = 0 V,	See Note 5	−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0 V				85	mA

†The algebraic convention, where the least-positive (most-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. Refer to EIA Standards RS-422A and RS-423A for exact conditions.
5. Only one output at a time should be shorted.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, see Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			27	30	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, see Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

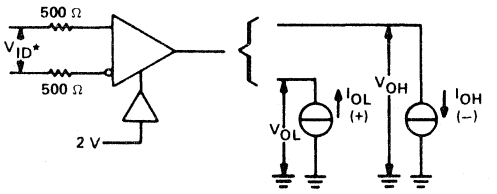
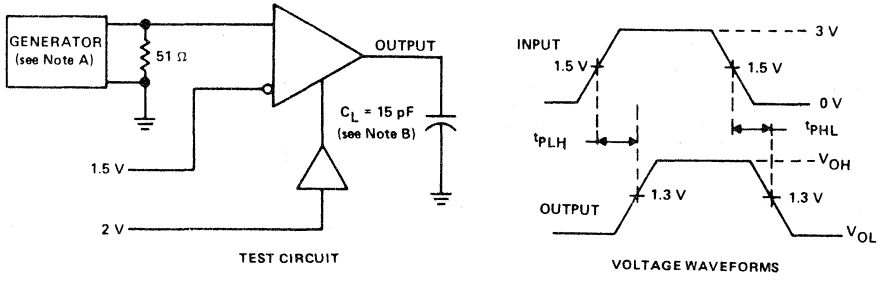


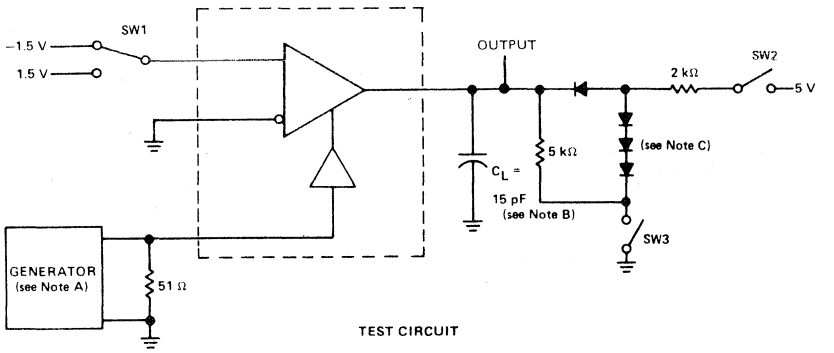
FIGURE 1–V_{OH}, V_{OL}



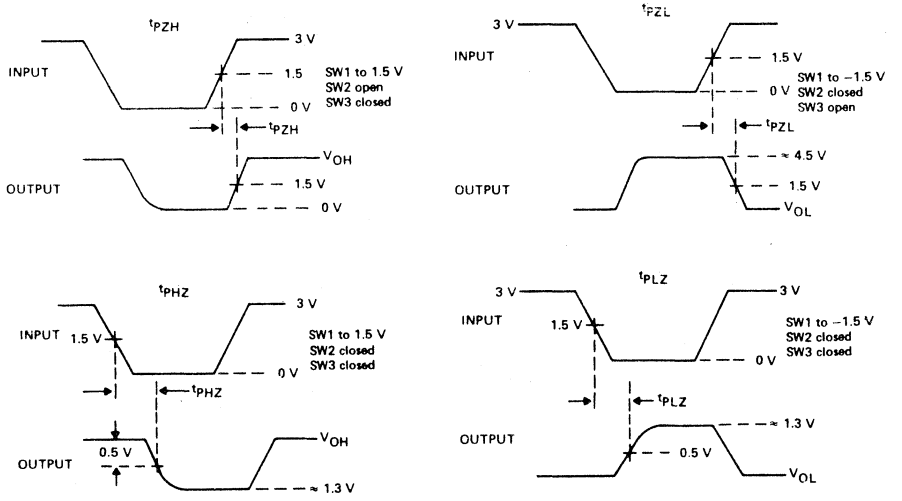
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns.
B. C_L includes probe and stray capacitance.

FIGURE 2–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3–ENABLE AND DISABLE TIMES

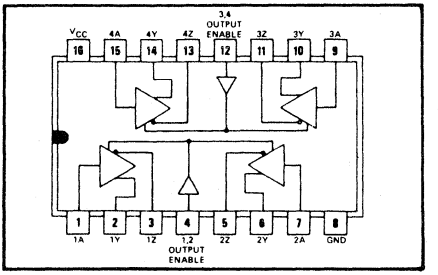
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f$ = 6 ns.
B. C_L includes probe and stray capacitance
C. All diodes are 1N916 or equivalent.

TYPE MC3487
QUADRUPLE DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12749, MAY 1980

- Meets EIA Standard RS-422A and Federal Standard 1020
- Three-State, TTL-Compatible Outputs
- Fast Transition Times
- High-Impedance Inputs
- Single 5-Volt Supply
- Power-Up and Power-Down Protection
- Designed To Be Interchangeable with Motorola MC3487

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a logic low level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 milliamperes.

FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

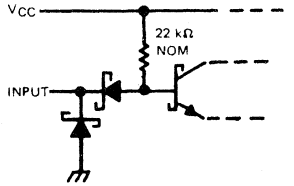
H = TTL high level X = irrelevant
L = TTL low level

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-volt supply.

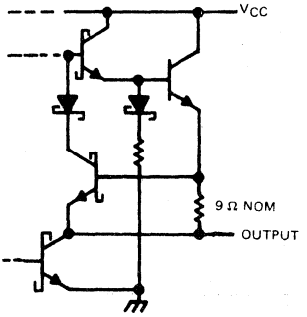
The MC3487 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IH}	High-level input voltage				2		V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V	I_{OH} = −20 mA	2.5		V
				I_{OH} = −48 mA	2		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			± 0.4	V
I_O	Output current with power off	V_{CC} = 0 V	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	μA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	μA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Inputs grounded,	No load			105	mA
		Output enables at 2 V				85	

†$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				20	ns
	Skew				6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF,	See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF,	See Figure 4		30	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				25	ns
t_{PLZ}	Output disable time from low level				25	ns

PARAMETER MEASUREMENT INFORMATION

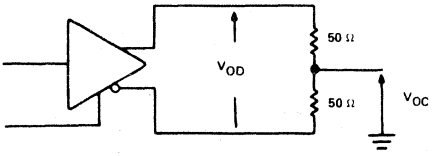
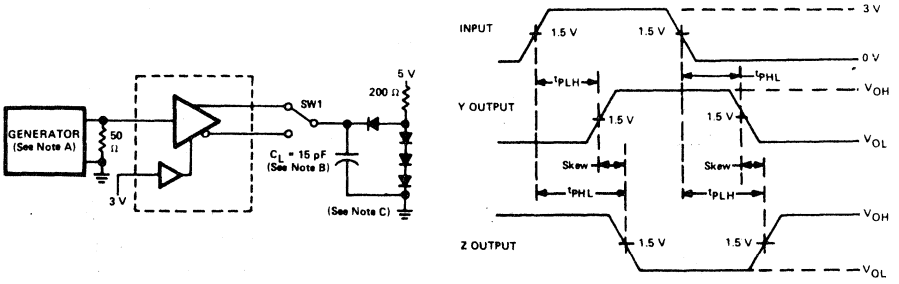


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

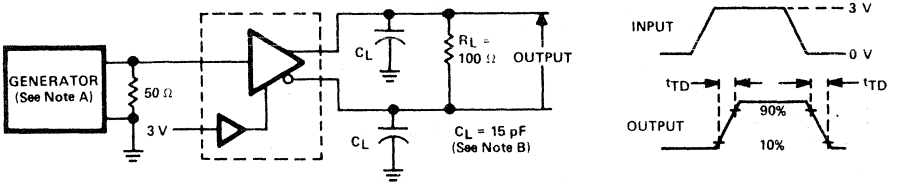


TEST CIRCUIT VOLTAGE WAVEFORM

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 5 ns, t_f ≤ 5 ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 2–PROPAGATION DELAY TIMES

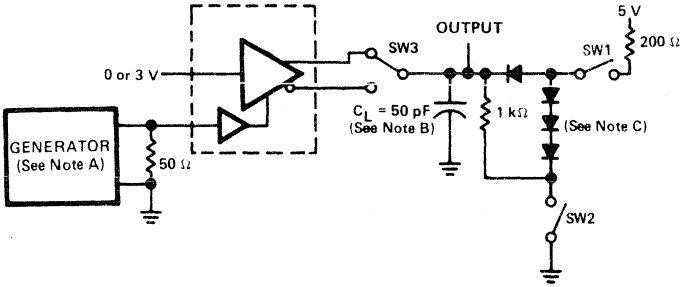
PARAMETER MEASUREMENT INFORMATION



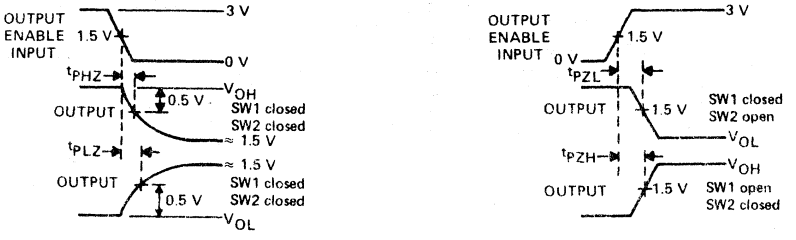
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–DIFFERENTIAL-OUTPUT TRANSITION TIMES

5



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_o = 50\ \Omega$.

B. C_L includes probe and stray capacitance.

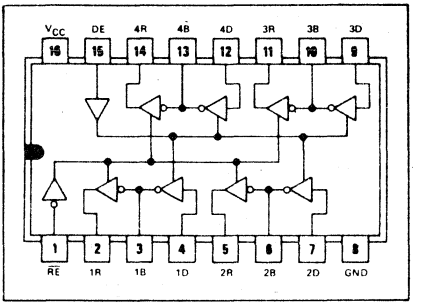
C. All diodes are 1N916 or 1N3064.

TYPES N8T26, N8T26A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12617, MAY 1978 – REVISED JULY 1980

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry†
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- N8T26A Driver has 48-mA Current Sink Capability
- Designed to be Interchangeable with Signetics N8T26 and N8T26A, also Called 8T26 and 8T26A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

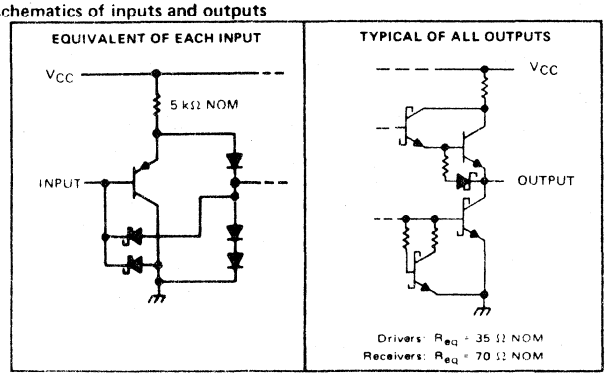


description

The N8T26 and N8T26A are quadruple transceivers utilizing Schottky-diode-clamped transistors. Both the driver and receiver have three-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of 200 microamperes. These devices are capable of high switching rates into high-capacitance loads and are suitable for driving long bus lines.

The N8T26 and N8T26A are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE (DRIVER)

INPUT		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

FUNCTION TABLE (RECEIVER)

INPUT		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

H = high level, L = low level
X = irrelevant, Z = high impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

†Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

N8T26 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			40	mA
	Receiver, R			16	
Operating free-air temperature, T_A		0		70	°C

N8T26 electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$				2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$						0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −5 mA					−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V	I_{OH} = −2 mA		2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V,	I_{OL} = 40 mA				0.5	V
		R	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V	$\overline{RE}$ at 2 V,	V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V,	V_O = 0.5 V				−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V					25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V					−200	μA
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V			−50		−150	mA
		R				−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V,	No load				87	mA

N8T26 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	10	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		9	17	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		20	43	ns
t_{PZL}	Output enable time to low level					20	38	

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

N8T26A recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			48	mA
	Receiver, R			20	
Operating free-air temperature, T_A		0		70	°C

N8T26A electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

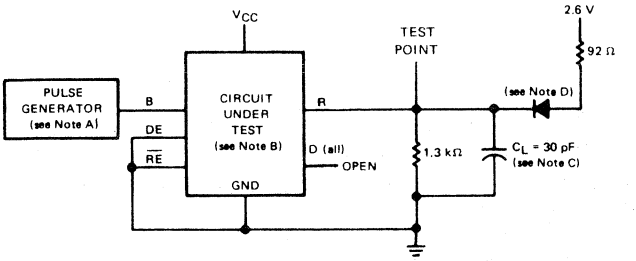
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$				2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$						0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −12 mA					−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V	I_{OH} = −2 mA		2.6	3.1		
			V_{IL} = 0.85 V	I_{OH} = −100 μA		3.5			
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V,	I_{OL} = 48 mA				0.5	V
		R	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OL} = 20 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V	$\overline{RE}$ at 2 V,	V_O = 2.6 V			100	μA
		B, R	DE at 0.85 V,	$\overline{RE}$ at 2 V,	V_O = 0.5 V			−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V					25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V					−200	μA
		D	V_I = 0.4 V,	DE at 0.85 V				−25	
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V			−50		−150	mA
		R				−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V,	No load				87	mA

N8T26A switching characteristics, V_{CC} = 5 V, T_A = 25°C

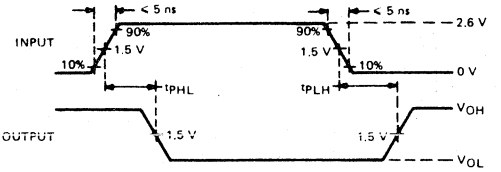
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		12	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	14	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		7	15	ns
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		14	20	ns
t_{PZL}	Output enable time to low level					17	25	

† All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

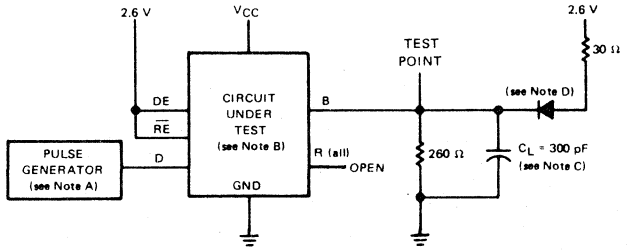


TEST CIRCUIT

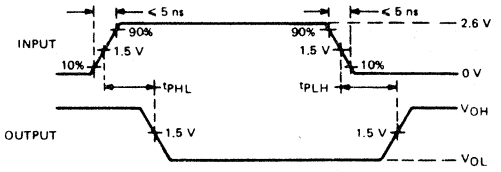


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT



TEST CIRCUIT

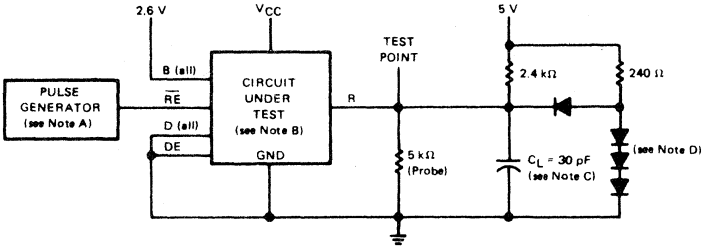


VOLTAGE WAVEFORMS

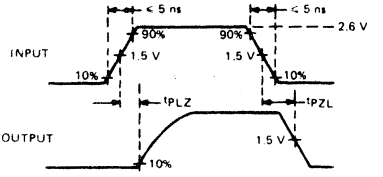
FIGURE 2–PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR = 10 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

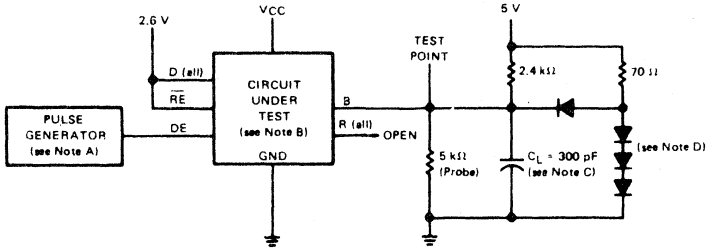


TEST CIRCUIT

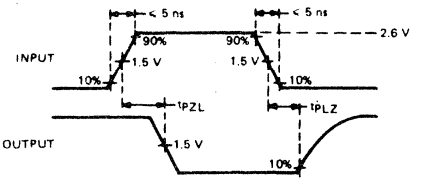


VOLTAGE WAVEFORMS

FIGURE 3–RECEIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

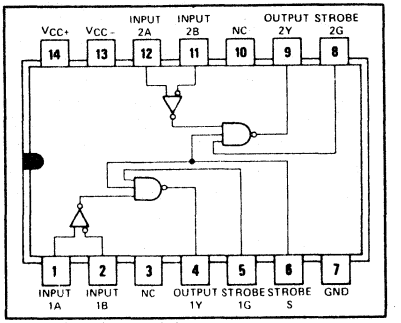
NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR = 5 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

TYPES SN55107A, SN55107B, SN55108A, SN55108B, SN75107A, SN75107B, SN75108A, SN75108B DUAL LINE RECEIVERS

BULLETIN NO. DL-S 12493, JANUARY 1977

- High Speed
- Standard Supply Voltages
- Dual Channels
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Range of ±3 V
- Differential Input Common-Mode Range of More than ±15 V Using External Attenuator
- Strobe Inputs For Receiver Selection
- Gate Inputs For Logic Versatility
- TTL or DTL Drive Capability
- High D-C Noise Margin
- '107A and '107B Have Totem-Pole Outputs
- '108A and '108B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage For Power-Off Condition

SN55107A, SN55107B, SN55108A, SN55108B . . . J DUAL-IN-LINE PACKAGE
SN75107A, SN75107B, SN75108A, SN75108B . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

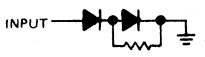
DIFFERENTIAL INPUTS A – B	STROBES G	S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
−25 mV < V_{ID} < 25 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

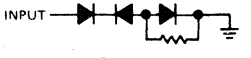
description

These circuits are TTL/DTL compatible high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and replace SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the "A" and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



"A" VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

The SN55107A, SN55107B, SN55108A, and SN55108B, are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0°C to 70°C.

design characteristics

The '107A, '107B, '108A, and '108B line receivers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

These receivers feature independent channels with common voltage supply and ground terminals. The '107A and '107B feature TTL-compatible active pull-up (totem-pole) outputs. The '108A and '108B are also TTL-compatible, but feature an open-collector output configuration that permits the wired-AND logic connection with similar outputs (such as the SN5401/SN7401 TTL gate or other '108A/'108B line receivers). This permits a level of logic to be implemented without extra delay. All other features of the line receivers are identical.

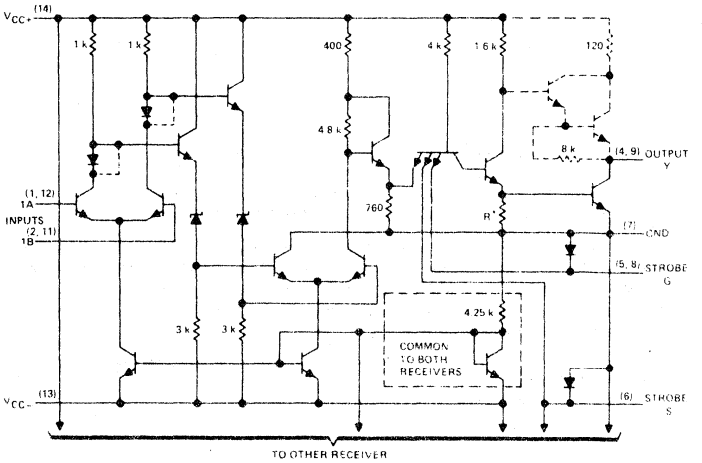
The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

5

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. These line receivers are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels. For applications that require a greater sensitivity (±10 mV), the SN75207, SN75207B, SN75208, and SN75208B are recommended.

schematic (each receiver)



*R = 1 kΩ for '107A and '107B, 750 Ω for '108A and '108B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '107A and 107B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '107A and '108A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage V_{CC-} . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±6 V
Common-mode input voltage (see Note 3) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4) . . . . . 600 mW
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

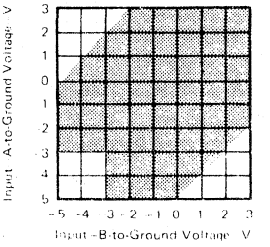
recommended operating conditions (see note 5)

	SN55107A, SN55107B SN55108A, SN55108B			SN75107A, SN75107B SN75108A, SN75108B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16			−16	mA
Differential input voltage, V_{ID} (see Note 6)	−5†		5	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 6 and 7)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (see Note 6)	−5†		3	−5†		3	V
Operating free-air temperature, T_A	−55		125	0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation of SN55107A, SN55107B, SN55108A, or SN55108B above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, these Series 55 chips are alloy mounted; Series 75 chips are glass mounted.
5. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
6. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
7. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.025	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.025	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

† The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		'107A, '107B			'108A, '108B			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V	V_{IDH} = 25 mV	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V	V_{IDL} = −25 mV			0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

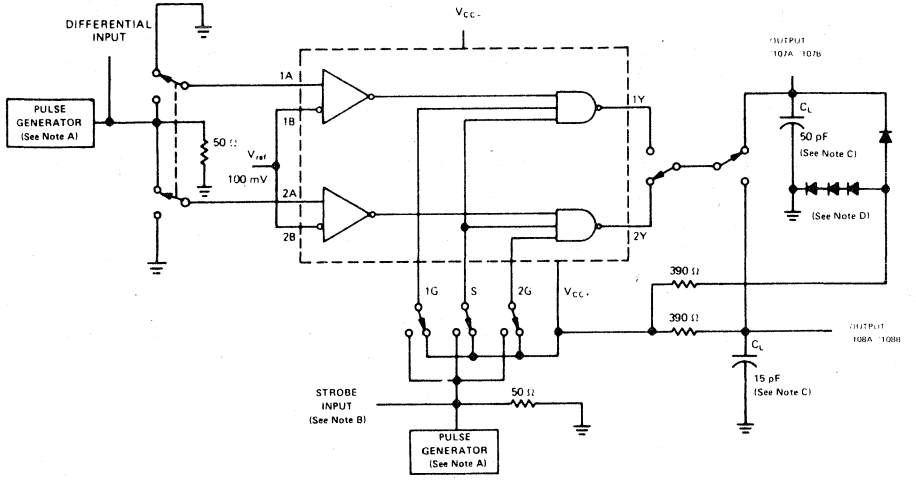
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

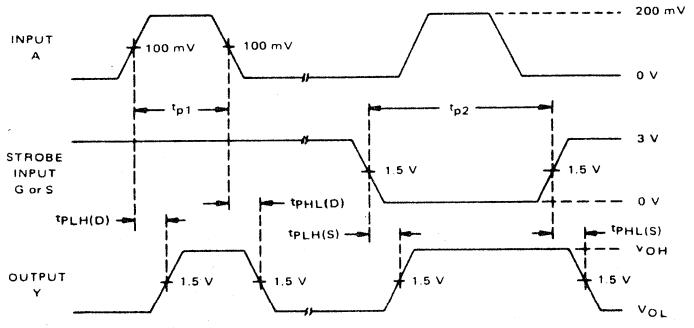
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS	'107A, '107B			'108A, '108B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		10	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		8	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 μs, PRR = 500 kHz.

B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N916.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

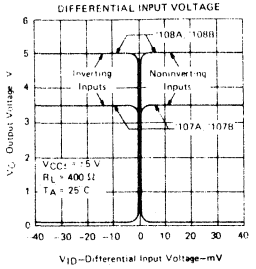


FIGURE 2

HIGH LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

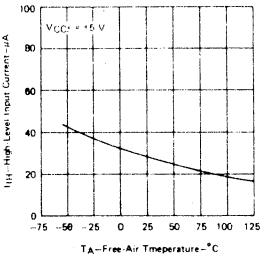


FIGURE 3

SUPPLY CURRENT, OUTPUTS HIGH
vs
FREE-AIR TEMPERATURE

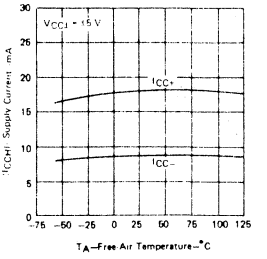


FIGURE 4

'107A, '107B
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

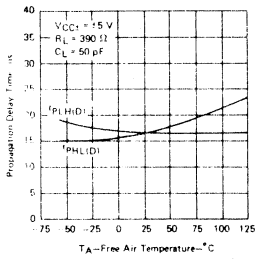


FIGURE 5

'108A, '108B
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

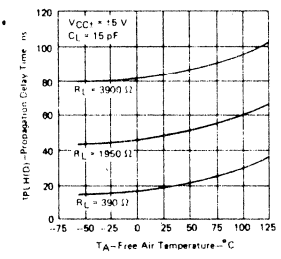


FIGURE 6

'108A, '108B
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

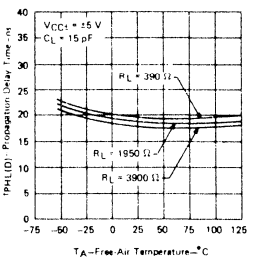


FIGURE 7

'107A, '107B
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

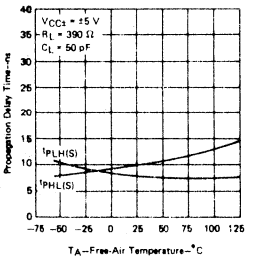


FIGURE 8

'108A, '108B
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

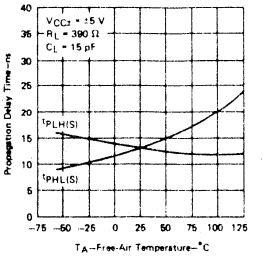


FIGURE 9

† Data for temperatures below 0°C and above 70°C are applicable for Series 55 devices only.

TYPICAL APPLICATION DATA

basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2 I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \approx I_{O(on)} \cdot R_T.$$

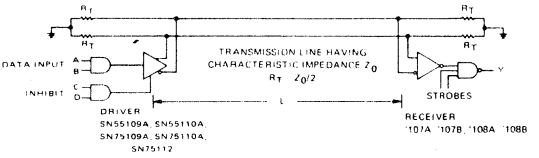


FIGURE 10

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

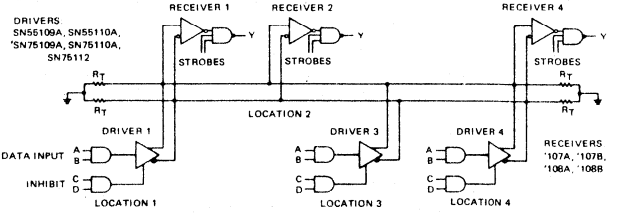


FIGURE 11

TYPICAL APPLICATION DATA

unbalanced or single-line systems

These dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 volts to +3 volts. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

5

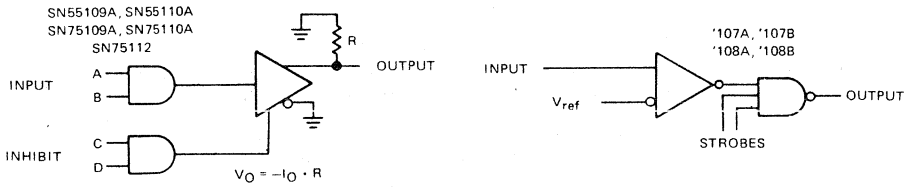


FIGURE 12

'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

For rules for such dot-AND connections, refer to the SN5401/SN7401 data sheet.

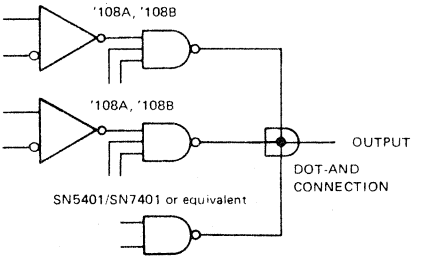


FIGURE 13

increasing common-mode input voltage range of receiver

The common-mode voltage range or CMVR is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 volts, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore reducing the versatility of the receiver.

TYPICAL APPLICATION DATA

increasing common-mode input voltage range of receiver, continued

The ability of the receiver to operate with approximately ±15 volts common-mode voltage at the inputs has been checked using the circuit shown in Figure 14. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately ±3 volts common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table A.

TABLE A

Attenuator 1: R1 = 2 kΩ, R2 = 0.5 kΩ
Attenuator 2: R1 = 6 kΩ, R2 = 1.5 kΩ
Attenuator 3: R1 = 12 kΩ, R2 = 3 kΩ

Table B shows some of the typical switching results obtained under such conditions.

TABLE B – TYPICAL PROPAGATION DELAYS FOR RECEIVER WITH ATTENUATOR TEST CIRCUIT SHOWN IN FIGURE 14

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
'107A, '107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
'108A, '108B	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

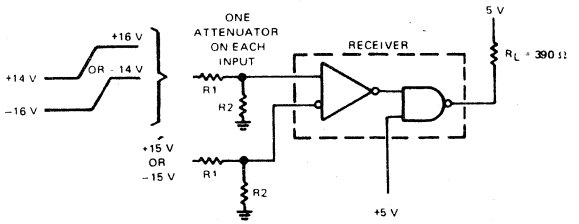


FIGURE 14–COMMON-MODE CIRCUIT FOR TESTING INPUT ATTENUATORS, WITH RESULTS SHOWN IN TABLE B

Two methods of terminating a transmission line to reduce reflections are:

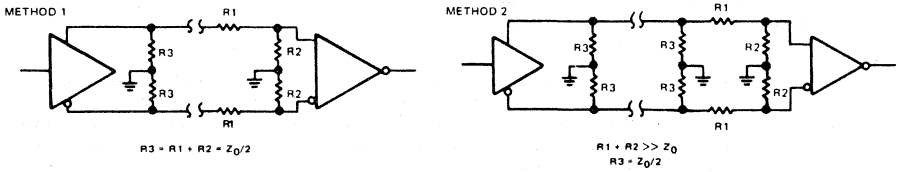


FIGURE 15

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

TYPICAL APPLICATION DATA

increasing common-mode input voltage range of receiver, continued

For party-line operation, method 2 should be used as follows:

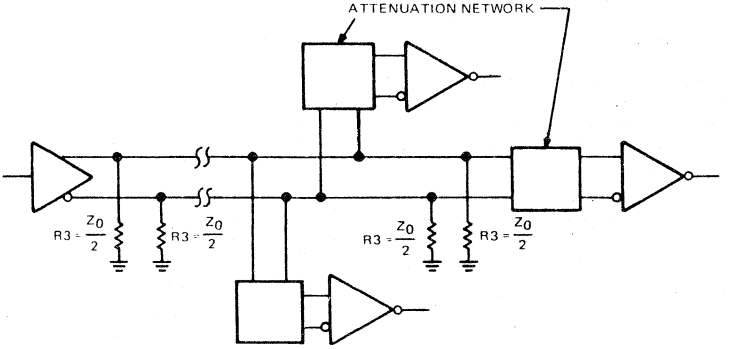


FIGURE 16

To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table A.

furnace control using the SN75108A

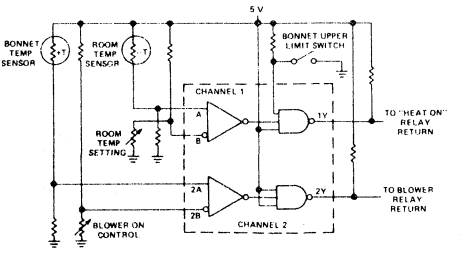


FIGURE 17—FURNACE CONTROL USING SN75108A

The furnace control circuit in Figure 17 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically the operation of this control is as follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the "heat on" relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the "heat on" relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

TYPICAL APPLICATION DATA

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters (shown in Figure 18a) restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 18b.

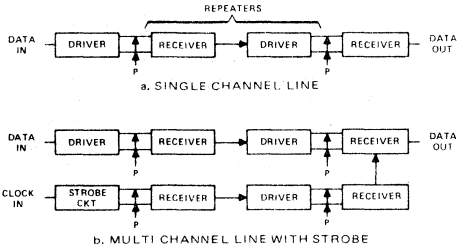


FIGURE 18–RECEIVER-DRIVER REPEATERS

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse width control.

As a differential comparator, a '107A or '108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 19. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

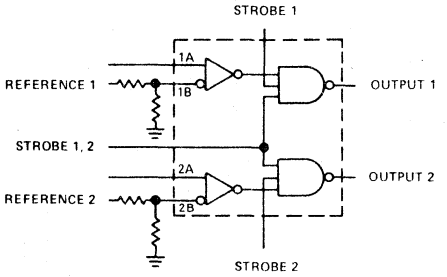
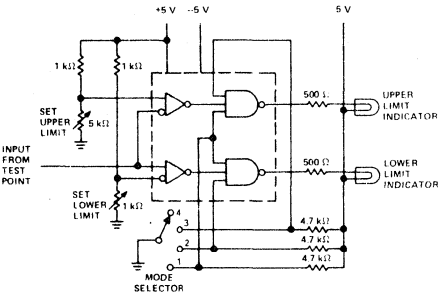


FIGURE 19–SN55107A SERIES RECEIVER AS A DUAL DIFFERENTIAL COMPARATOR

window detector

The window detector circuit in Figure 20 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time – such as detecting whether a voltage or signal has exceeded its limits or "window". Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the "upper and lower limits" test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	OFF
2	TEST FOR UPPER LIMIT
3	TEST FOR LOWER LIMIT
4	TEST FOR UPPER AND LOWER LIMITS

FIGURE 20–WINDOW DETECTOR USING SN75108A

TYPICAL APPLICATION DATA

temperature controller with zero-voltage switching

The circuit in Figure 21 switches an electric resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is AND'ed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

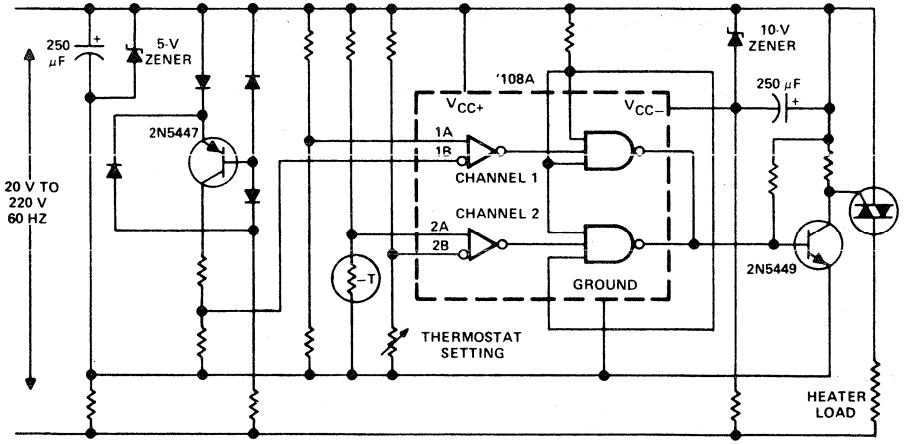


FIGURE 21–ZERO-VOLTAGE SWITCHING TEMPERATURE CONTROLLER

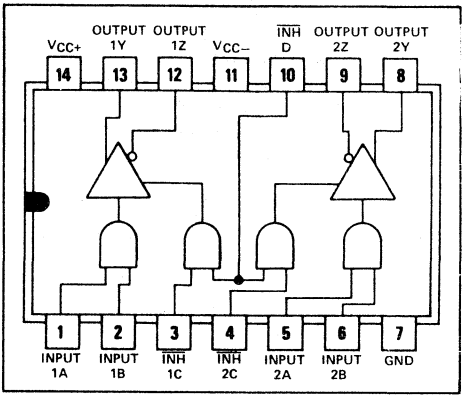
TYPES SN55109A, SN55110A, SN75109A, SN75110A, SN75112 DUAL LINE DRIVERS

BULLETIN NO. DL-S 12334, DECEMBER 1975—REVISED JANUARY 1977

- Improved Stability over Supply Voltage and Temperature Ranges
- Constant-Current Output
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range (−3 V to 10 V)
- TTL Input Compatibility
- Inhibitor Available for Driver Selection

−55°C to 125°C J Package	0°C to 70°C J or N Package	OUTPUT FUNCTION
SN55109A	SN75109A	6-mA Current Switch
SN55110A	SN75110A	12-mA Current Switch
	SN75112	27-mA Current Switch

SN55109A, SN55110A . . . J DUAL-IN-LINE PACKAGE
SN75109A, SN75110A, SN75112 . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 have improved output current regulation with supply voltage and temperature variations. In addition the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

FUNCTION TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level, X = irrelevant

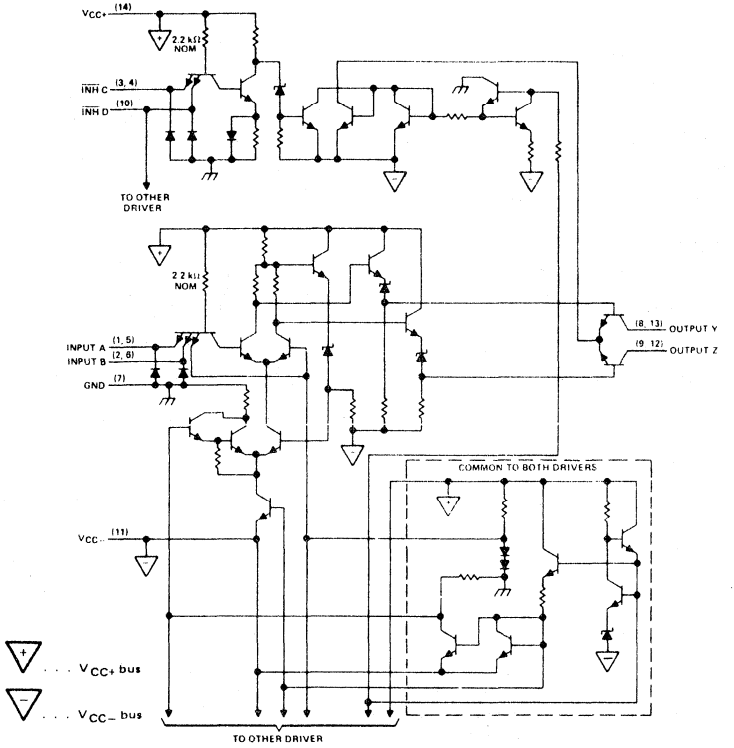
These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the inhibit inputs. The output current is nominally 6 milliamperes for the '109A, 12 milliamperes for the '110A, and 27 milliamperes for the SN75112.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to 10 volts, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2.0 volts for high-logic-level input conditions and 0.8 volt for low-logic-level input conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	−7 V
Input voltage (any input)	5.5 V
Output voltage (any output)	−5 V to 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature, Series 55	−55°C to 125°C
Series 75	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55109A and SN55110A chips are alloy-mounted; SN75109A, SN75110A, and SN75112 chips are glass-mounted.

recommended operating conditions (see note 3)

	SN55109A, SN55110A			SN75109A, SN75110A, SN75112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage	0		10	0		10	V
Negative common-mode output voltage	0		−3	0		−3	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A, SN75109A			SN55110A, SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_I = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	μA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				−10			−17			−32		

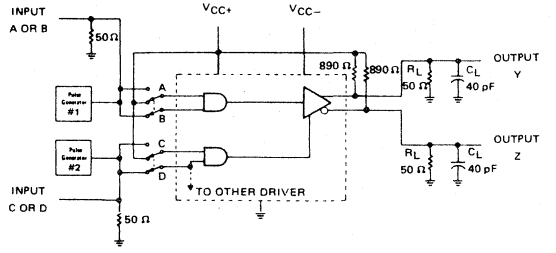
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

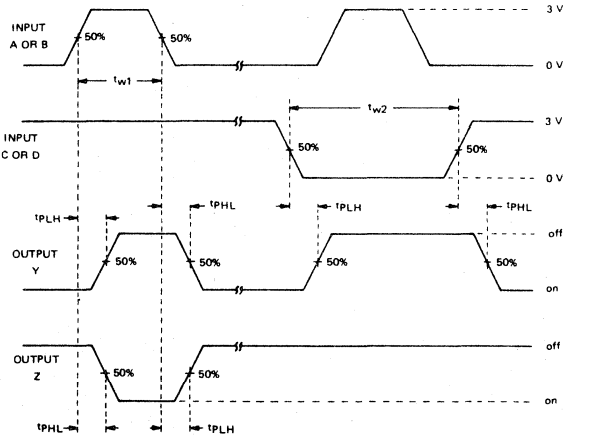
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

§ t_{PLH} ≡ Propagation delay time, low-to-high-level output.
t_{PHL} ≡ Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 500 ns, PRR = 1 MHz, t_{w2} = 1 μs, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

ON-STATE OUTPUT CURRENT vs NEGATIVE SUPPLY VOLTAGE

SN55109A, SN75109A

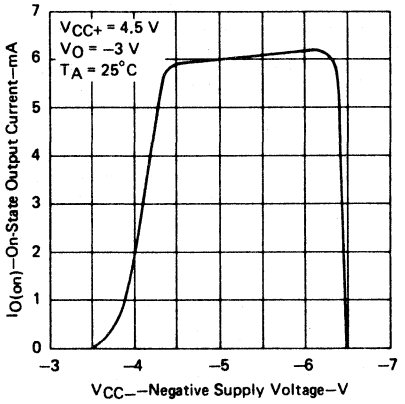


FIGURE 2

SN55110A, SN75110A

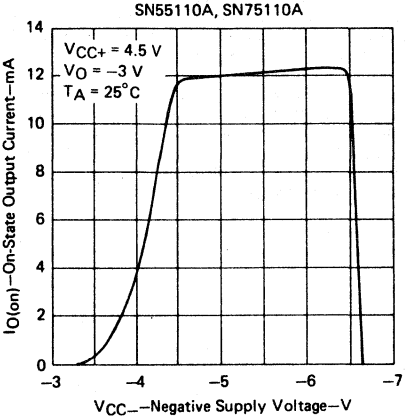


FIGURE 3

SN75112

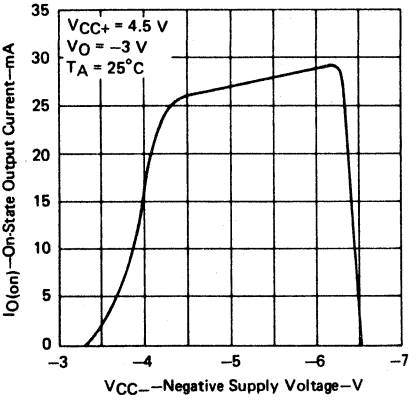


FIGURE 4

TYPICAL APPLICATION INFORMATION

basic balanced-line transmission system

The '109A, '110A, and SN75112 dual line drivers are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately: $V_{DIFF} \approx 1/2\ I_{O(on)} \cdot R_T$

High series line resistance will cause degradation of the signal. However, line receivers such as the SN55107A, SN55108A, SN75107A, and SN75108A will detect signal as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately: $V_{DIFF} \approx I_{O(on)} \cdot R_T$

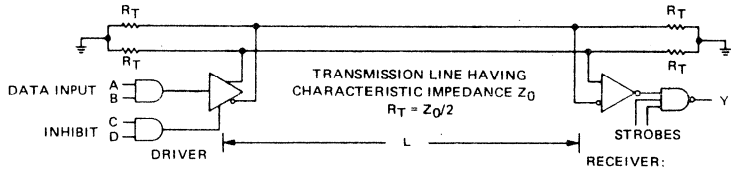


FIGURE 5

data-bus or party-line system

The strobe feature of the '109A, '110A, and SN75112 line drivers allow these circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers are disabled. This series of drivers has been designed to allow widely varying thermal and electrical environments at the various terminal locations. The data-bus system offers maximum performance at minimum cost.

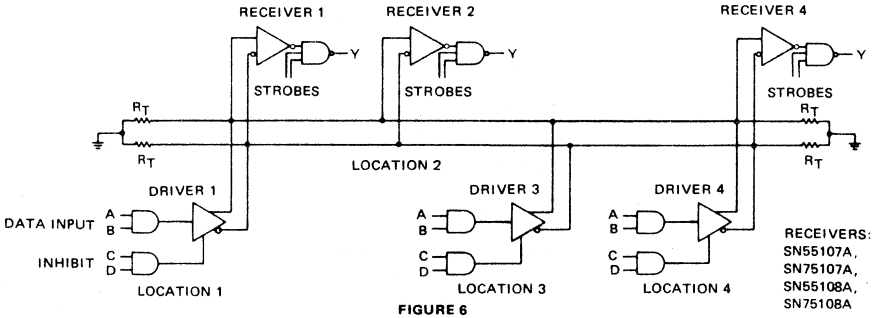


FIGURE 6

TYPICAL APPLICATION DATA

special pulse-control circuit

Figure 7 shows a circuit that may be used as a pulse generator output or in many other testing applications.

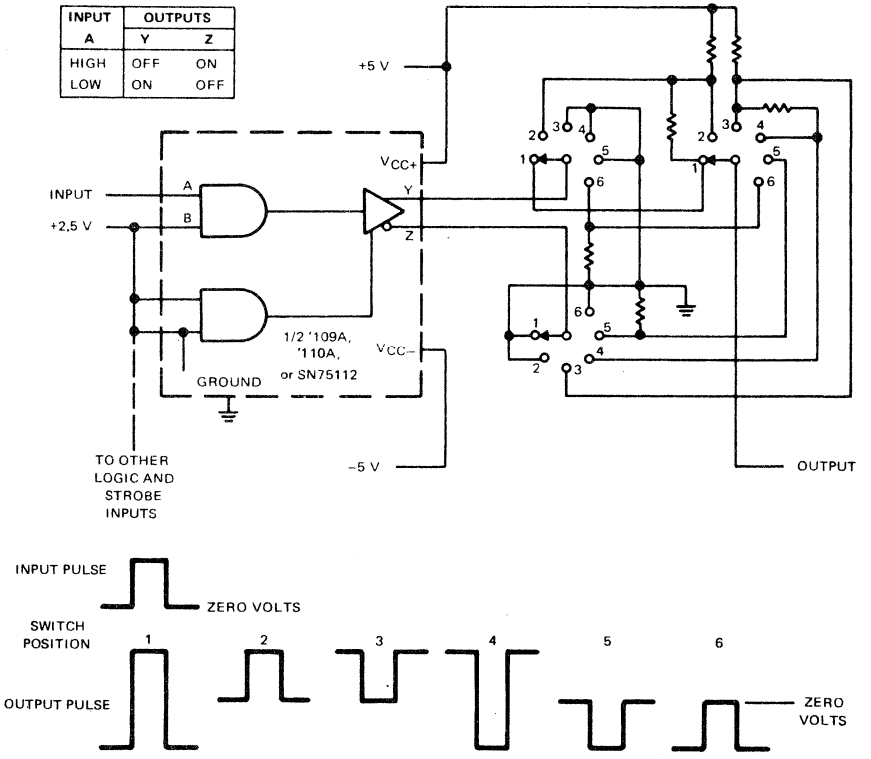


FIGURE 7–PULSE CONTROL CIRCUIT

TYPES SN55113, SN55114, SN55115, SN75113, SN75114, SN75115 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

BULLETIN NO. DL-S 11910, SEPTEMBER 1973—REVISED SEPTEMBER 1980

LINE CIRCUITS
featuring

- Each Circuit Offers Choice of Open-Collector or Active Pull-Up (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL/DTL Compatibility

additional features of SN55113 and SN75113 line drivers with three-state outputs

- High-Impedance Output State for Party-Line Applications
- Short-Circuit Protection
- High-Current Outputs
- Single-Ended or Differential AND/NAND Outputs
- Common and Individual Output Controls
- Clamp Diodes at Inputs
- Easily Adaptable to SN55114 and SN75114 Applications

additional features of SN55114 and SN75114 line drivers

- Designed to be Interchangeable with Fairchild 9614 Line Drivers
- Short-Circuit Protection of Outputs
- High-Current Outputs
- Clamp Diodes at Inputs and Outputs to Terminate Line Transients
- Single-Ended or Differential AND/NAND Outputs
- Triple Inputs

additional features of SN55115 and SN75115 line receivers

- Designed to be interchangeable with Fairchild 9615 Line Receivers
- ±15 V Common-Mode Input Voltage Range
- Optional-Use Built-In 130-Ω Line-Terminating Resistor
- Individual Frequency Response Controls
- Individual Channel Strobes

CONTENTS

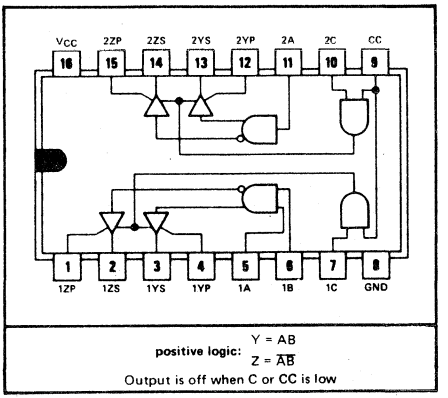
TYPES SN55113, SN75113
DUAL DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

description

The SN55113 and SN75113 dual differential line drivers with three-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = AB$, $Z = \overline{AB}$

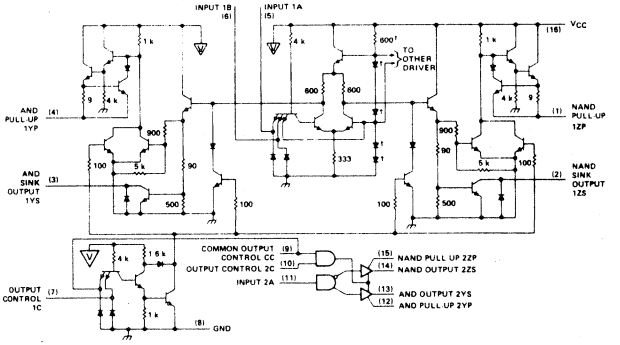
Output is off when C or CC is low

FUNCTION TABLE

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B†	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)
†B input and 4th line of function table applicable only to driver number 1.

schematic



▽ . . . V_{CC} bus
Resistor values shown are nominal and in ohms.

†These components common to both drivers.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55113	−55°C to 125°C
SN75113	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55113 chips are alloy-mounted; SN75113 chips are glass-mounted.

REVISED SEPTEMBER 1980

recommended operating conditions

	SN55113			SN75113			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

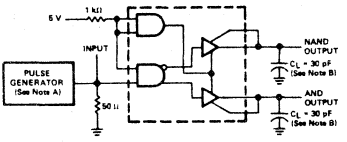
PARAMETER			TEST CONDITIONS†			SN55113			SN75113			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 40 mA			0.23	0.4		0.23	0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX,	I_O = −40 mA			−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25 V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10			±10	μA
				T_A = MAX	V_O = 0			−150			−20	
					V_O = 0.4 V			±80			±20	
					V_O = 2.4 V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
		CC						2			2	
I_{IH}	High-level input current	A, B, C	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
		CC						80			80	
I_{IL}	Low-level input current	A, B, C	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0,	T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)		All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		47	65		47	65	mA
					V_{CC} = 7 V		65	85		65	85	

† All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

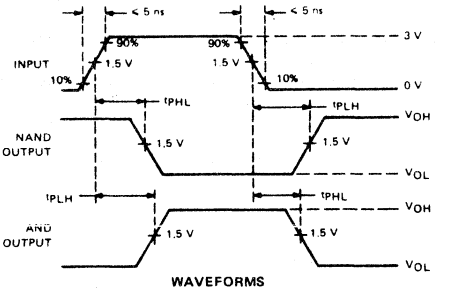
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55113			SN75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 1		13	20		13	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	ns
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 2		7	15		7	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 3		14	30		14	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 2		10	20		10	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 3		17	35		17	35	ns

PARAMETER MEASUREMENT INFORMATION

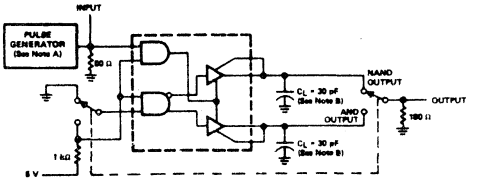


TEST CIRCUIT

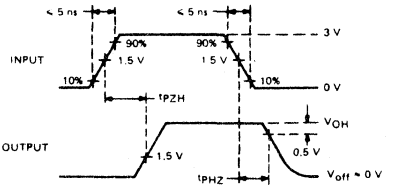


WAVEFORMS

FIGURE 1—t_{PLH} and t_{PHL}

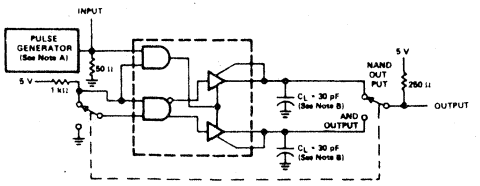


TEST CIRCUIT

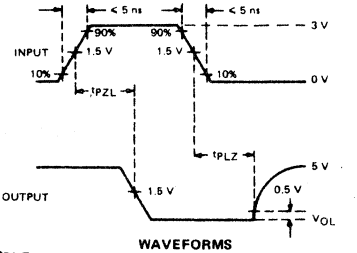


WAVEFORMS

FIGURE 2—t_{PZH} and t_{PHZ}



TEST CIRCUIT



WAVEFORMS

FIGURE 3—t_{PZL} and t_{PLZ}

NOTES: A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

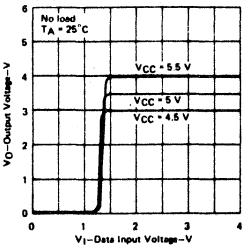


FIGURE 4

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

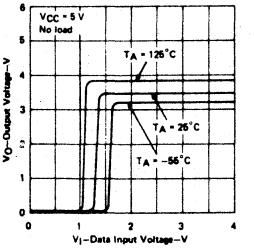


FIGURE 5

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

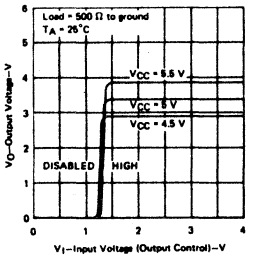


FIGURE 6

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

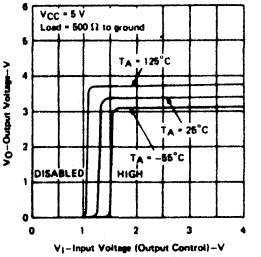


FIGURE 7

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

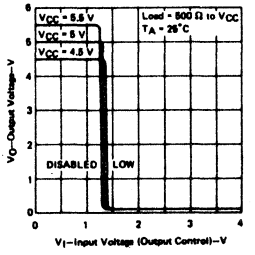


FIGURE 8

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

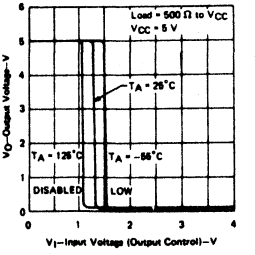


FIGURE 9

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

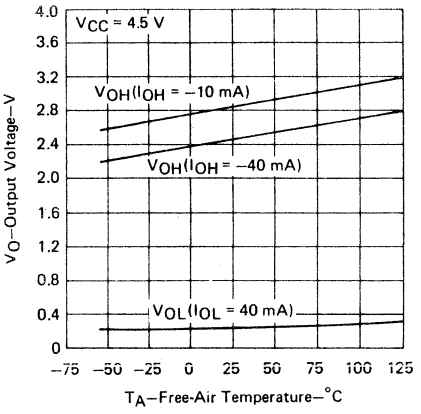


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

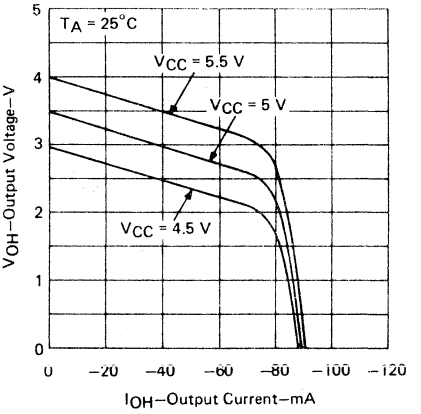


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

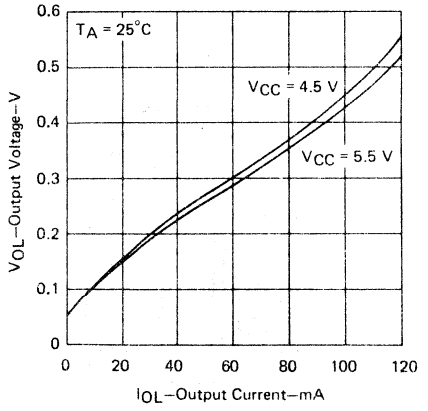


FIGURE 12

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

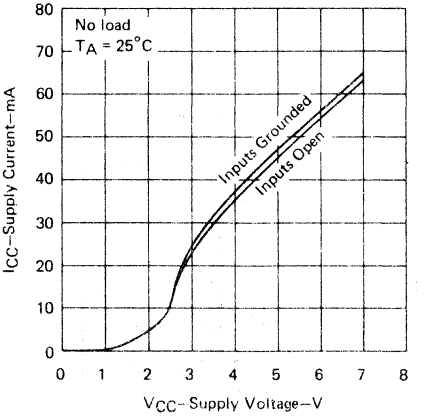


FIGURE 13

†Data for temperature below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

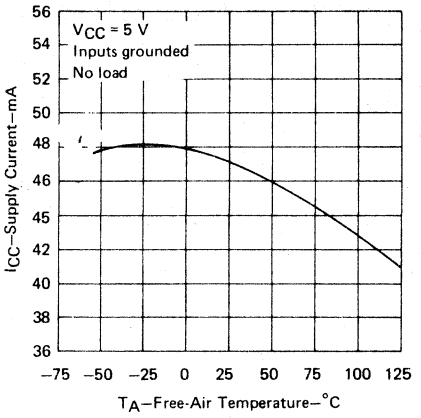


FIGURE 14

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

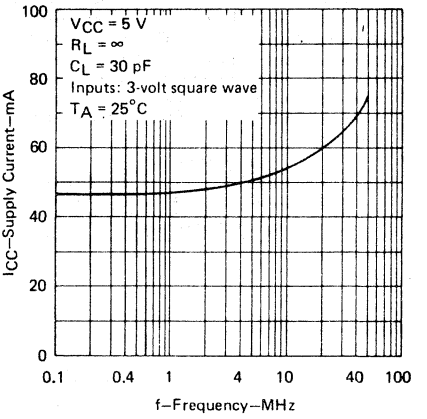


FIGURE 15

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

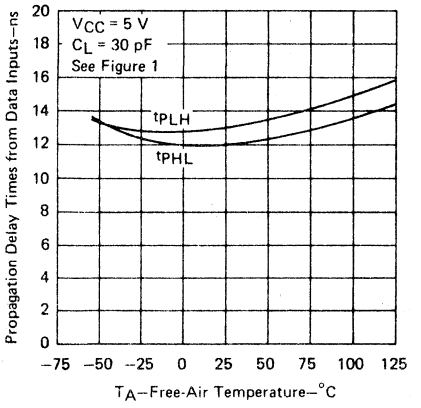


FIGURE 16

OUTPUT ENABLE and DISABLE TIMES
vs
FREE-AIR TEMPERATURE

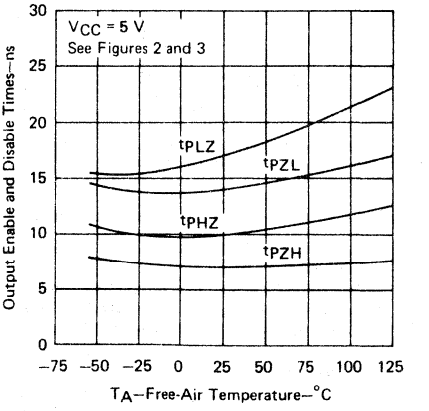


FIGURE 17

† Data for temperature below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPES SN55114, SN75114
DUAL DIFFERENTIAL LINE DRIVERS

description

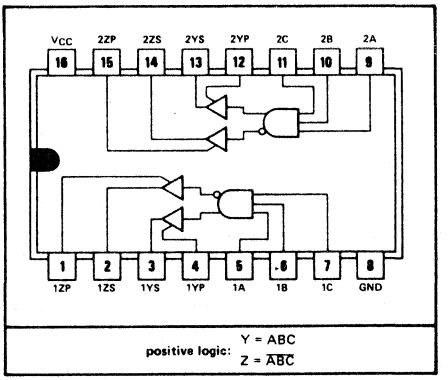
The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted-pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	H	H	H	L
ALL OTHER INPUT COMBINATIONS			L	H

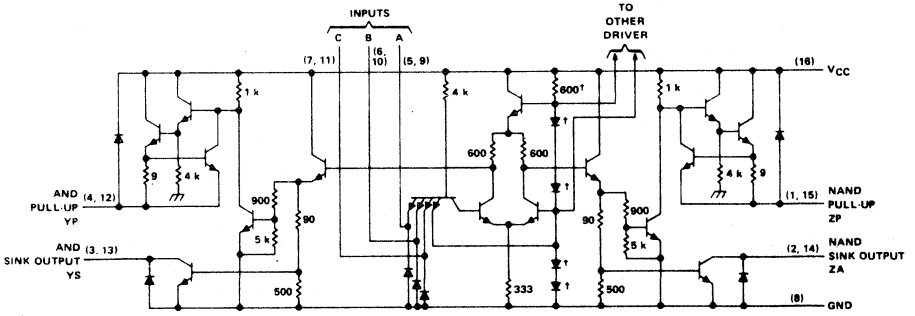
H = high level, L = low level

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = ABC$, $Z = \overline{ABC}$

schematic (each driver)



†These components common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55114	−55°C to 125°C
SN75114	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55114 chips are alloy-mounted; SN75114 chips are glass-mounted.

recommended operating conditions

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

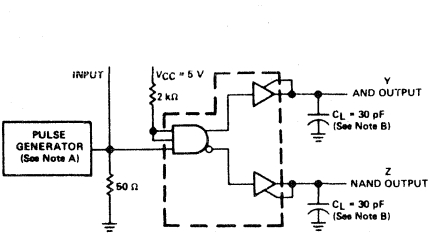
PARAMETER		TEST CONDITIONS†			SN55114			SN75114			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 40 mA			0.2	0.4		0.2	0.45	V
V_{OK}	Output clamp voltage	V_{CC} = 5 V,	I_O = 40 mA,	T_A = 25°C		6.1	6.5		6.1	6.5	V
		V_{CC} = MAX,	I_O = −40 mA,	T_A = 25°C		−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25 V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_O = 0,	T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)	All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		37	50		37	50	mA
				V_{CC} = 7 V		47	65		47	70	

† All parameters, with the exception of off-state open-collector output current, are measured with the active pull-up connected to the sink output.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

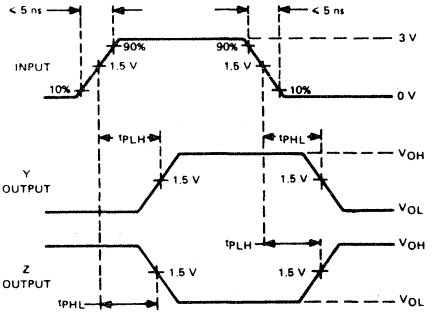
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55114			SN75114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 18		15	20		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20		11	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 100 ns, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 18–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

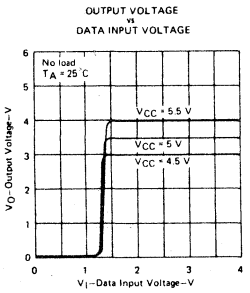


FIGURE 19

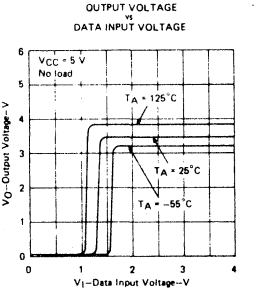


FIGURE 20

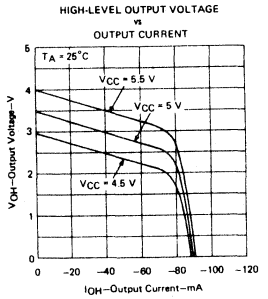


FIGURE 21

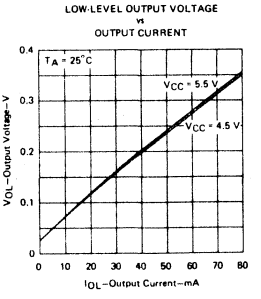


FIGURE 22

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

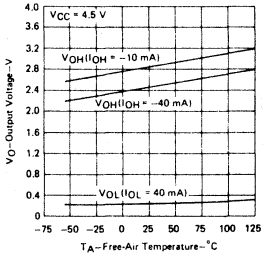


FIGURE 23

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

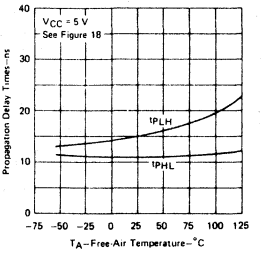


FIGURE 24

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

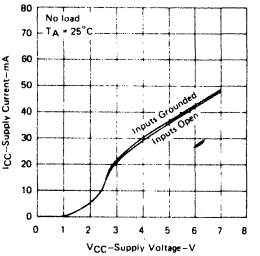


FIGURE 25

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

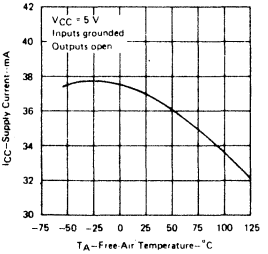


FIGURE 26

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

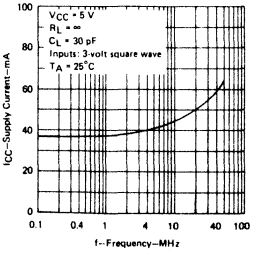


FIGURE 27

†Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

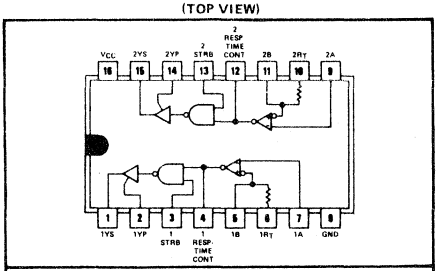
TYPES SN55115, SN75115
DUAL DIFFERENTIAL LINE RECEIVERS

description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The open-collector output configuration permits the wire-AND connection with similar outputs (such as SN5401/SN7401 TTL gates or other SN55115/SN75115 line receivers). This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, 1YS and 2YS, and the corresponding active pull-up terminals, 1YP and 2YP, available on adjacent package pins. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

5

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



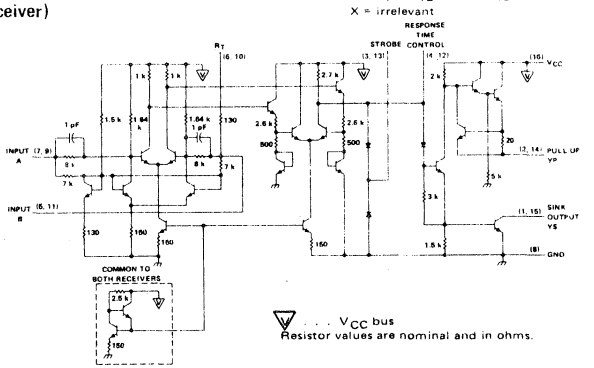
positive logic: see function table

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

schematic (each receiver)



. . . V_{CC} bus
Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage at A, B, and R_T inputs	±25 V
Input voltage at strobe input	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total dissipation at (or below 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55115	−55°C to 125°C
SN75115	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55115 chips are alloy-mounted; SN75115 chips are glass-mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−5			−5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

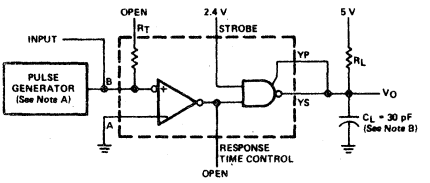
PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{TH}§	Differential input high-threshold voltage	V_O = 0.4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{TL}§	Differential input low-threshold voltage	V_O = 2.4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
$V_{IH(strobe)}$	High-level strobe input voltage			2.4			2.4			V
$V_{IL(strobe)}$	Low-level strobe input voltage					0.4			0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = 0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other Input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	μA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response-time-control current (Pin 4 or Pin 12)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				μA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-circuit output current♦	V_{CC} = MAX, V_O = 0, V_{ID} = −0.5 V	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
§Differential voltages are at the B input terminal with respect to the A input terminal.
¶The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
♦Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

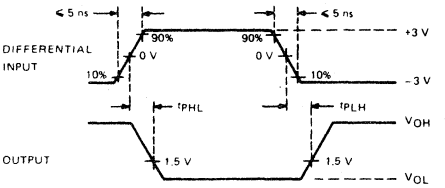
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN55115			SN75115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	R_L = 3.9 kΩ, See Figure 28		18	50		18	75	ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 390 Ω, See Figure 28		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

FIGURE 28—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

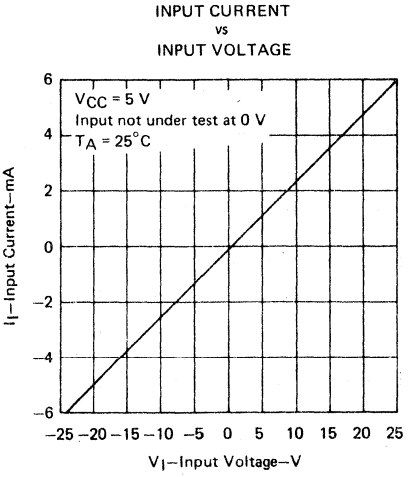


FIGURE 29

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

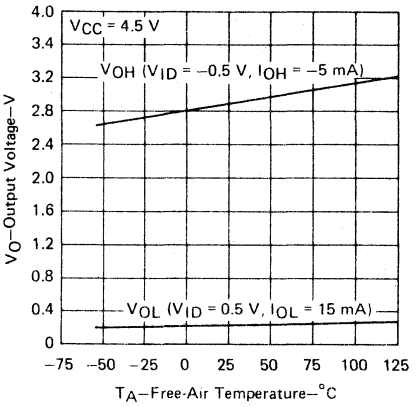


FIGURE 30

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

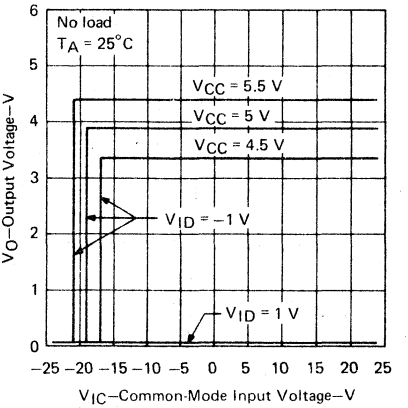


FIGURE 31

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT†

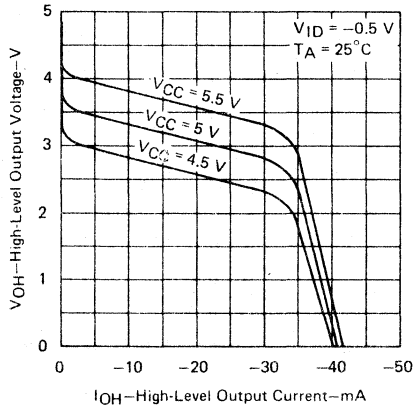


FIGURE 32

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

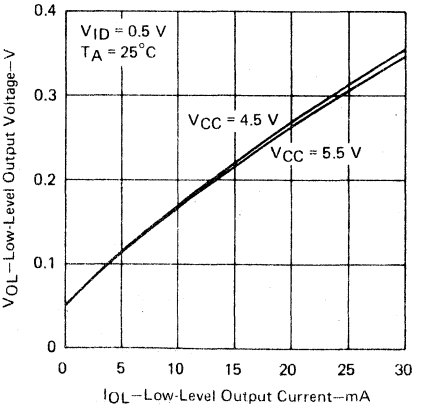


FIGURE 33

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

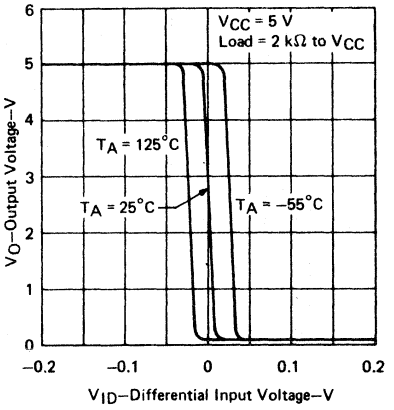


FIGURE 34

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

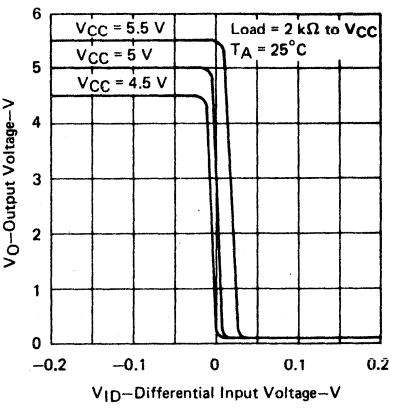


FIGURE 35

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

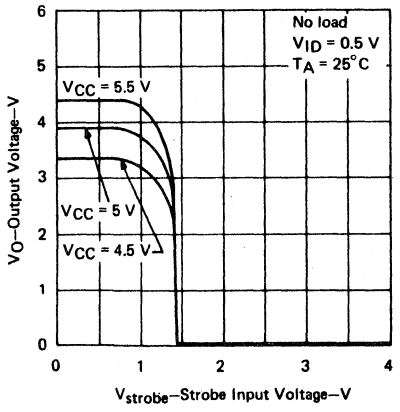


FIGURE 36

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

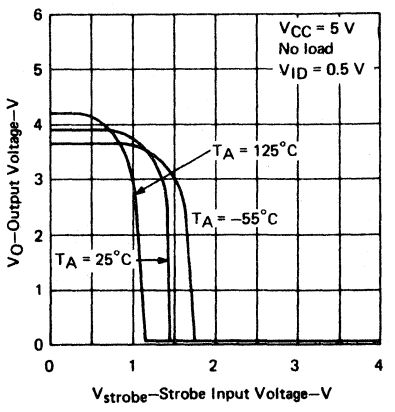


FIGURE 37

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
SUPPLY VOLTAGE

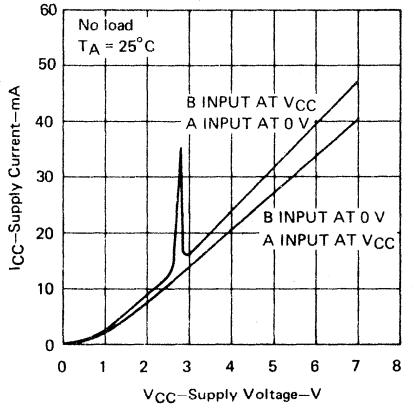


FIGURE 38

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
FREE-AIR TEMPERATURE

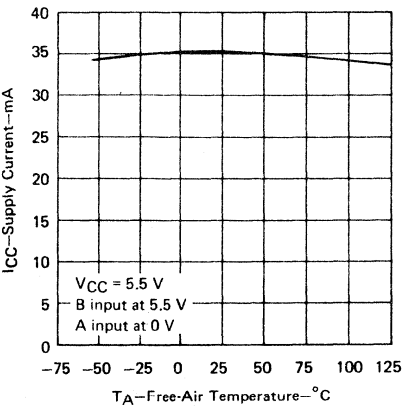


FIGURE 39

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

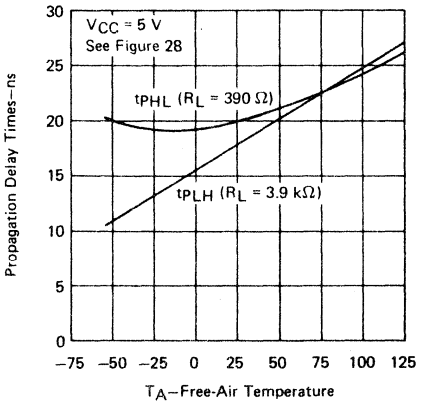


FIGURE 40

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

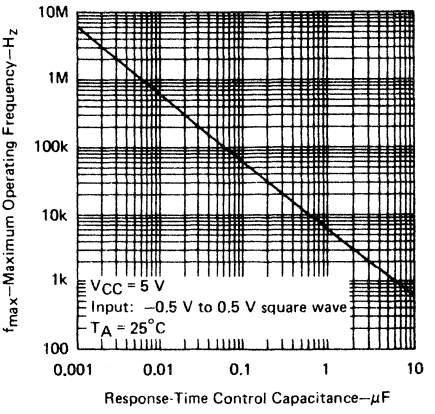
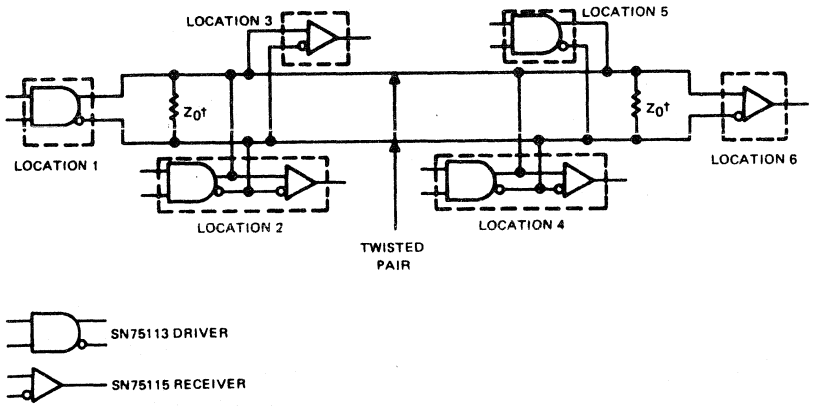


FIGURE 41

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL APPLICATION DATA



†A capacitor may be connected in series with Z_0 to reduce power dissipation.

FIGURE 42–BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

TYPES SN55116 THRU SN55119, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

BULLETIN NO. DL-S 12376, MAY 1976 – REVISED SEPTEMBER 1980

features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, '117) or Enable ('118, '119)
- Designed for Party-Line (Data-Bus) Applications
- Choice of Ceramic or Plastic Packages

additional features of the SN55116/SN55116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

additional features of the SN55117/SN75117

- Driver Output Internally Connected to Receiver Input

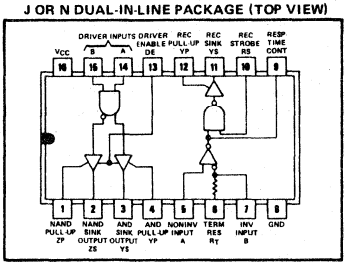
The SN55118/SN75118 is an SN55116/SN75116 with 3-State Receiver Output Circuitry

The SN55119/SN75119 is an SN55117/SN75117 with 3-State Receiver Output Circuitry

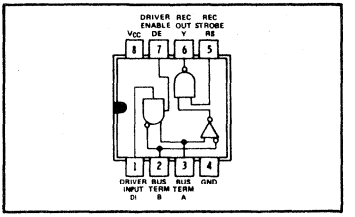
description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a three-state differential line driver and a differential-input line receiver, both of which operate from a single 5-volt power supply. The driver inputs and receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 three-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

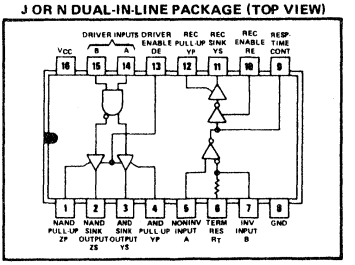
SN55116, SN75116
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



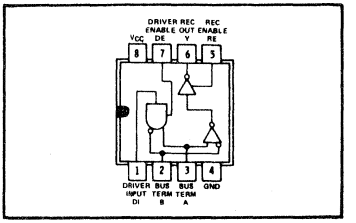
SN55117, SN75117
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55118, SN75118
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55119, SN75119
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



description (continued)

The '116 and '118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver. The driver performs the dual input AND and NAND functions when enabled, or presents a high impedance to the load when in the disabled state. The driver output stages are similar to the TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package pins. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink pins together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and '118 features a differential-input circuit having a common-mode voltage range of ±15 volts. An internal 130-ohm resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control pin allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the '118 has an output-enable for the three-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground pins.

The '117 and '119 circuits provide the basic driver and receiver functions of the '116 and '118, but use a package that is only half as large. The '117 and '119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the '117 receiver has an output strobe while the '119 receiver has a three-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency response controls.

The SN55116, SN55117, SN55118, and SN55119 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

'116, '118
FUNCTION TABLE
OF DRIVER

INPUTS			OUTPUTS	
DE	A	B	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

'116, '118
FUNCTION TABLE OF RECEIVER

STROBE OR ENABLE	DIFF INPUT	OUTPUT Y	
		'116	'118
L	X	H	Z
H	L	H	H
H	H	L	L

'117, '119
FUNCTION TABLE
OF DRIVER

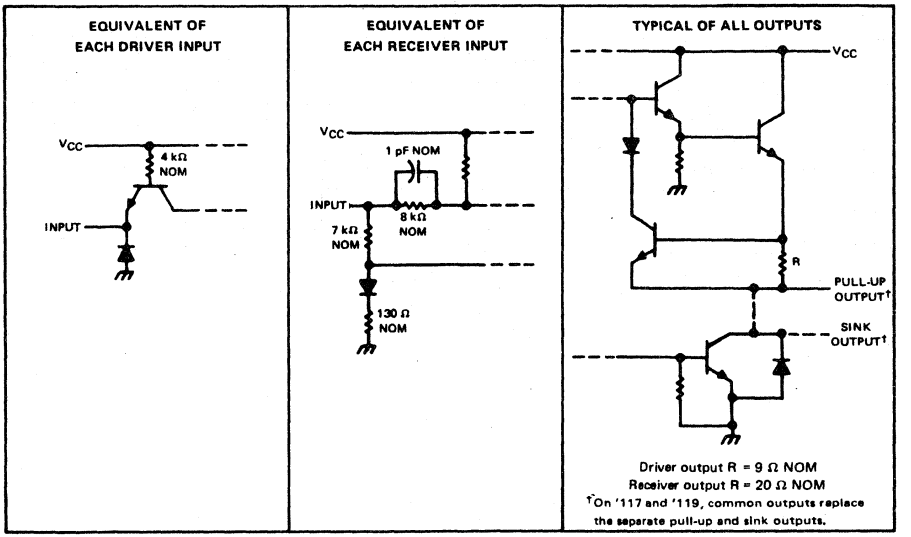
INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'117, '119
FUNCTION TABLE OF RECEIVER

INPUTS			OUTPUT Y	
A	B	RS/RE	'117	'119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max)
L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max)
X = irrelevant
Z = high impedance (off)
? = indeterminate

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage at data, enable, and strobe inputs	5.5 V
Input voltage at receiver and termination inputs: '116 and '118	±25 V
Input voltage at receiver inputs: '117 and '119	0 to 6 V
Off-state voltage applied to open-collector outputs: '116 and '118	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55'	−55°C to 125°C
SN75'	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55116 through SN55119 chips are alloy-mounted; SN75116 through SN75119 chips are glass-mounted.

recommended operating conditions

		SN55'			SN75'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Drivers			−40			−40	mA
	Receivers			−5			−5	
Low-level output current, I_{OL}	Drivers			40			40	mA
	Receivers			15			15	
Receiver common-mode input voltage, V_{IC}	'116			±15			±15	V
	'117	0		6	0		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER			TEST CONDITIONS†			'116, '118 MIN	'116, '118 TYP‡	'116, '118 MAX	'117, '119 MIN	'117, '119 TYP‡	'117, '119 MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA		2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA					0.4			0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX, I_O = −40 mA,	DE at 0.8 V				−1.5			−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55′			200				
					SN75′			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, T_A = 25°C	DE at 0.8 V,				±10				μA
			V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55′			−150				
				V_O = 0.4 V to V_{CC}	SN55′			±80				
				V_O = 0 to V_{CC}	SN75′			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V					40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V					−1.6			−1.6	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0,	T_A = 25°C		−40		−120	−40		−120	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX				42	60		42	60	mA

† All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS	SN55′ MIN	SN55′ TYP	SN55′ MAX	SN75′ MIN	SN75′ TYP	SN75′ MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 13		14	20		14	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 14		8	15		8	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 15		17	30		17	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 14		16	20		16	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 15		20	35		20	35	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, '118 MIN	'116, '118 TYP‡	'116, '118 MAX	'117, '119 MIN	'117, '119 TYP‡	'117, '119 MAX	UNIT
V_{TH}♦	Differential input high-threshold voltage¶		V_O = 0.4 V,	I_{OL} = 15 mA	V_{IC} = 0			0.5			0.5	V
					V_{IC} = MAX			1			1	
V_{TL}♦	Differential input low-threshold voltage¶		V_O = 2.4 V,	I_{OH} = −5 mA	V_{IC} = 0	−0.5#			−0.5#			V
					V_{IC} = MAX	−1#			−1#			
V_{ICR}	Common-mode input voltage range¶		V_{CC} = 5 V,	V_{ID} = −1 V or 1 V		+15 to −15			+6 to 0			V
V_{IH}	High-level strobe or enable input voltage					2			2			V
V_{IL}	Low-level strobe or enable input voltage							0.8			0.8	V
V_{OH}	High-level output voltage¶		V_{CC} = MIN,	V_{ID} = −0.5 V,	V_{IC} = 0	2.4			2.4			V
			I_{OH} = −5 mA	V_{ID} = −1 V,	V_{IC} = MAX	2.4			2.4			
V_{OL}	Low-level output voltage¶		V_{CC} = MIN,	V_{ID} = 0.5 V,	V_{IC} = 0			0.4			0.4	V
			I_{OL} = 15 mA	V_{ID} = 1 V,	V_{IC} = MAX			0.4			0.4	
$I_{I(rec)}$	Receiver input current¶		V_{CC} = MAX	V_I = 0 V,	Other input at 0 V	−0.5	−0.9		−0.5	−1		mA
				V_I = 0.4 V,	Other input at 2.4 V	−0.4	−0.7		−0.4	−0.8		
				V_I = 2.4 V	Other input at 0.4 V	0.1	0.3		0.1	0.4		
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, '117			5			5	μA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	'118, '119			1			1	mA
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	'118, '119			40			40	μA
I_{IL}	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V	V_{ID} = 0.5 V,	'116, '117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	'118, '119			−1.6			−1.6	
$I_{(RC)}$	Response-time-control current (Pin 9)		V_{CC} = MAX, RC at 0 V	V_{ID} = 0.5 V,	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = −1 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55'			200				
					SN75'			20				
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	'118, '119			±10			±10	μA
				T_A = MAX	SN55118			±40				
					SN55119						±40	
					SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = −0.5 V	V_O = 0,	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX, V_{IC} = 0	V_{ID} = 0.5 V	T_A = 25°C		42	60		42	60	mA

† Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

♦ Differential voltages are at the B input terminal with respect to the A input terminal.

¶ Measurement of these characteristics on the '117 and '119 requires the driver to be disabled with the driver enable at 0.8 V.

The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS	SN55'			SN75'			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output		R_L = 400 Ω, See Figure 16		20	50		20	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output				17	50		17	75	ns
t_{PZH}	Output enable time to high level	'118	R_L = 480 Ω, See Figure 14		9	15		9	20	ns
t_{PZL}	Output enable time to low level	and	R_L = 250 Ω, See Figure 15		16	25		16	35	ns
t_{PHZ}	Output disable time from high level	'119	R_L = 480 Ω, See Figure 14		12	20		12	30	ns
t_{PLZ}	Output disable time from low level	only	R_L = 250 Ω, See Figure 15		17	25		17	35	ns

TYPICAL CHARACTERISTICS

5

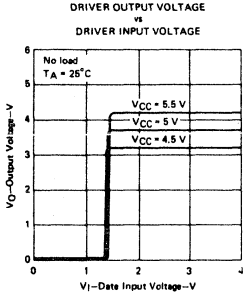


FIGURE 1

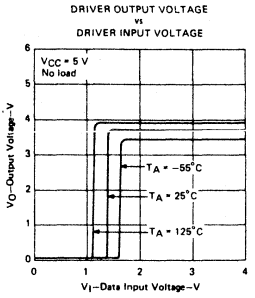


FIGURE 2

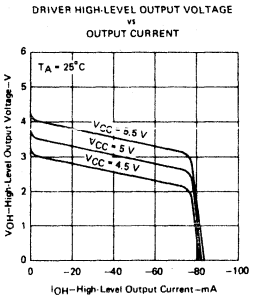


FIGURE 3

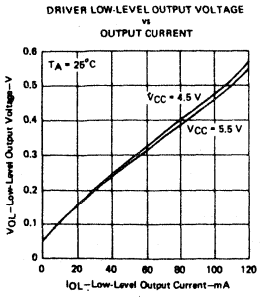


FIGURE 4

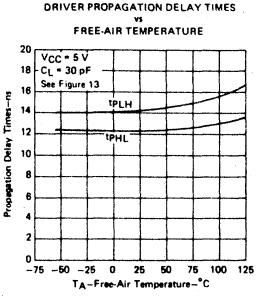


FIGURE 5

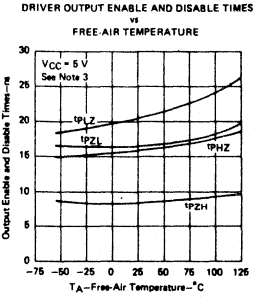


FIGURE 6

NOTE 3: For t_{PZH} and t_{PHZ}: R_L = 180 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

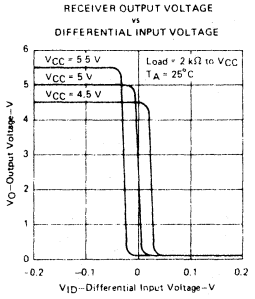


FIGURE 7

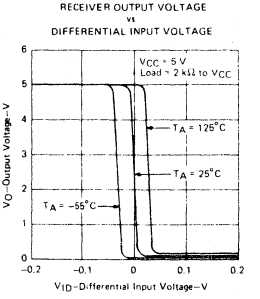


FIGURE 8

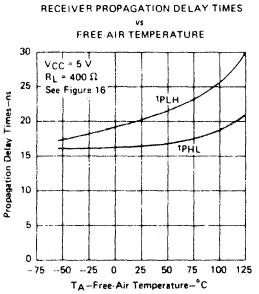


FIGURE 9

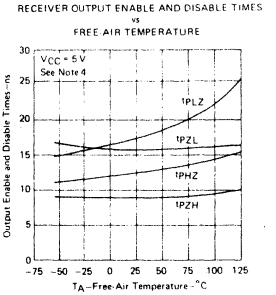


FIGURE 10

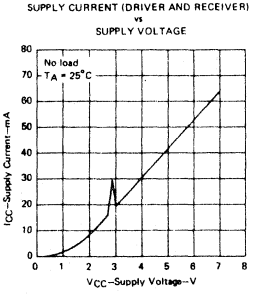


FIGURE 11

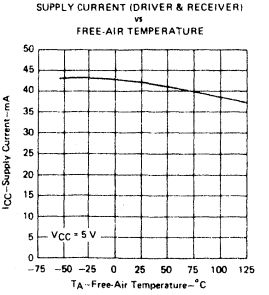
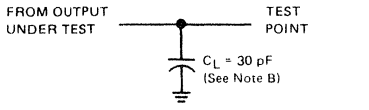


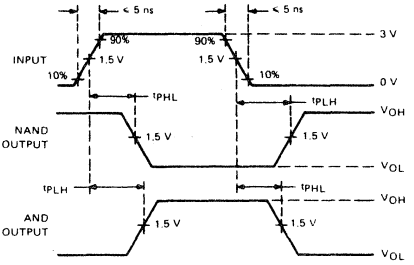
FIGURE 12

NOTE 4: For t_{PZH} and t_{PHZ}: R_L = 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

PARAMETER MEASUREMENT INFORMATION

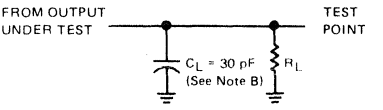


LOAD CIRCUIT

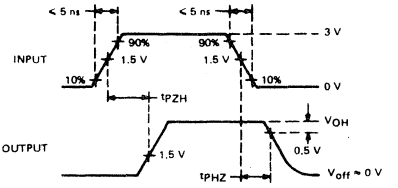


VOLTAGE WAVEFORMS

FIGURE 13–t_{PLH} and t_{PHL} (DRIVERS ONLY)

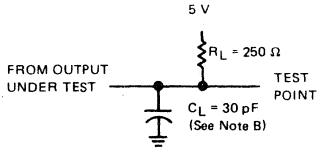


LOAD CIRCUIT

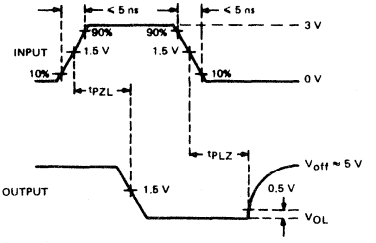


VOLTAGE WAVEFORMS

FIGURE 14–t_{PZH} and t_{PHZ}

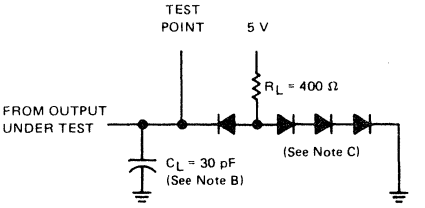


LOAD CIRCUIT

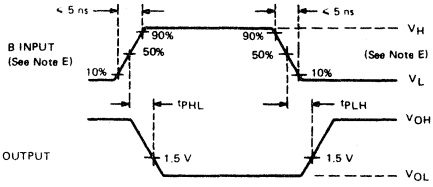


VOLTAGE WAVEFORMS

FIGURE 15–t_{PZL} and t_{PLZ}



LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 16–t_{PLH} and t_{PHL} (RECEIVERS ONLY)

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. When testing the '116 and '118 receiver sections, the response-time control and the termination resistor pins are left open.
E. For '116 and '118, V_H = 3 V, V_L = −3 V, the A input is at 0 V.
For '117 and '119, V_H = 3 V, V_L = 0 V, the A input is at 1.5 V.

TYPES SN55121, SN55122, SN75121, SN75122
DUAL LINE DRIVERS AND TRIPLE LINE RECEIVERS

BULLETIN NO. DL-S 12049, SEPTEMBER 1973 – REVISED APRIL 1974

LINE CIRCUITS

- Designed for Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair
- Designed for Operation with 50-Ω to 500-Ω Transmission Lines
- TTL Compatible with Single 5-V Supply

additional features of SN55121, SN75121 line drivers

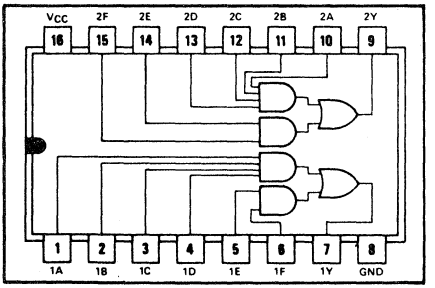
- Plug-In Replacement for Signetics 8T13
- 2.4-V Output at I_{OH} = −75 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- High Speed . . .Maximum Propagation Delay Time = 20 ns

additional features of SN55122, SN75122 line receivers

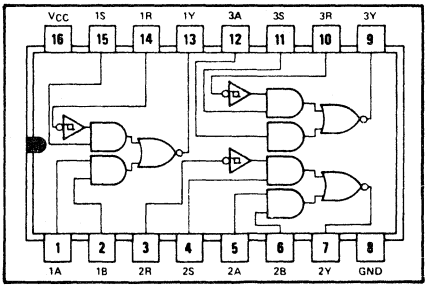
- Plug-In Replacement for Signetics 8T14
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Fanout to 10 Series 54/74 Standard Loads

5

SN55121, SN75121
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55122, SN75122
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN55121, SN75121 dual line drivers and the SN55122, SN75122 triple line receivers are designed for digital data transmission over lines having impedances from 50 to 500 ohms. They are also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN55121, SN75121 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 volts. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55122, SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of −0.15 volt with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs which, if both are high, will hold the output low. The third receiver has only an A input which, if high, will hold the output low.

SN55121, SN75121 FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

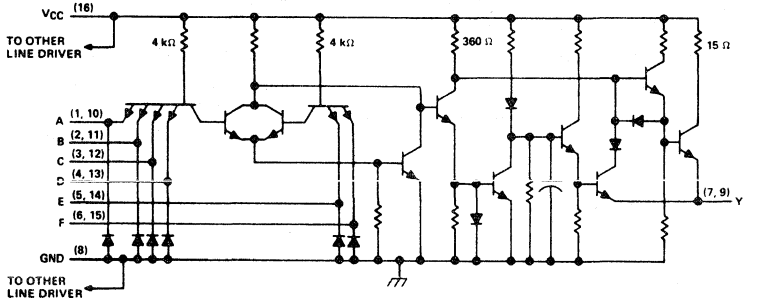
H = high level
L = low level
X = irrelevant

SN55122, SN75122 FUNCTION TABLE

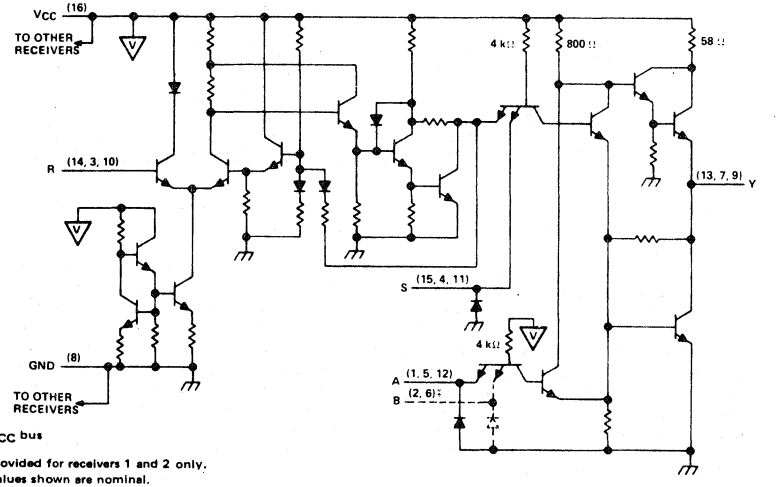
INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

†B input and last two lines of the function table are applicable to receivers 1 and 2 only.

SN55121, SN75121 schematic (each driver)



SN55122, SN75122 schematic (each receiver)



▽ . . . VCC bus

‡B input is provided for receivers 1 and 2 only.
Resistor values shown are nominal.

SN55121, SN75121 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Input voltage . . . . . 6 V
Output voltage . . . . . 6 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1 W
Operating free-air temperature range: SN55121 . . . . . −55°C to 125°C
SN75121 . . . . . 0°C to 75°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

SN55121,,SN75121 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−75	mA
Operating free-air temperature, T_A: SN55121	−55		125	°C
SN75121	0		75	°C

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SN55121, SN75121 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 5 V, I_I = −12 mA		−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V, I_I = 10 mA	5.5		V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −75 mA, See Note 3	2.4		V
I_{OH}	High-level output current	V_{CC} = 5 V, V_{IH} = 4.5 V, V_{OH} = 2 V, T_A = 25°C, See Note 3	−100	−250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V, V_{OL} = 0.4 V, See Note 3		−800	μA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V, V_O = 3 V		500	μA
I_{IH}	High-level input current	V_I = 4.5 V		40	μA
I_{IL}	Low-level input current	V_I = 0.4 V	−0.1	−1.6	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5 V, T_A = 25°C		−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, All inputs at 2 V, Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, All inputs at 0.8 V, Outputs open		60	mA

‡Not more than one output should be shorted at a time.

SN55121, SN75121 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 15 pF, See Figure 1		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 1000 pF, See Figure 1		22	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	50	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55121 chips are alloy-mounted; SN75121 chips are glass-mounted.
3 The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

SN55122, SN75122 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Input voltage: R input . . . . . 6 V
A, B, or S input . . . . . 5.5 V
Output voltage . . . . . 6 V
Output current . . . . . ±100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6) . . . . . 1 W
Operating free-air temperature range: SN55122 . . . . . −55°C to 125°C
SN75122 . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

SN55122, SN75122 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−500	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A: SN55122	−55		125	°C
SN75122	0		75	°C

SN55122, SN75122 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	A,B,R, or S		2			V
V_{IL}	Low-level input voltage	A,B,R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis†	R	V_{CC} = 5 V, T_A = 25°C	0.3	0.6		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V, I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V, I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = 0 V, V_{IL} = 0.8 V, I_{OH} = −500 μA, See Note 3	2.6			V
			$V_{I(A)}$ = 0 V, $V_{I(B)}$ = 0 V, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (See Note 4), I_{OH} = −500 μA	2.6			
V_{OL}	Low-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA, See Note 3			0.4	V
			$V_{I(A)}$ = 0 V, $V_{I(B)}$ = 0 V, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (See Note 5), I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V			40	μA
		R	V_I = 3.8 V			170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25 V			72	mA

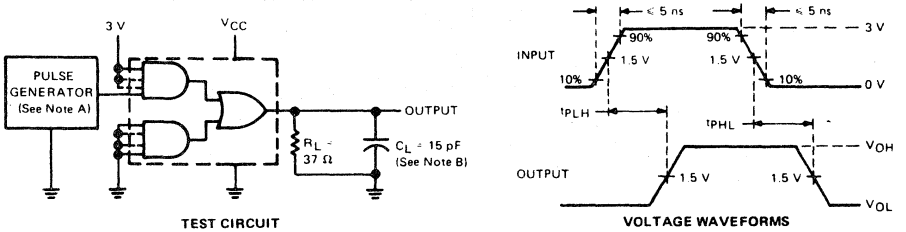
†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
‡Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 1. Voltage values are with respect to network ground terminal.
3. The output voltage limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.
4. Receiver input was at a high level immediately before being reduced to 1.45 V.
5. Receiver input was at a low level immediately before being raised to 1.45 V.
6. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55122 chips are alloy-mounted; SN75122 chips are glass-mounted.

SN55122, SN75122 switching characteristics, V_{CC} = 5 V, T_A = 25°C

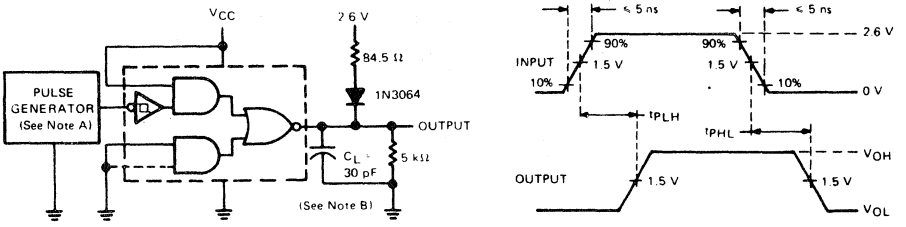
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from R input	See Figure 2		20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT — VOLTAGE WAVEFORMS

FIGURE 1–SN55121, SN75121 SWITCHING TIMES



TEST CIRCUIT — VOLTAGE WAVEFORMS

FIGURE 2–SN55122, SN75122 SWITCHING TIMES

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, t_w = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

SN55121, SN75121

OUTPUT CURRENT vs OUTPUT VOLTAGE

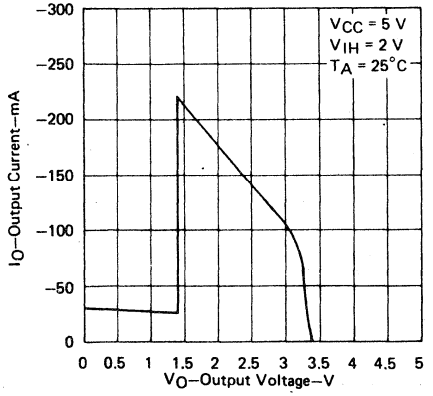


FIGURE 3

SN55122, SN75122

OUTPUT VOLTAGE vs INPUT VOLTAGE

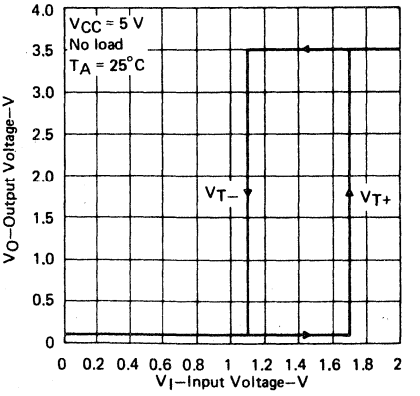


FIGURE 4

TYPICAL APPLICATION DATA

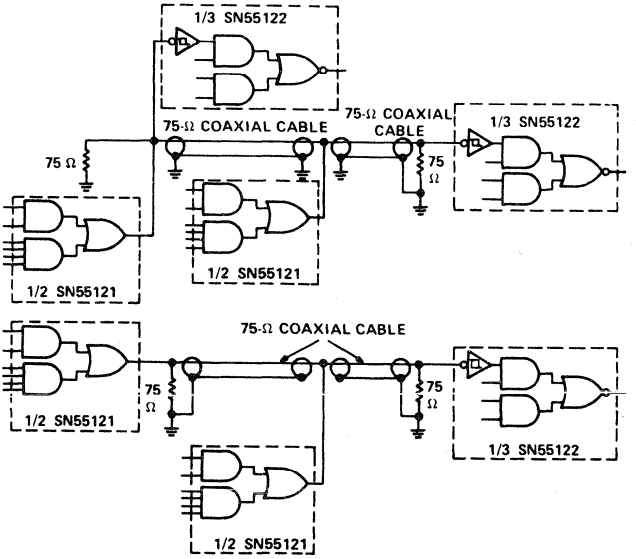
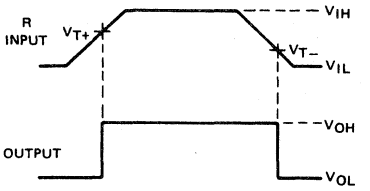


FIGURE 5–SINGLE-ENDED PARTY LINE CIRCUITS



The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring up pulses.

FIGURE 6–PULSE SQUARING

TYPES SN75123, SN75124
DUAL LINE DRIVER AND TRIPLE LINE RECEIVER

BULLETIN NO. DL-S 12043, SEPTEMBER 1973–REVISED APRIL 1974

LINE CIRCUITS

- Meet IBM System 360 Input/Output Interface Specifications
- Operate from Single 5-V Supply
- TTL Compatible

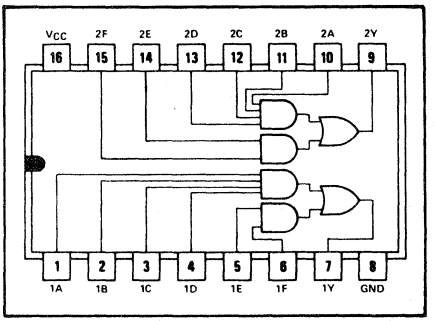
additional features of SN75123 line driver

- Plug-In Replacement for Signetics 8T23
- 3.11-V Output at I_{OH} = −59.3 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration

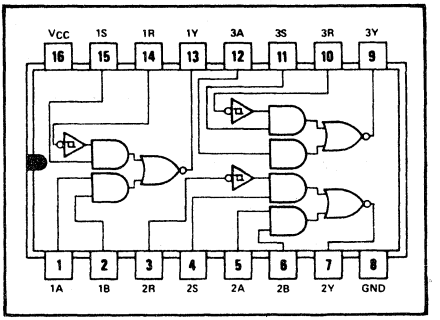
additional features of SN75124 line receiver

- Plug-In Replacement for Signetics 8T24
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility

SN75123
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



SN75124
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75123 dual line driver and the SN75124 triple line receiver are both specifically designed to meet the input/output interface specifications for IBM System 360. They are also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN75123 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 volts. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of −0.15 volt with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs which, if both are high, will hold the output low. The third receiver has only an A input which, if high, will hold the output low.

SN75123 FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

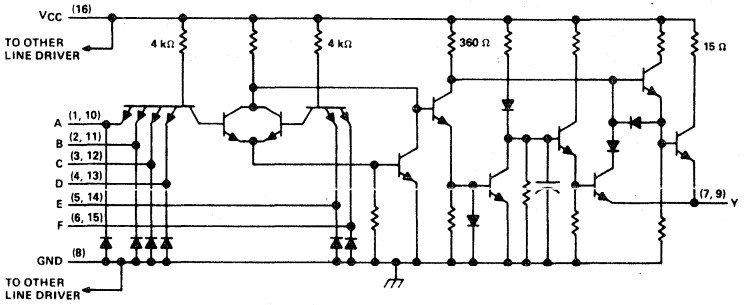
H = high level
L = low level
X = irrelevant

SN75124 FUNCTION TABLE

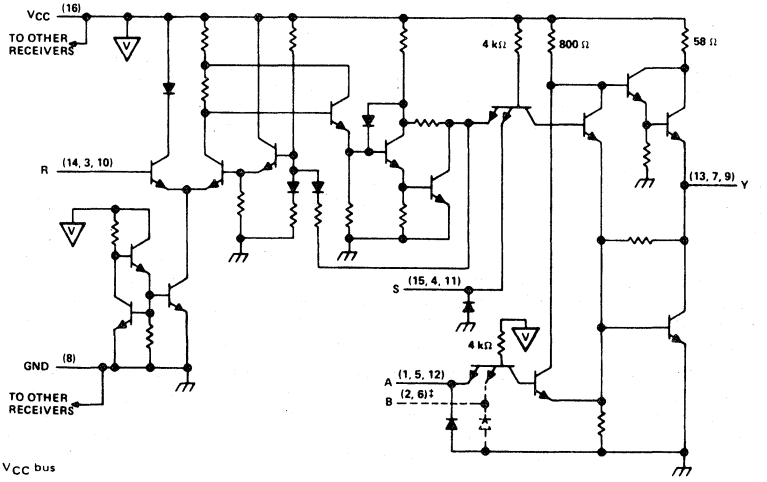
INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

†B input and last two lines of the function table are applicable to receivers 1 and 2 only.

SN75123 schematic (each driver)



SN75124 schematic (each receiver)



▽ . . . V_{CC} bus

‡B input is provided on receivers 1 and 2 only
Resistor values shown are nominal

SN75123 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Output voltage	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

SN75123 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−100	mA
Operating free-air temperature, T_A	0		75	°C

SN75123 electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 75°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA				−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{CC} = 5 V,	V_{IH} = 2 V,	T_A = 25°C	3.11			V
		I_{OH} = −59.3 mA,	See Note 3	T_A = 0°C to 75°C	2.9			
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100		−250	mA
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA, See Note 3				0.15	V
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V				40	μA
I_{IH}	High-level input current	V_I = 4.5 V					40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1		−1.6	mA
I_{OS}	Short-circuit output current ‡	V_{CC} = 5 V,	T_A = 25°C				−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, Outputs open	All inputs at 2 V,				28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, Outputs open	All inputs at 0.8 V,				60	mA

‡ Not more than one output should be shorted at a time.

SN75123 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 15 pF, See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 100 pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	25	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75123 chips are glass-mounted.
3. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

TYPE SN75124
TRIPLE LINE RECEIVER

SN75124 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R input with V_{CC} applied	7 V
R input with V_{CC} not applied	6 V
A, B, or S input	5.5 V
Output voltage	7 V
Output current	±100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

SN75124 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−800	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		75	°C

5

SN75124 electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 75°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	A,B, or S			2			V
		R			1.7			
V_{IL}	Low-level input voltage	A,B, or S					0.8	V
		R					0.7	
$V_{T+}-V_{T-}$	Hysteresis†	R	V_{CC} = 5 V,	T_A = 25°C	0.2	0.4		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V,	I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = V_{IH} min, See Note 3	V_{IL} = V_{IL}max, I_{OH} = −800 μA,	2.6			V
V_{OL}	Low-level output voltage		V_{IH} = V_{IH} min, See Note 3	V_{IL} = V_{IL}max, I_{OL} = 16 mA,			0.4	V
I_I	Input current at maximum input voltage	R	V_I = 7 V				5	mA
			V_I = 6 V,	V_{CC} = 0			5	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V				40	μA
		R	V_I = 3.11 V				170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V		−0.1		−1.6	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V,	T_A = 25°C	−50		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25 V				72	mA

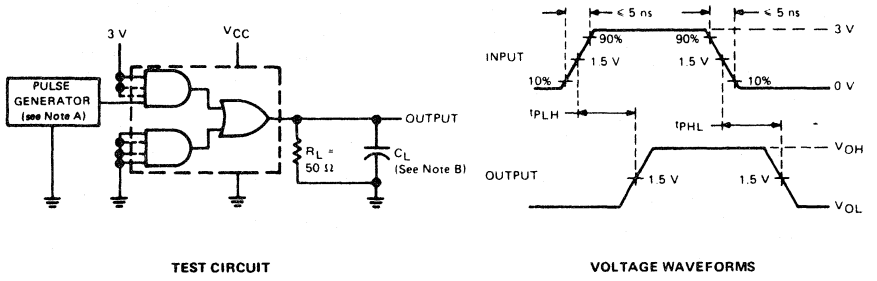
†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN75124 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 2		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

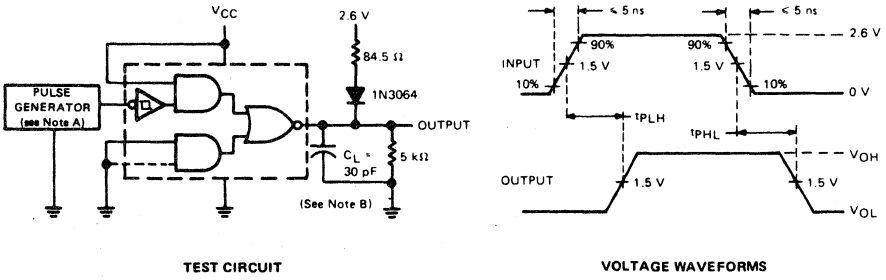
NOTES: 1. Voltage values are with respect to network ground terminal.
3. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75124 chips are glass-mounted.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1–SN75123 SWITCHING TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2–SN75124 SWITCHING TIMES

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_w = 200$ ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

SN75123
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

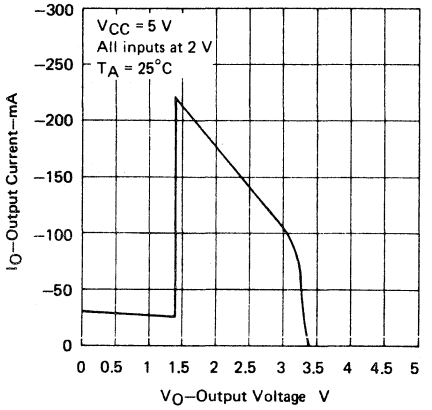


FIGURE 3

SN75124
OUTPUT VOLTAGE
vs
RECEIVER INPUT VOLTAGE

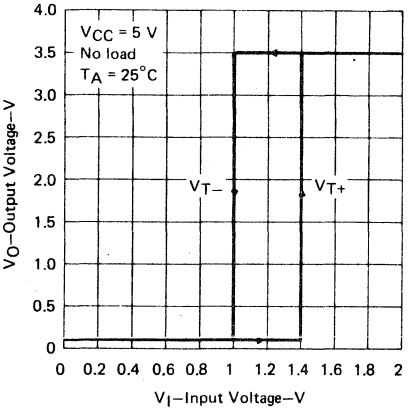


FIGURE 4

TYPICAL APPLICATION DATA

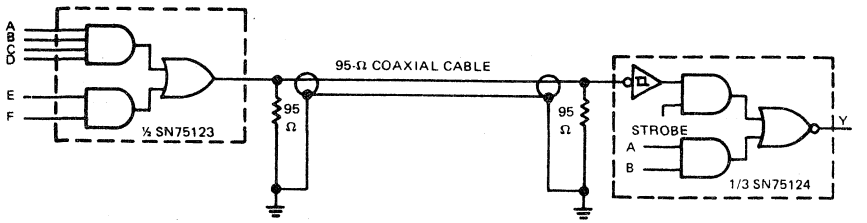


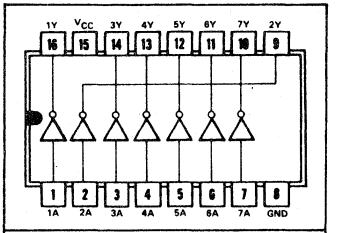
FIGURE 5–UNBALANCED LINE COMMUNICATION USING '123 AND '124

TYPES SN75125, SN75127
SEVEN-CHANNEL LINE RECEIVERS

BULLETIN NO. DL-S 12457, JANUARY 1977 – REVISED SEPTEMBER 1980

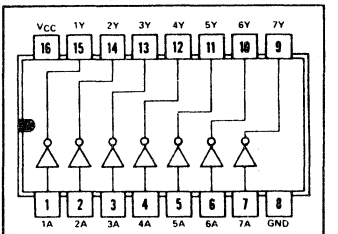
- Meets IBM 360/370 I/O Specification
- Input Resistance . . . 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors†
- Operates from Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low
- Seven Channels in one 16-Pin Package
- Standard V_{CC} and Ground Positioning on SN75127

SN75125
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: $Y = \overline{A}$

SN75127
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

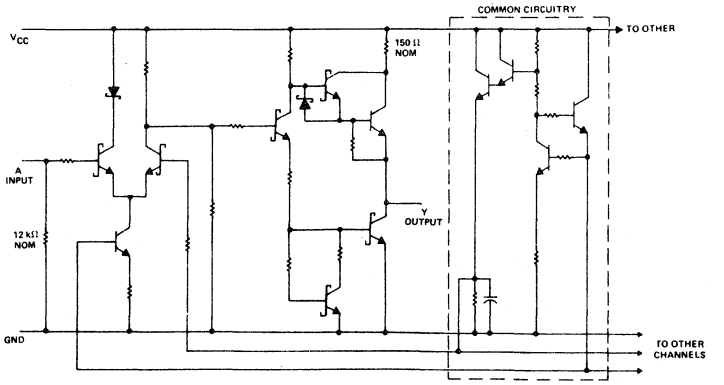


logic: $Y = \overline{A}$

description

The SN75125 and SN75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The SN75125 and SN75127 are characterized for operation from 0°C to 70°C.

schematic (each receiver)



†Integrated Schottky Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range: SN75125 . . . . . −0.15 V to 7 V
SN75127 . . . . . −2 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 800 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75125 and SN75127 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

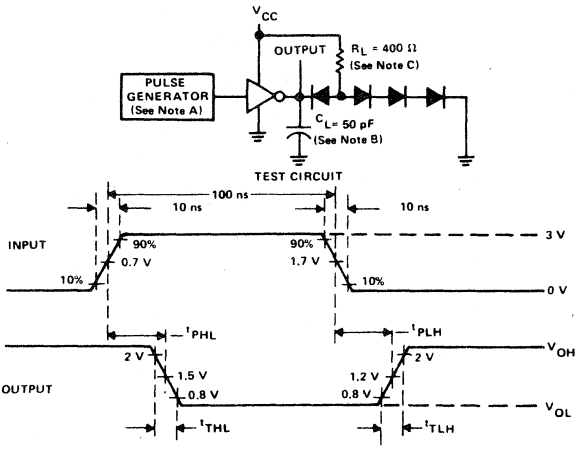
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1.7			V
V_{IL}	Low-level input voltage				0.7	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_I	Input resistance	V_{CC} = 4.5 V, 0 V, or open, ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V, I_{OH} = −0.4 mA, All inputs at 0.7 V		15	25	mA
		V_{CC} = 5.5 V, I_{OL} = 16 mA, All inputs at 4 V		28	47	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times		0.5	0.8	1.3	ns
t_{TLH}	Transition time, low-to-high-level output		1	7	12	ns
t_{THL}	Transition time, high-to-low-level output		1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

TYPICAL CHARACTERISTICS

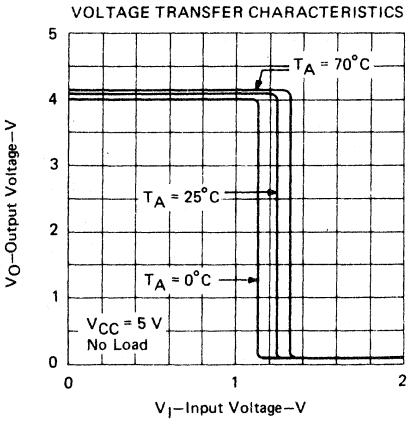


FIGURE 2

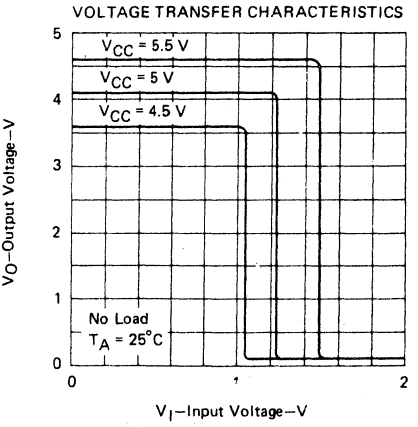


FIGURE 3

TYPICAL CHARACTERISTICS

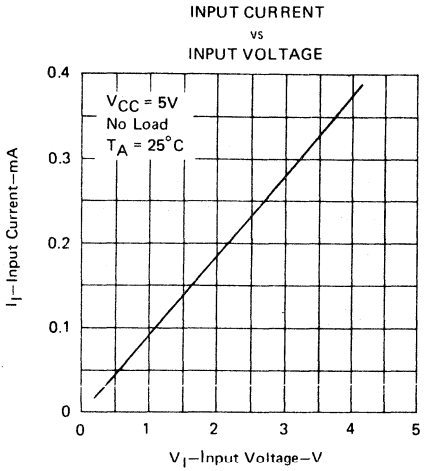


FIGURE 4

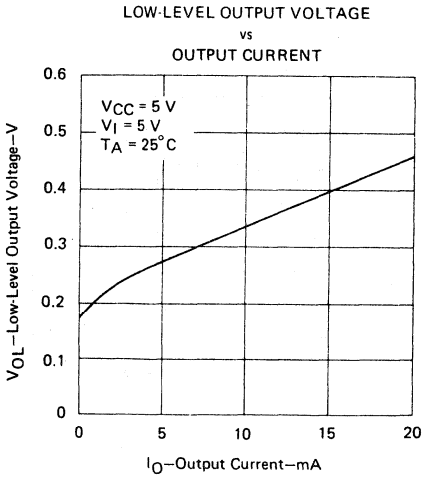


FIGURE 5

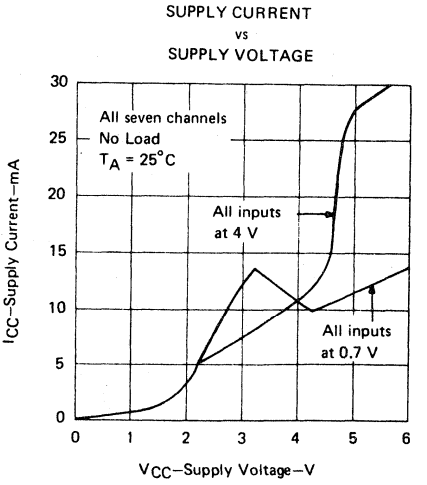


FIGURE 6

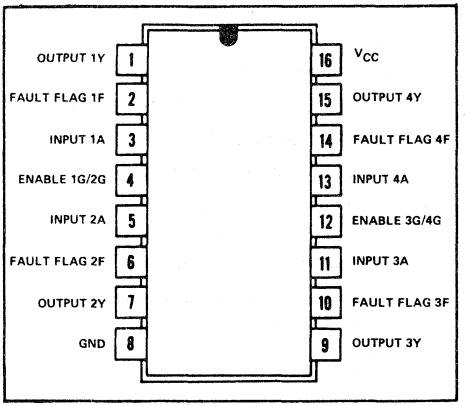
FUTURE PRODUCTS TO BE ANNOUNCED

TYPE SN75126 QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75130)
- Output Voltage of 3.11 V Min at I_{OH} = −60 mA
- Overload Protection with Foldback Current Limiting
- High-Speed, Low-Power Schottky Circuitry
- Functionally Interchangeable with MC 3481

J OR N PACKAGE
(TOP VIEW)

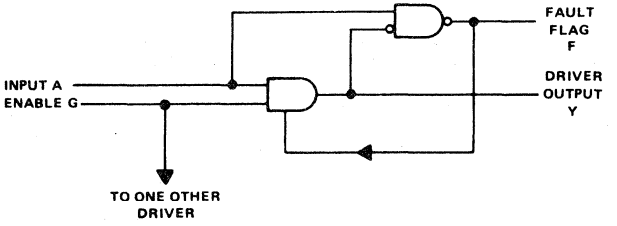


description

The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −60 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). This device is compatible with standard TTL logic and supply voltages. Fabrication techniques employ low-power-Schottky technology to achieve fast switching and low power dissipation. The data bus will not be disturbed during power up and power down. Fault flag circuitry is designed to sense a line short on any Y output line, output a logic low level, and reduce the output current to a safe level.

The SN75126 is designed for use with the SN75125 or SN75127 seven-channel receivers, or the SN75128 or SN75129 eight-channel receivers.

functional block diagram (one of four drivers, positive logic)



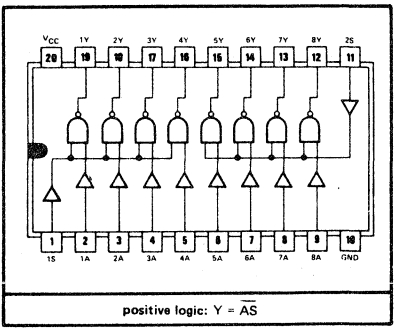
TYPES SN75128, SN75129
EIGHT-CHANNEL LINE RECEIVERS

BULLETIN NO. DL-S 12569, JANUARY 1977 – REVISED SEPTEMBER 1980

- Meets IBM 360/370 I/O Specification
- Input Resistance . . . . . 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors†
- Operates from a Single 5-Volt Supply
- High-Speed . . . Low Propagation Delay
- Ratio Specification . . . t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- SN75128 Strobe . . . Active-High
  SN75129 Strobe . . . Active-Low

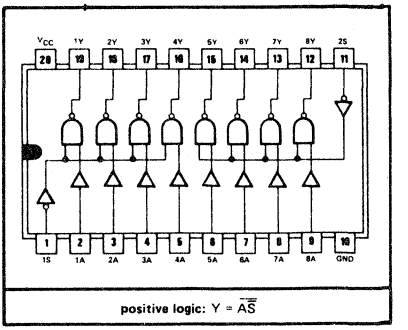
5

SN75128
J OR N DUAL IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AS}$

SN75129
J OR N DUAL IN-LINE PACKAGE
(TOP VIEW)



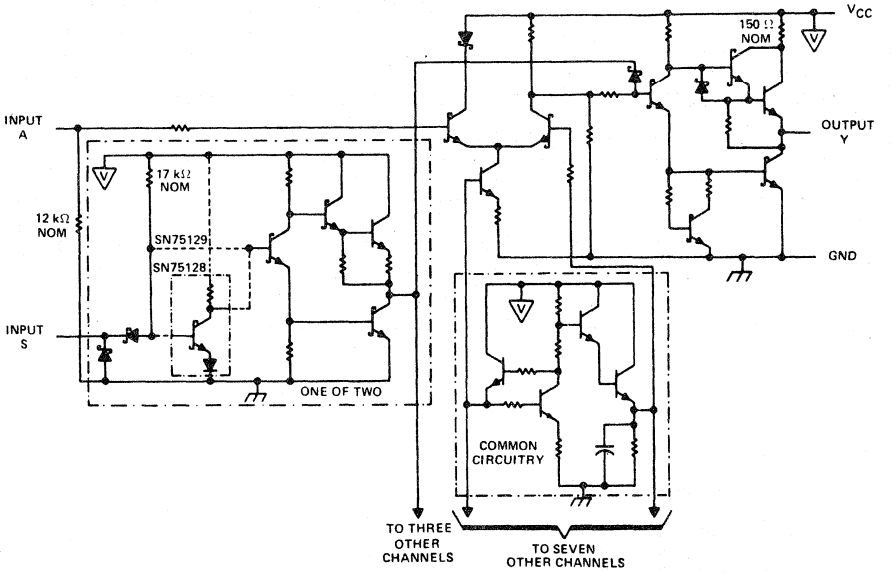
positive logic: $Y = \overline{AS}$

description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The SN75128 has an active-high strobe; the SN75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors† allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

schematic (each receiver)



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
A input voltage range	−0.15 V to 7 V
Strobe input voltage	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75128 and SN75129 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	A		1.7			V
		S		2			
V_{IL}	Low-level input voltage	A				0.7	V
		S				0.7	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V, I_I = −18 mA			−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
		S	V_{CC} = 5.5 V, V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
		S	V_{CC} = 5.5 V, V_I = 0.4 V			−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_I	Input resistance		V_{CC} = 4.5 V, 0 V, or open; ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 4 V		32	53	

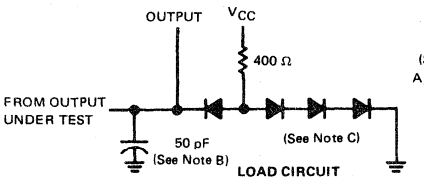
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

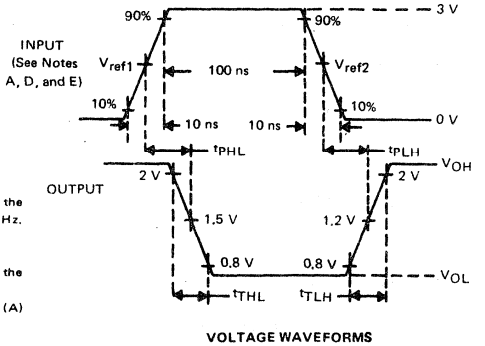
‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION





NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_o = 50 Ω, PRR = 5 MHz.
B. Includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in-phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

FIGURE 1

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

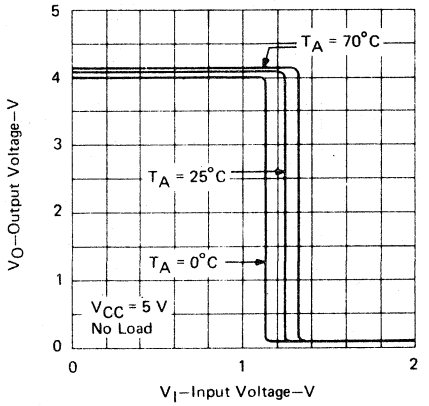


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS FROM A INPUTS

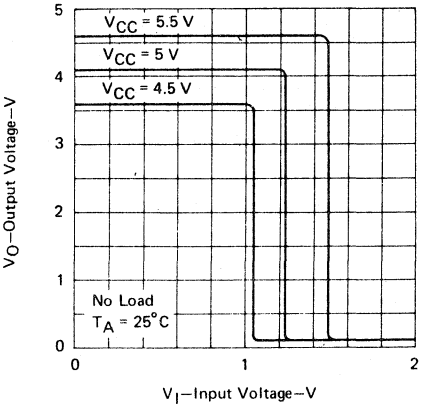


FIGURE 3

INPUT CURRENT vs INPUT VOLTAGE

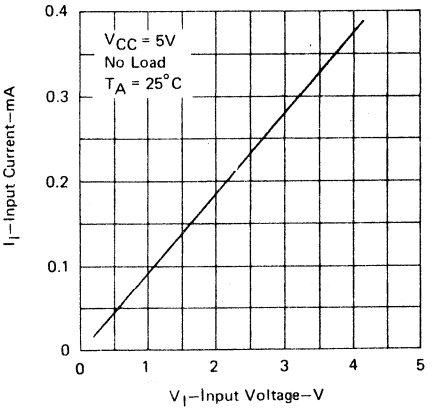


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

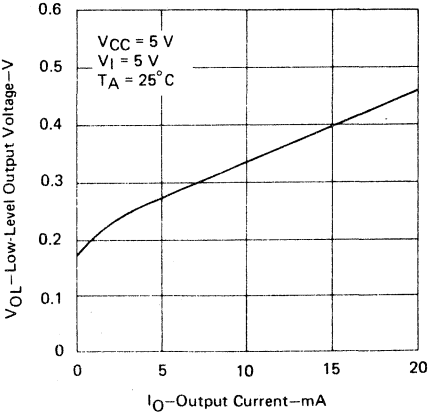


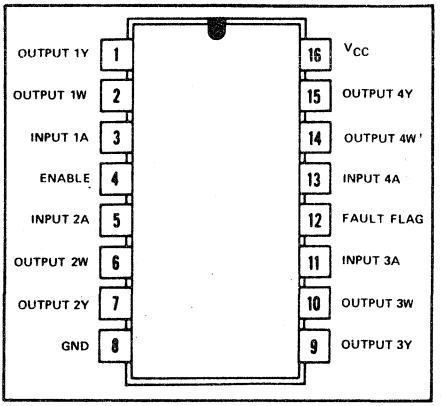
FIGURE 5

TYPE SN75130
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75126)
- Output Voltage of 3.11 V Min at I_{OH} = −60 mA
- Overload Protection with Foldback Current Limiting
- Common Enable and Common Fault Flag
- High-Speed, Low-Power Schottky Circuitry
- Functionally Interchangeable with MC 3485

J OR N PACKAGE
(TOP VIEW)

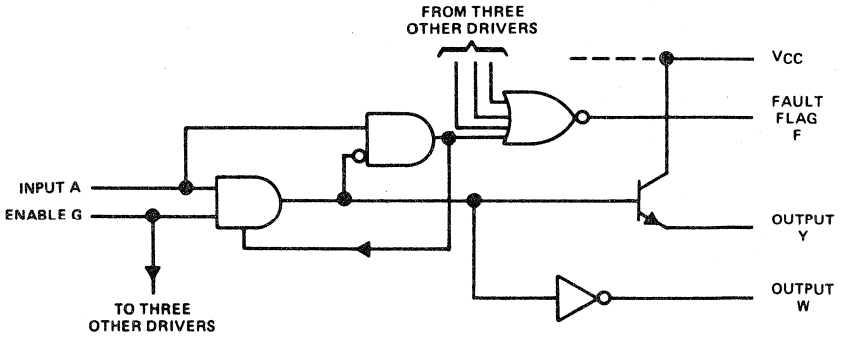


5

description

The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O Specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −60 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). This device is compatible with standard TTL logic and supply voltages. Fabrication techniques employ low-power Schottky technology to achieve fast switching and low power dissipation. The data bus will not be disturbed during power up and power down. Fault-flag circuitry is designed to sense a short on any of the Y output lines, output a logic low level, and reduce the output current on the shorted line to a safe level.

functional block diagram (one of four drivers, positive logic)

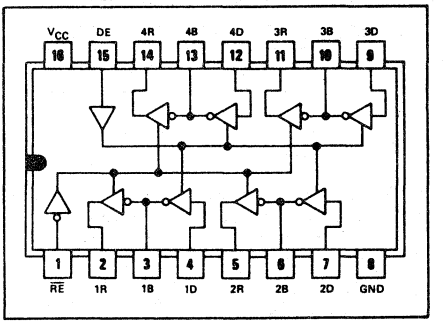


TYPE SN75136 QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12485, JANUARY 1977

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry†
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- 40-mA Current Sink Capability (Driver)
- Designed to be Functionally Interchangeable with Signetics N8T26

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

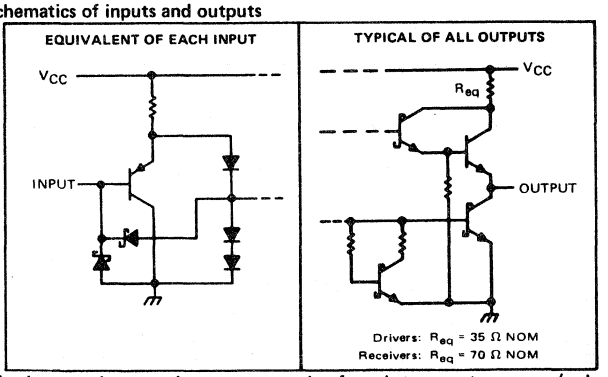


description

The SN75136 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have three-state outputs. With p-n-p inputs, the input loading is minimized to a maximum input current of 200 μA.

The SN75136 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE (DRIVER)

INPUTS		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

FUNCTION TABLE (RECEIVER)

INPUTS		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): N package	1150 mW
J package	1025 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75136 chips are glass-mounted.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver			−10	mA
	Receiver			−2	
Low-level output current, I_{OL}	Driver			40	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

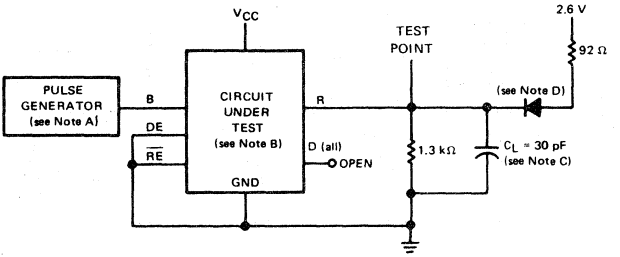
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$		2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$				0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V, I_{OH} = −2 mA	2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V, I_{OL} = 40 mA			0.5	V
		R	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V, $\overline{RE}$ at 2 V, V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V, V_O = 0.5 V			−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V			25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V			−200	μA
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V	−50		−150	mA
		R		−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load			87	mA

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

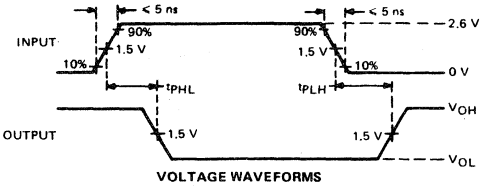
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	24	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		16	24	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		9	24	ns
t_{PZL}	Output enable time to low level					31	38	

PARAMETER MEASUREMENT INFORMATION

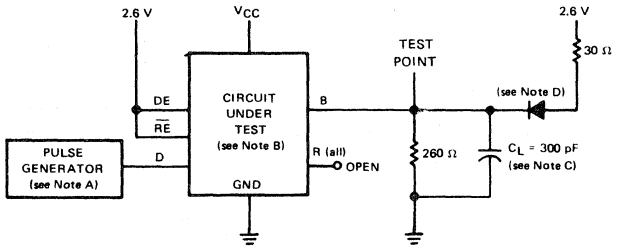


TEST CIRCUIT

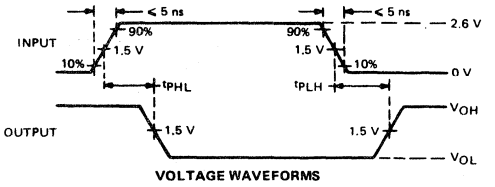


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT



TEST CIRCUIT

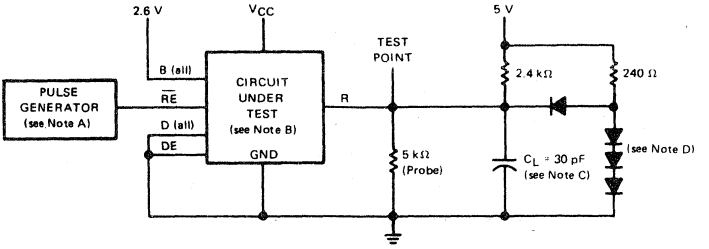


VOLTAGE WAVEFORMS

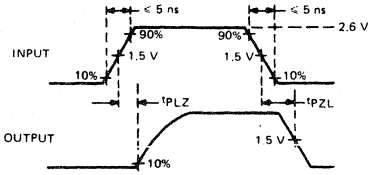
FIGURE 2–PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR = 10 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

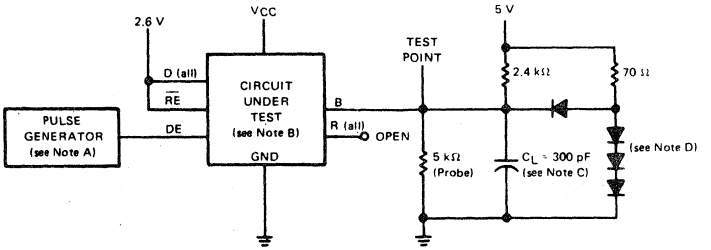


TEST CIRCUIT

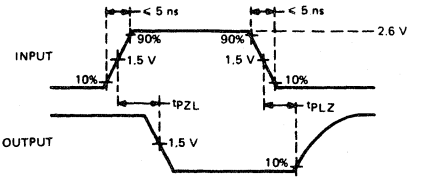


VOLTAGE WAVEFORMS

FIGURE 3–RECEIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR = 5 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

TYPES SN55138, SN75138
QUADRUPLE BUS TRANSCEIVERS

BULLETIN NO. DL-S 12046, SEPTEMBER 1973 – REVISED JANUARY 1977

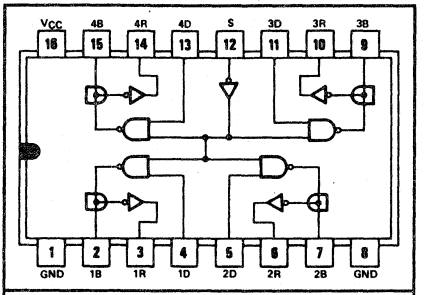
- Single 5-V Supply
- High-Input-Impedance, High-Threshold Receivers
- Common Driver Strobe
- TTL/DTL Compatible Driver and Strobe Inputs with Clamp Diodes
- High-Speed Operation
- 100-mA Open-Collector Driver Outputs
- Four Independent Channels
- TTL Compatible Receiver Output
- Available in Plastic or Ceramic 16-Pin Dual-In-Line Packages

description

The SN55138 and SN75138 quad bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver output is of the open-collector type, and is designed to handle loads of up to 100 milliamperes (50 ohms to 5 volts). The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 volts (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single five-volt supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero. The SN55138 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75138 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



Positive logic: $B = \overline{DS}$, $R = \overline{B}$
Each bus terminal, B, is a driver output and a receiver input.

FUNCTION TABLE (TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

FUNCTION TABLE (RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55138	SN75138	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Driver off-state output voltage		7	7	V
Low-level output current into the driver output		150	150	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1025	mW
	N package		1150	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package			260	°C

NOTES: 1. Voltage values are with respect to both ground terminals connected together.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55138 chips are alloy-mounted; SN75138 chips are glass-mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
High-level output current, I_{OH}	Receiver output			−400			−400	μA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	Driver or strobe			2			2			V
		Receiver			3.2			2.9			
V_{IL}	Low-level input voltage	Driver or strobe					0.8			0.8	V
		Receiver					1.5			1.8	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)} = V_{IL}$ max,	$V_{IH(S)}$ = 2 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} = MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)} = V_{IH}$ min, I_{OL} = 16 mA			0.4			0.4	
I_I	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	$V_I = V_{CC}$			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			−50			−50	μA
	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

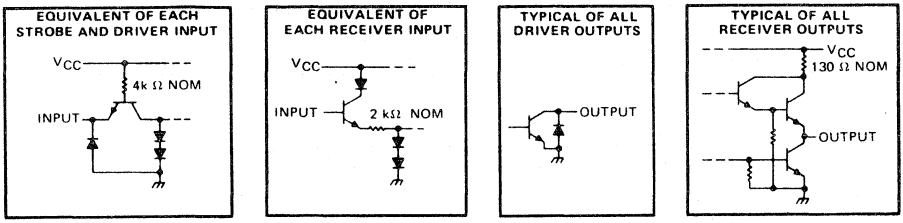
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

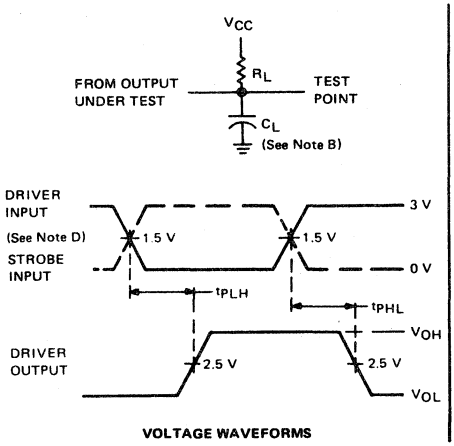
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, R_L = 50 Ω, See Figure 1		15	24	ns
t_{PHL}					14	24	
t_{PLH}	Strobe	Driver			18	28	ns
t_{PHL}					22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF, R_L = 400 Ω, See Figure 2		7	15	ns
t_{PHL}					8	15	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs

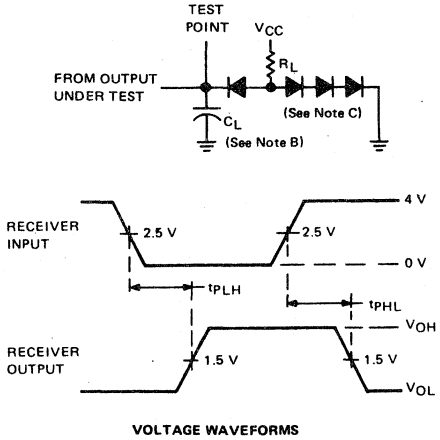


PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY TIMES FROM DATA AND STROBE INPUTS

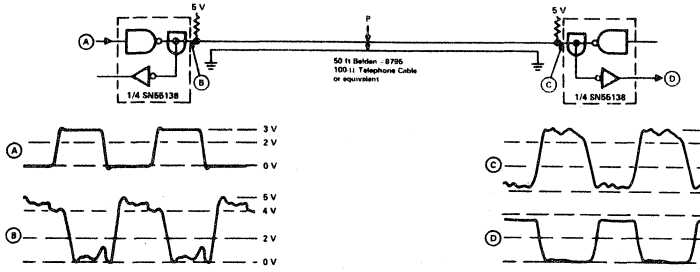


VOLTAGE WAVEFORMS

FIGURE 2–PROPAGATION DELAY TIMES FROM RECEIVER INPUT

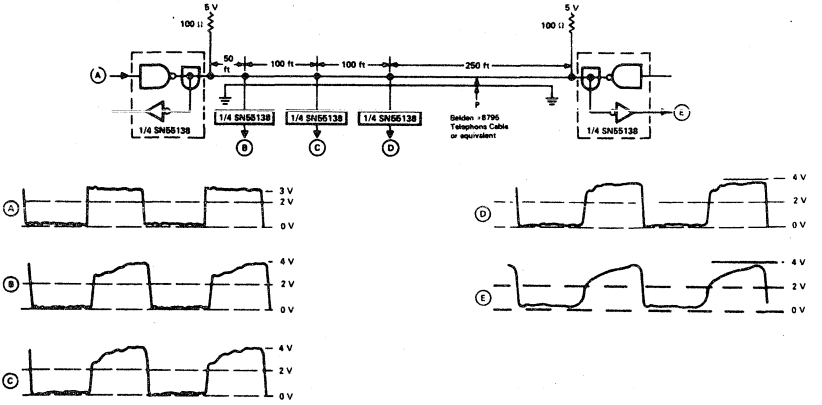
NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR = 1 MHz, t_r ≤10 ns, t_f ≤10 ns, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL APPLICATION DATA



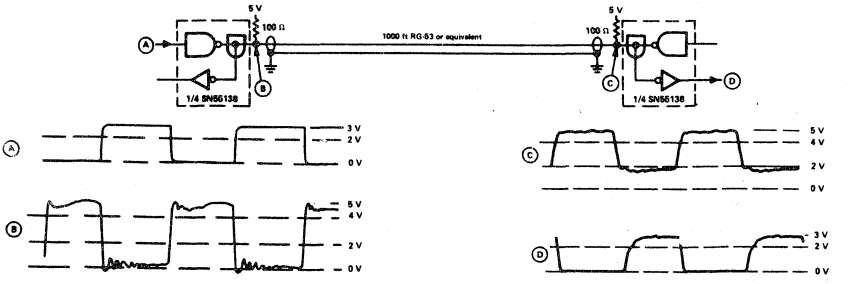
TYPICAL VOLTAGE WAVEFORMS

FIGURE 3–POINT-TO-POINT COMMUNICATION OVER 50 FEET OF TWISTED PAIR AT 5 MHz



TYPICAL VOLTAGE WAVEFORMS

FIGURE 4–PARTY-LINE COMMUNICATION ON 500 FEET OF TWISTED PAIR AT 1 MHz



TYPICAL VOLTAGE WAVEFORMS

FIGURE 5–POINT-TO-POINT COMMUNICATION OVER 1000 FEET OF COAX AT 1 MHz

TYPICAL CHARACTERISTICS†

DRIVER TRANSFER CHARACTERISTICS

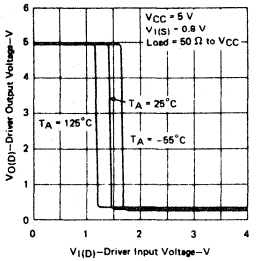


FIGURE 6

DRIVER TRANSFER CHARACTERISTICS

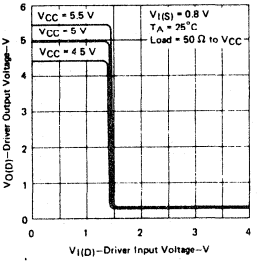


FIGURE 7

STROBE-TO-DRIVER-OUTPUT TRANSFER CHARACTERISTICS

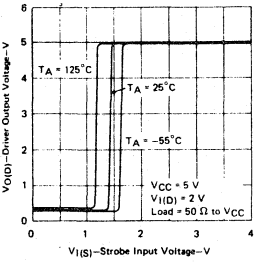


FIGURE 8

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

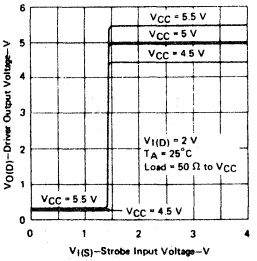


FIGURE 9

RECEIVER TRANSFER CHARACTERISTICS

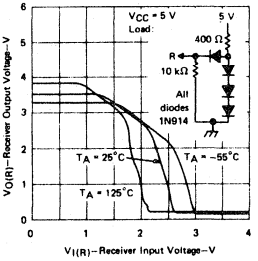


FIGURE 10

RECEIVER TRANSFER CHARACTERISTICS

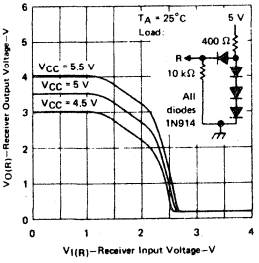


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

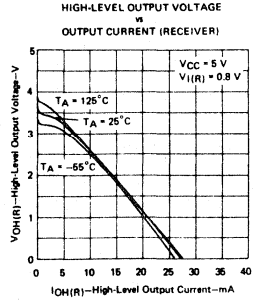


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

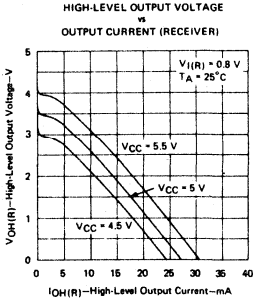


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

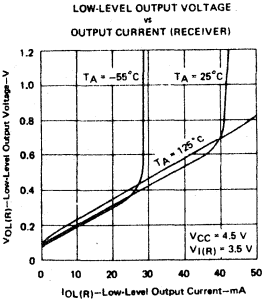


FIGURE 14

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (DRIVER OUTPUT)

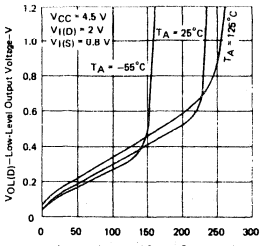


FIGURE 15

RECEIVER INPUT CURRENT vs RECEIVER INPUT VOLTAGE

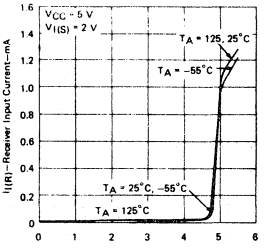


FIGURE 16

RECEIVER INPUT CURRENT vs RECEIVER INPUT VOLTAGE

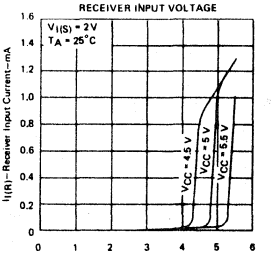


FIGURE 17

SUPPLY CURRENT vs SUPPLY VOLTAGE (ALL DRIVER OUTPUTS LOW)

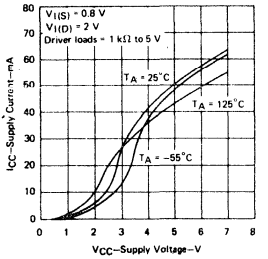


FIGURE 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

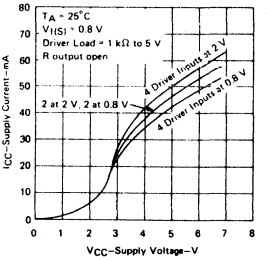


FIGURE 19

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

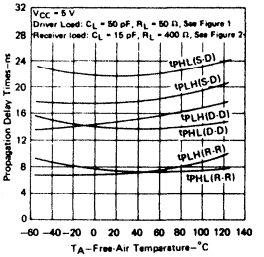


FIGURE 20

PROPAGATION DELAY TIMES vs SUPPLY VOLTAGE

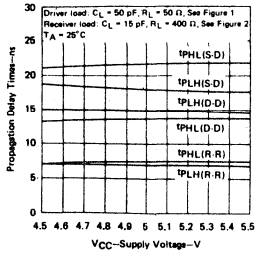


FIGURE 21

DRIVER PROPAGATION DELAY TIMES vs LOAD CAPACITANCE

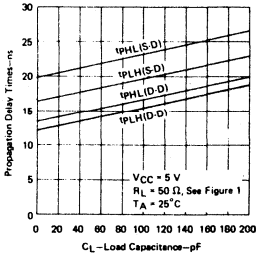


FIGURE 22

RECEIVER PROPAGATION DELAY TIMES vs LOAD CAPACITANCE

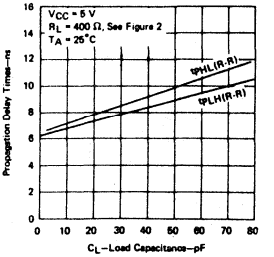


FIGURE 23

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPES SN55140, SN55141, SN55142A, SN55143A, SN75140, SN75141, SN75142A, SN75143A DUAL LINE RECEIVERS

BULLETIN NO. DL-S 12456, JANUARY 1977–REVISED JULY 1979

features common to all eight types

- Single 5-V Supply
- ±100 mV Sensitivity
- For Application As:
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications

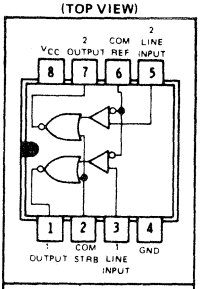
features of '140 and '141

- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

features of '142A and '143A

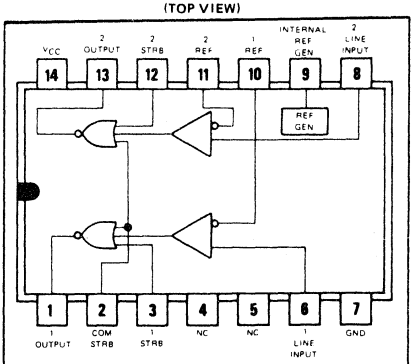
- Individual Reference Pins
- Common and Individual Strobes
- Internal 2.5-Volt Reference Available
- '143A Has Diode-Protected Input Stage for Power-Off Condition

SN55140, SN55141 . . .
JG DUAL-IN-LINE PACKAGE
SN75140, SN75141 . . .
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
see function table

SN55142A, SN55143A . . . J DUAL-IN-LINE PACKAGE
SN75142A, SN75143A . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

Pin 2, if unused, must be grounded when replacing '142 or '143 with '142A or '143A devices.

description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 volts to 3.5 volts, making it possible to optimize noise immunity for a given system design. A 2.5-volt internal reference is available for use on the '142A and '143A. Due to their low input current (less than 100 microamperes), they are ideally suited for party-line (bus-organized) systems.

The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected. Each receiver of the '142A has an individual reference voltage pin and an individual strobe. The '143A is the same as the '142A except that the input stage is diode protected. The internal reference voltage of the '142A and '143A can be externally adjusted with a single resistor from 1.5 volts to 3.5 volts.

'140, '141 FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	H
$> V_{ref} + 100$ mV	X	L
X	H	L

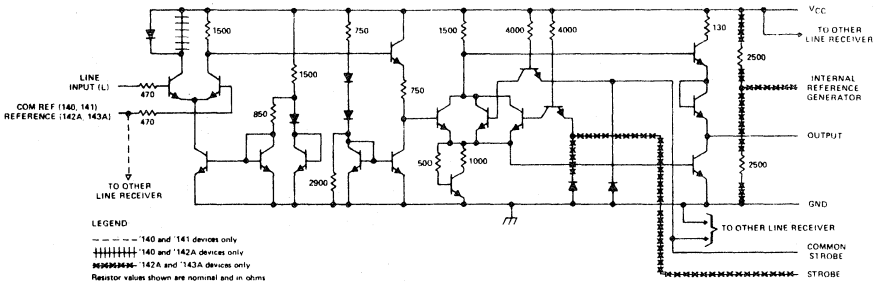
H = high level, L = low level, X = irrelevant

'142A, '143A FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	INDIVIDUAL STROBE	COMMON STROBE	OUTPUT
$\leq V_{REF} - 100$ mV	L	L	H
$\geq V_{REF} + 100$ mV	X	X	L
X	H	X	L
X	X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Reference input voltage, V_{ref} . . . . . 5.5 V
Line input voltage with respect to ground . . . . . −2 V to 5.5 V
Line input voltage with respect to V_{ref} . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: SN55′ Circuits . . . . . −55°C to 125°C
SN75′ Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package . . . . . 260°C

NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see the Dissipation Derating Table. In the J and JG package, these chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	600 mW	8.2 mW/°C	77°C
JG	600 mW	6.6 mW/°C	59°C
N	600 mW	9.2 mW/°C	85°C
P	600 mW	8.0 mW/°C	75°C

recommended operating conditions

		SN55′ CIRCUITS			SN75′ CIRCUITS			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
Reference input voltage, V_{ref}		1.5		3.5	1.5		3.5	V
Input voltage, V_I	Line	0		$V_{CC}-1$	0		$V_{CC}-1$	V
	Strobe	0		5.5	0		5.5	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

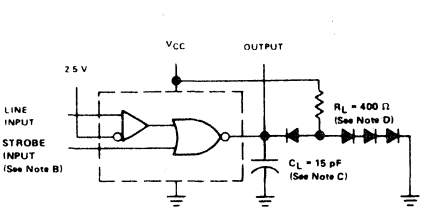
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IH(L)}$	High-level line input voltage			V_{ref} + 100			mV
$V_{IL(L)}$	Low-level line input voltage					V_{ref} − 100	mV
$V_{IH(S)}$	High-level strobe input voltage			2			V
$V_{IL(S)}$	Low-level strobe input voltage					0.8	V
V_{OH}	High-level output voltage		$V_{IL(L)}$ = V_{ref} − 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)}$ = V_{ref} + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{IL(L)}$ = V_{ref} − 100 mV, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA			0.4	
$V_{IK(S)}$	Strobe input clamp voltage		$I_{I(S)}$ = −12 mA			−1.5	V
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V			1	mA
		Com strb				2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V			40	μA
		Com strb				80	
		Line input	$V_{I(L)}$ = 3.5 V, V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0 V, V_{ref} = 3.5 V		35	100	
		Com ref			70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V			−1.6	mA
		Com strb				−3.2	
		Line input	$V_{I(L)}$ = 0 V, V_{ref} = 1.5 V			−10	μA
		Reference	$V_{I(L)}$ = 1.5 V, V_{ref} = 0 V			−10	
		Com ref				−20	
V_{gen}	Internal reference generator voltage‡	'142A, '143A	V_{CC} = 5 V, I_{gen} = 0	2.3	2.5	2.7	V
			V_{CC} = 5 V, I_{gen} = −70 μA		2.4		
I_{OS}	Short-circuit output current§		V_{CC} = 5.5 V	−18		−55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} − 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} + 100 mV		20	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time.

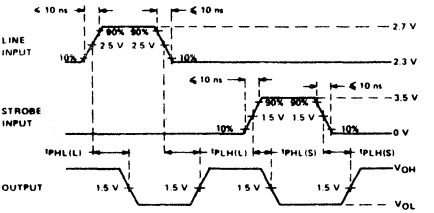
switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high-level output from line input	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low-level output from line input			22	30	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			8	15	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

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NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω.
B. Unused strobe(s) is (are) to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LINE INPUT VOLTAGE

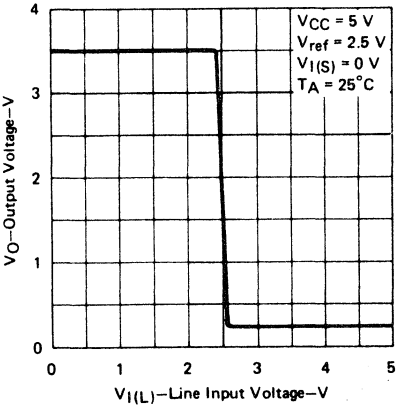
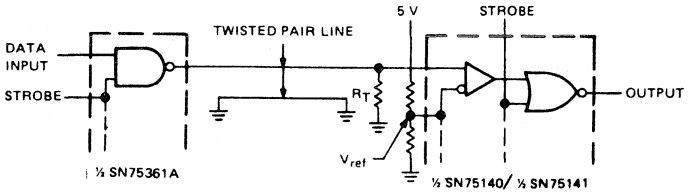


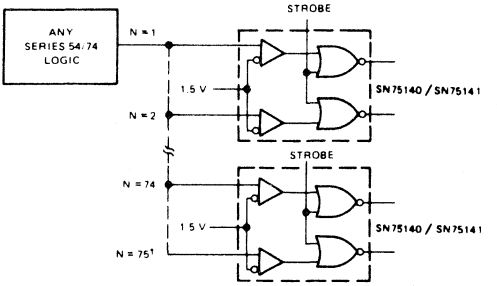
FIGURE 2

TYPICAL APPLICATION DATA

line receiver

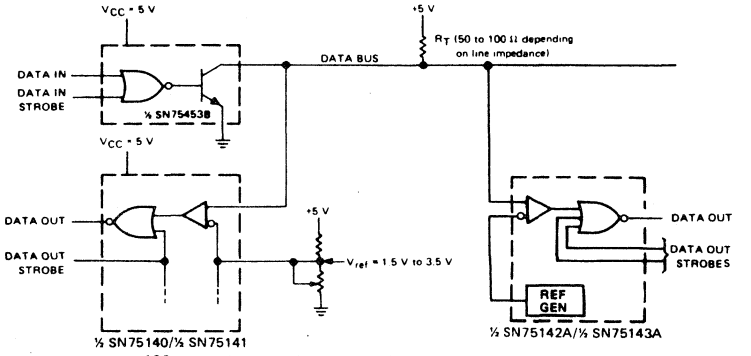


high fan-out from standard TTL gate



†Although most Series 54/74 circuits have a guaranteed 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

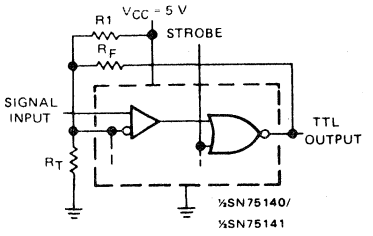
dual bus transceiver



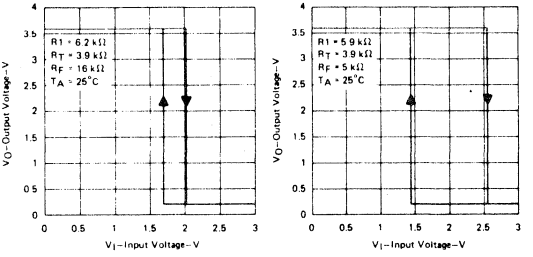
Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package, and only one power supply is required (+5 V). Data In and Data Out terminals are TTL compatible.

TYPICAL APPLICATION DATA

schmitt trigger



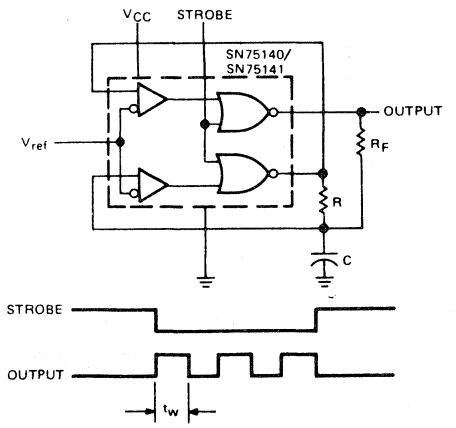
EXAMPLES OF TRANSFER CHARACTERISTICS



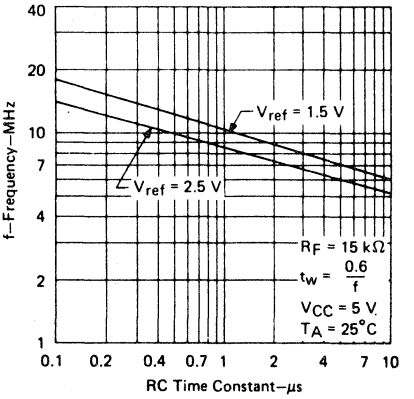
5

Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

gated oscillator

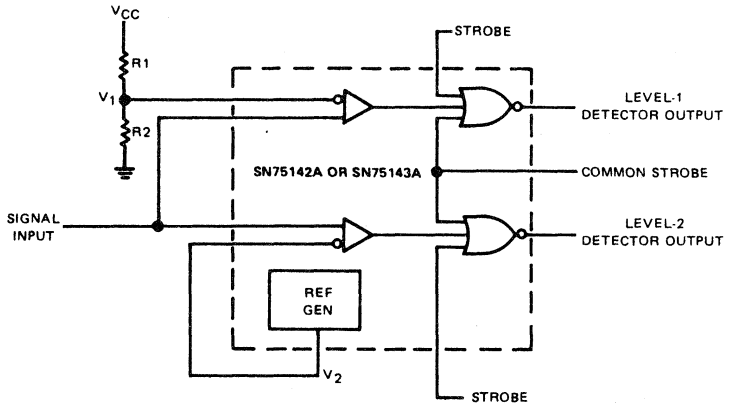


OSCILLATOR FREQUENCY
vs
RC TIME CONSTANT

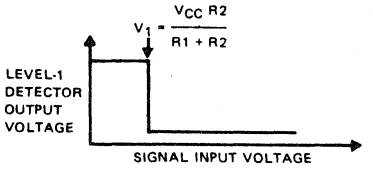


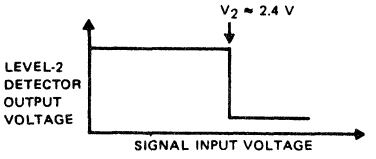
TYPICAL APPLICATION DATA

level detector



VOLTAGE TRANSFER CHARACTERISTICS WITH STROBES LOW



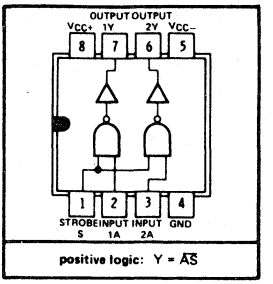


TYPE SN75150 DUAL LINE DRIVER

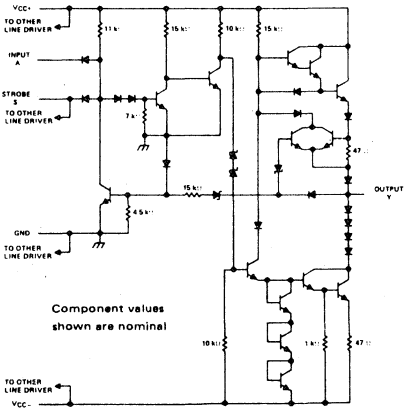
BULLETIN NO. DL-S 11428, JANUARY 1971 – REVISED JANUARY 1977

- Satisfies Requirements of EIA Standard RS-232-C
- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between −25 V and 25 V
- 2 μs Max Transition Time through the +3 V to −3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ±12 V

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematic (each line driver)



description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and −12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-}	−15 V
Input voltage	15 V
Applied output voltage	±25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG package	925 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75150 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	10.8	12	13.2	V
Supply voltage V_{CC-}	−10.8	−12	−13.2	V
Input voltage, V_I	0		5.5	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	2	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5	8		V
V_{OL}	Low-level output voltage (See note 3)	1	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8	−5	V
I_{IH}	High-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
				Strobe input		2	20	
I_{IL}	Low-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
				Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current‡	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2	8	mA
				V_O = −25 V		−3	−8	
				V_O = 0 V, V_I = 3 V	10	15	30	
				V_O = 0 V, V_I = 0 V	−10	−15	−30	
I_{CCH+}	Supply current from V_{CC+}, high-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0 V, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ, T_A = 25°C			8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	mA

NOTE 3: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

†All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

PARAMETER MEASUREMENT INFORMATION

d-c test circuits‡

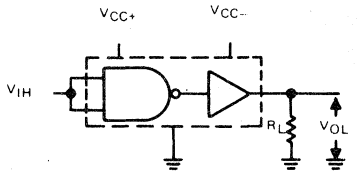
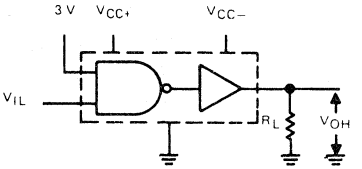
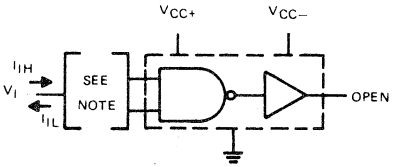


FIGURE 1–V_{IH}, V_{OL}



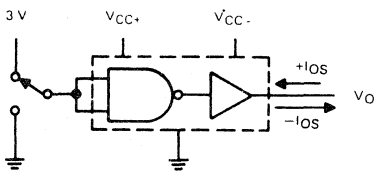
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_{IL}, the other input is open.

FIGURE 3–I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4–I_{OS}

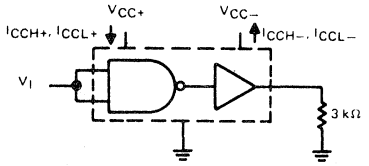
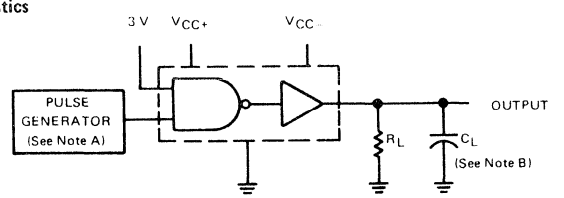


FIGURE 5–I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

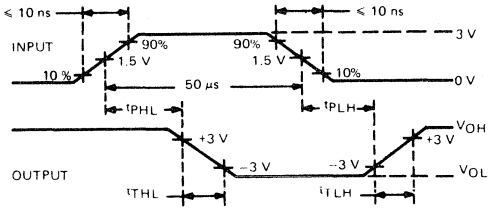
‡Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

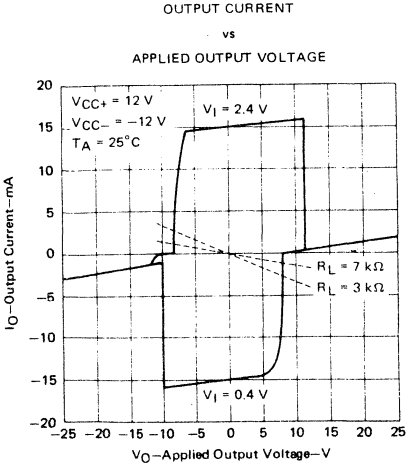


FIGURE 7

TYPICAL APPLICATION DATA

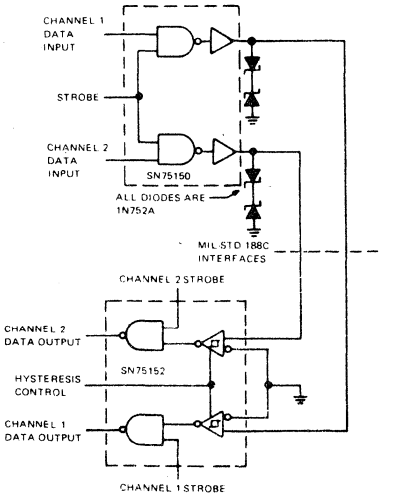


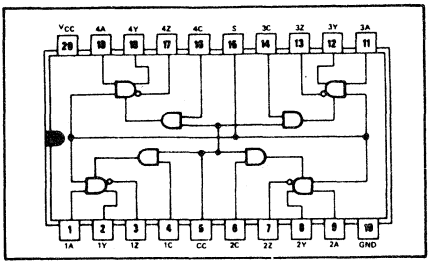
FIGURE 8–DUAL-CHANNEL SINGLE-ENDED INTERFACE CIRCUIT MEETING MIL-STD-188C, PARAGRAPH 7.2.

TYPES SN55151, SN55153, SN75151, SN75153 QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12629, DECEMBER 1978

- Meets EIA Standard RS-422A
- High-Impedance Output State for Party-Line Operation
- High Output Impedance in Power-Off Condition
- Low Input Current to Minimize Loading
- Single 5-V Supply
- 40-mA Sink- and Source-Current Capability
- High-Speed Schottky Circuitry
- Low Power Requirements

SN55151 . . . . J
SN75151 . . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



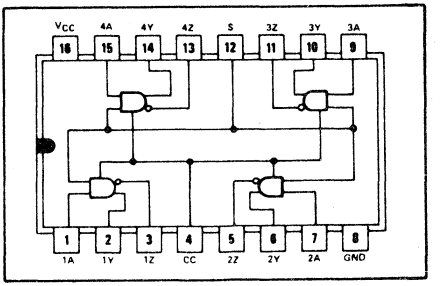
description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the '151 provides an additional enable input for each driver. The output circuits have active pull-up and pull-down and are capable of sinking or sourcing 40 milliamperes.

The '151 and '153 meet all requirements of RS-422A and Federal Standard 1020.

The SN55151 and SN55153 are characterized over the full military temperature range of −55°C to 125°C. The SN75151 and SN75153 are characterized for operation from 0°C to 70°C.

SN55153 . . . . J
SN75153 . . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

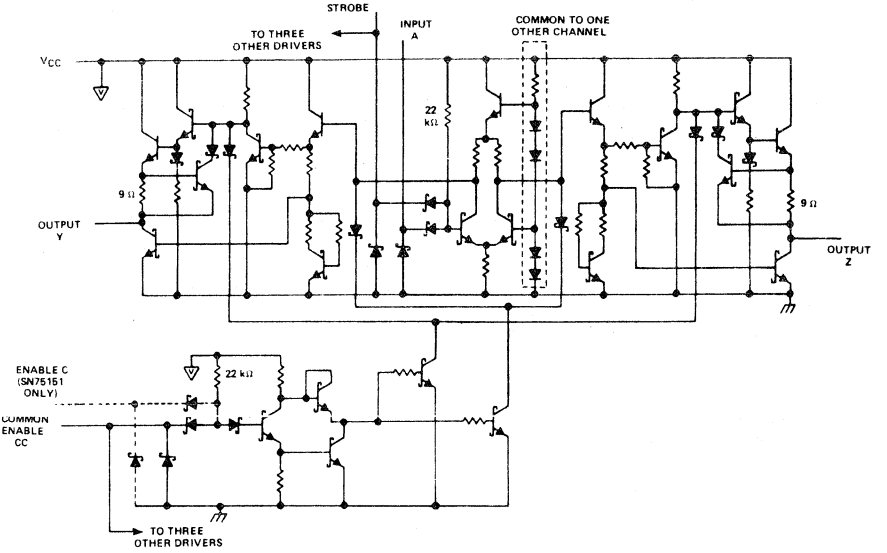


SN55151, SN75151
FUNCTION TABLE

INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

SN55153, SN75153
FUNCTION TABLE

INPUTS			OUTPUTS	
ENABLE CC	STROBE	DATA A	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55151, SN55153	−55°C to 125°C
SN75151, SN75153	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1, 6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1, 6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, SN55151 and SN55153 chips are alloy-mounted; SN75151 and SN75153 chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-mounted)	1000 mW	11 mW/°C	59°C
J (Glass-mounted)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode output voltage	−0.25		6	−0.25		6	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55'			SN75'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2			−2	V
			All others		−0.9	−1.5		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.4			2.5			V
			I_{OH} = −40 mA	2			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OL} = 40 mA			0.5			0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.4	$2V_{OD2}$		3.4	$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		2	2.8		V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4		±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.9	3		1.8	3	V
		V_{CC} = MIN			1.5	3		1.6	3	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4		±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−150			−20	µA
			V_O = 2.5 V			80			20	
			V_O = V_{CC}			150			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100		0.1	100	µA
			V_O = −0.25 V		−0.1	−100		−0.1	−100	
			V_O = −0.25 V to 6 V			±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C ('151), A			20			20	µA
			CC, S			80			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C ('151), A			−0.36			−0.36	mA
			CC, S			−1.6			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	outputs disabled		30	60		30	60	mA
			outputs enabled		60	80		60	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF See Figure 2, Termination B		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		12	20	ns
t_{THL}	Transition time, high-to-low-level output			12	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		13	30	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

PARAMETER MEASUREMENT INFORMATION

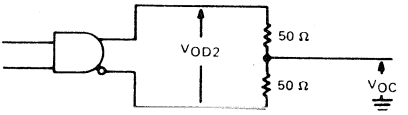
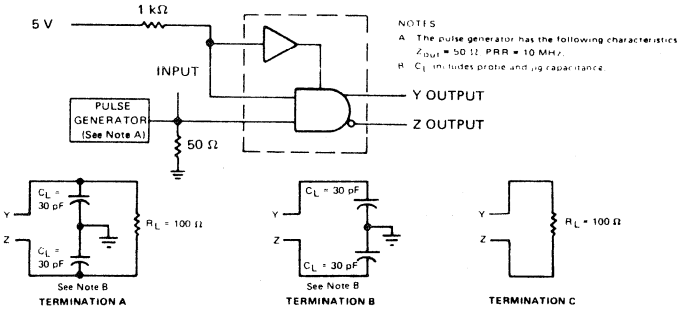
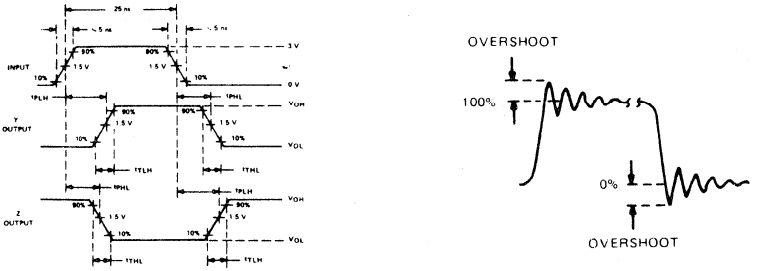


FIGURE 1—DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



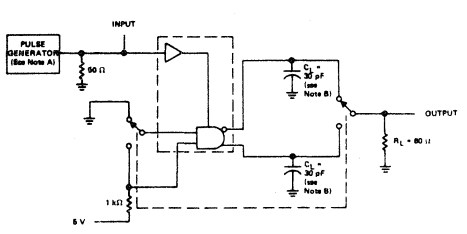
TEST CIRCUITS



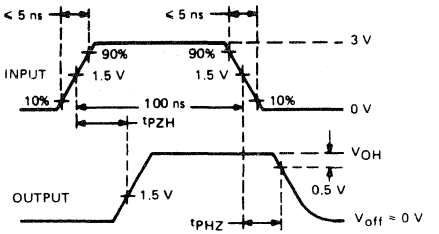
VOLTAGE WAVEFORMS

FIGURE 2—t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION

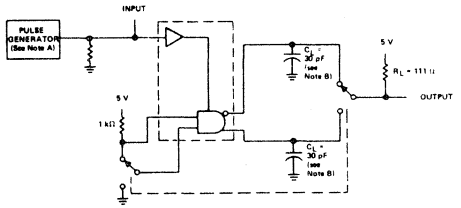


TEST CIRCUIT

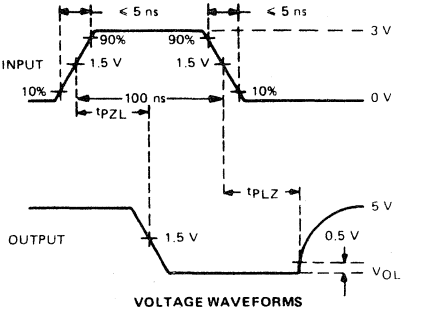


VOLTAGE WAVEFORMS

FIGURE 3–t_{PZH} AND t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

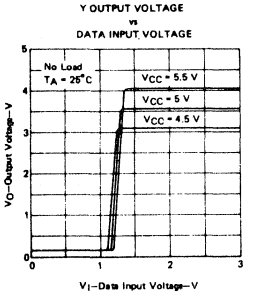


FIGURE 5

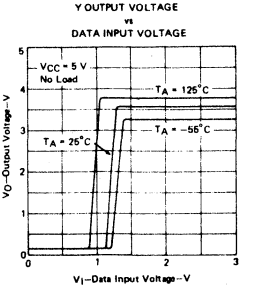


FIGURE 6

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

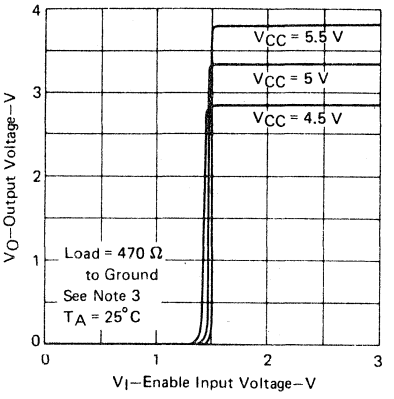


FIGURE 7

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

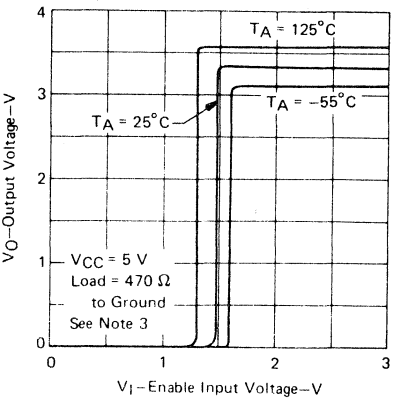


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

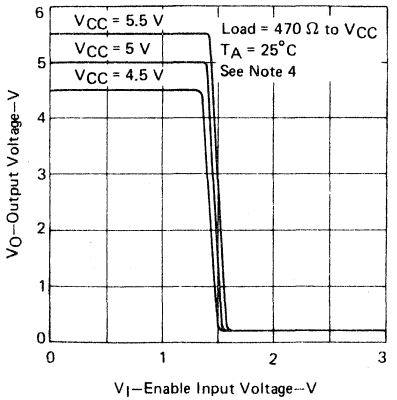


FIGURE 9

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

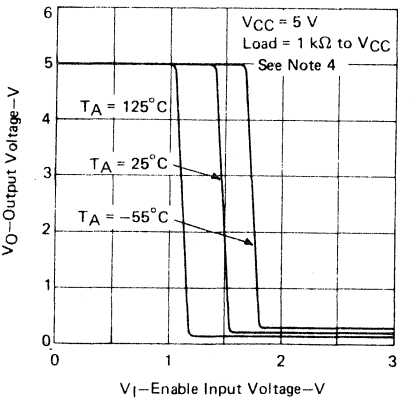


FIGURE 10

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

†Data for temperatures below 0°C and above 70°C are applicable to SN55151 and SN55153 circuits only.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

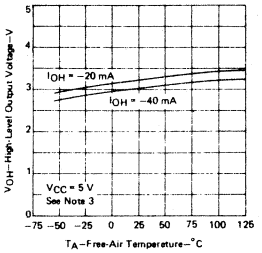


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

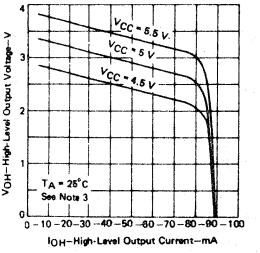


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

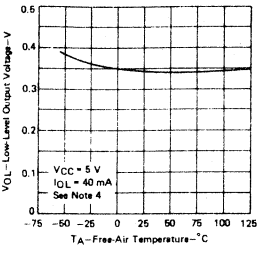


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

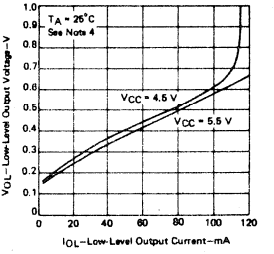


FIGURE 14

SUPPLY CURRENT vs SUPPLY VOLTAGE

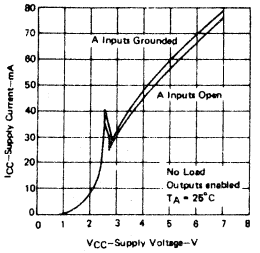


FIGURE 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

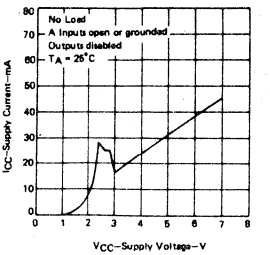


FIGURE 16

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

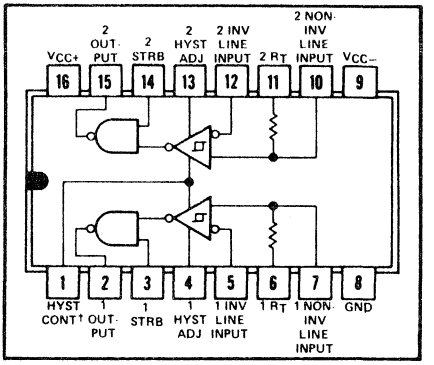
†Data for temperature below 0°C and above 70°C are applicable to SN55151 and SN55153 circuits only.

TYPE SN75152
DUAL LINE RECEIVER

BULLETIN NO. DL-S 11755, AUGUST 1972

- Meets Specifications of EIA RS-232-C or MIL-STD-188C†
- Dual Differential Receiver with Independent Strobes
- Common-Mode Input Voltage Range . . . ±25 V
- Differential Input Capability with One Input Grounded . . . ±25 V
- Continuously Adjustable Hysteresis with External Resistors
- Standard Supply Voltages . . . +12 V and −12 V
- Input Hysteresis (Double Thresholds) Remain Approximately Fixed for Power Supply and/or Temperature Variations

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



†To meet the specifications of EIA Standard RS-232-C, connect Hysteresis Control (Pin 1) to V_{CC-} (Pin 9). Also, connect pin 6 to pin 5 and pin 11 to pin 12. To meet the specifications of MIL-STD-188, leave Hysteresis Control (pin 1) and termination resistors (pin 6 and 11) open.

description

The SN75152 is a dual differential line receiver designed to meet the requirements of EIA standard RS-232-C or MIL-STD-188 interfaces. A single control (pin 1) sets the input hysteresis for the required operation. An added feature is the capability of adjusting the hysteresis to any voltage between ± 0.3 volt typical and ± 5 volts typical by means of the hysteresis adjust terminals (pin 4 and 13) making the SN75152 useful for a wide variety of line receiver and Schmitt trigger applications. The large common-mode input voltage range and differential input voltage (± 25 volts) give the circuit added versatility. The SN75152 is designed for operation from standard ± 12-volt supplies with ± 10% variation. Each receiver has an output strobe that is TTL compatible.

FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
H	H	H
L	H	L
X	L	H

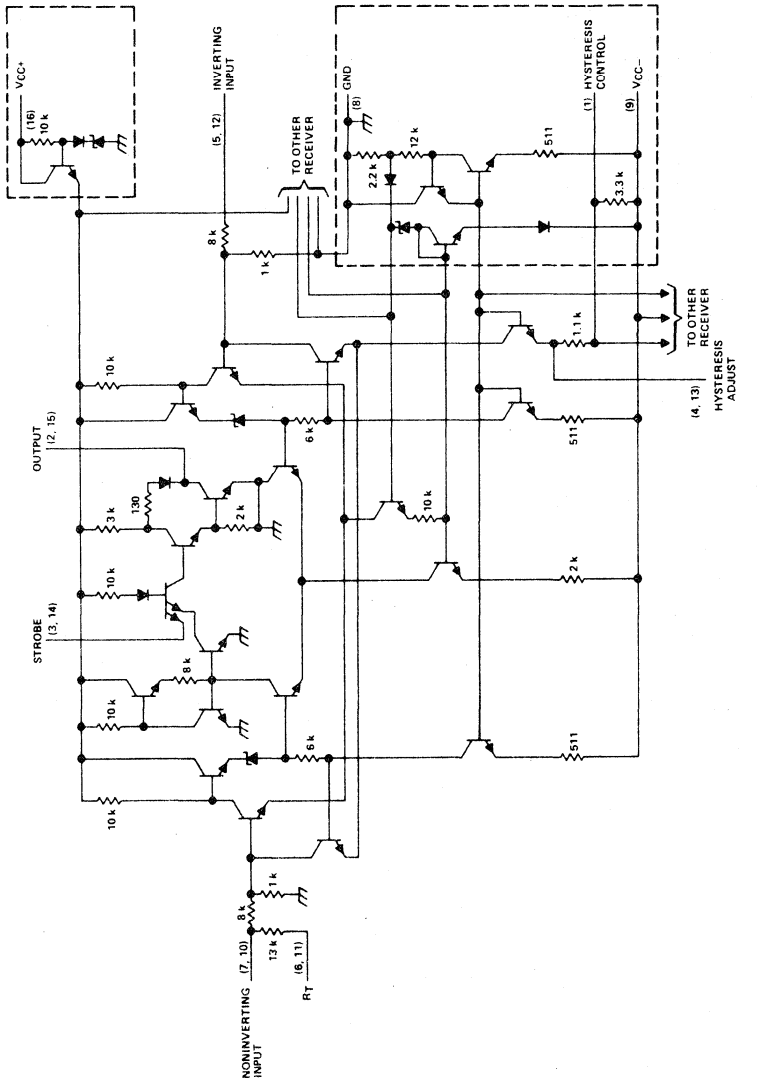
Definition of logic levels:

For the strobe: H (high) is any voltage between V_{IH} min and V_{CC}.
L (low) is any voltage between ground and V_{IL} max.

For the line input: H (high) is any differential input voltage (V_{ID})‡ more positive than V_{T-}, once the level of V_{T+} has been reached.
L (low) is any differential input voltage (V_{ID})‡ more negative than V_{T+}, once the level of V_{T-} has been reached.
X (irrelevant) is any input voltage permitted by maximum ratings.

‡Differential input voltages (V_T and V_{ID}) are at the noninverting input terminal with respect to the inverting input terminal.

schematic (each receiver)



Portions of circuit within dashed lines are common to both receivers.
Resistor values shown are nominal and in ohms.

5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Voltage at any line input with respect to other line input, ground, or R_T terminal	±25 V
R_T terminal voltage (see Note 1)	+25 V
Strobe input voltage (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V ± 10%, V_{CC-} = −12 V ± 10% (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
					(SEE NOTE 2)			
V_{T+}	Positive-going threshold voltage	See Figure 8 and Note 2	1	MIL-STD-188 Conditions	0.1	0.3	0.5	V
V_{T-}	Negative-going threshold voltage				−0.5	−0.3	−0.1	
V_{T+}	Positive-going threshold voltage		2	EIA RS-232-C Conditions	1.5	2.2	3	V
V_{T-}	Negative-going threshold voltage				−3	−2.2	−1.5	
V_{IH}	High-level input voltage at strobe		1		2			V
V_{IL}	Low-level input voltage at strobe		1				0.8	V
V_{OH}	High-level output voltage		1 and 2	V_{ID} = V_{T+} max, $V_{I(strobe)}$ = 2 V, I_{OH} = −500 μA	3	4.1	6	V
			1 and 2	V_{ID} = V_{T-} min, $V_{I(strobe)}$ = 0.8 V, I_{OH} = −500 μA	3	4.1	6	
V_{OL}	Low level output voltage		1 and 2	V_{ID} = V_{T-} min, $V_{I(strobe)}$ = 2 V, I_{OL} = 6.4 mA	0	0.15	0.4	V
I_I	Input current into strobe at maximum strobe voltage		3	$V_{I(strobe)}$ = 5.5 V		0.1	1	mA
I_{IH}	High-level strobe current		3	$V_{I(strobe)}$ = 2.4 V		30	80	μA
I_{IL}	Low-level strobe current		3	$V_{I(strobe)}$ = 0.4 V		−0.5	−1.5	mA
r_I	Input resistance	MIL-STD-188	4	$\lvert V_{ID} \rvert$ = 0 V to 25 V, R_T open	6	9		kΩ
		EIA RS-232-C	4	$\lvert V_{ID} \rvert$ = 3 V to 25 V, R_T connected to inverting line input	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		5			+1	±2	V
I_{OS}	Short-circuit output current		6	V_{ID} = 3 V		−1.9	−4	mA
I_{CC+}	Supply current from V_{CC+}		1	V_{ID} = −3 V, $V_{I(strobe)}$ = 2.4 V		10	16	mA
I_{CC-}	Supply current from V_{CC-}		1	V_{ID} = −3 V, $V_{I(strobe)}$ = 2.4 V		−7	−13	mA

‡Differential input voltages (V_T and V_{ID}) are at the noninverting line input terminal with respect to the inverting line input terminal.

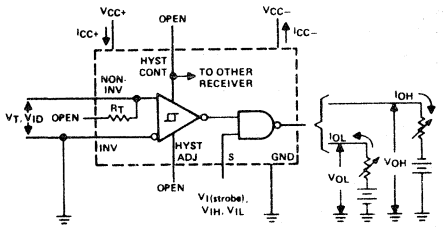
§Typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

NOTE 2: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only, e.g., when −0.1 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	7	C_L = 15 pF		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output				60		ns

PARAMETER MEASUREMENT INFORMATION



NOTE: Output is open for testing I_{CC+} and I_{CC-}

FIGURE 1–MIL-STD-188 CONDITION

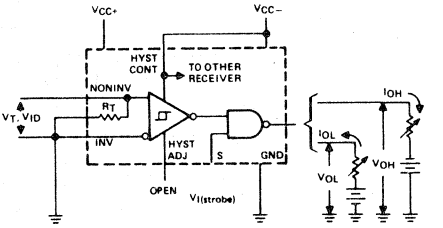


FIGURE 2–EIA RS-232-C CONDITION

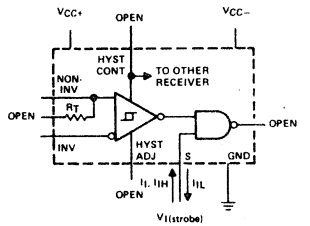


FIGURE 3

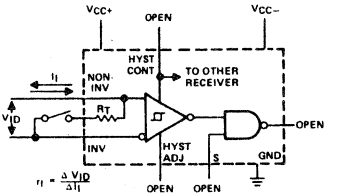


FIGURE 4

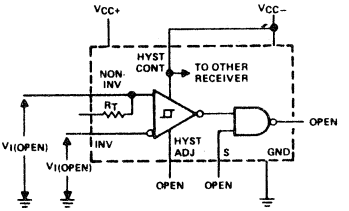


FIGURE 5

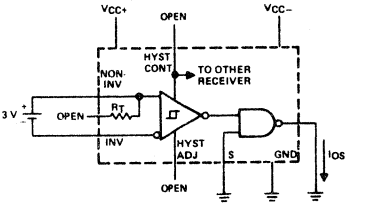
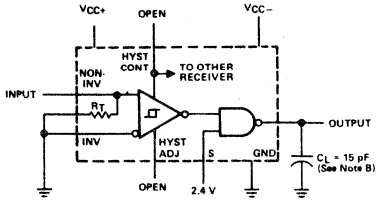
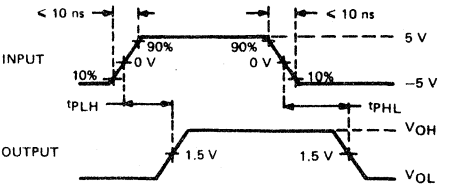


FIGURE 6



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 500 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 7–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

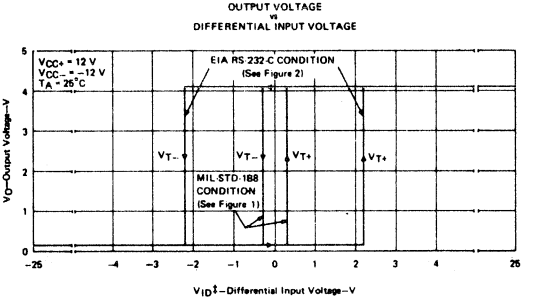


FIGURE 8

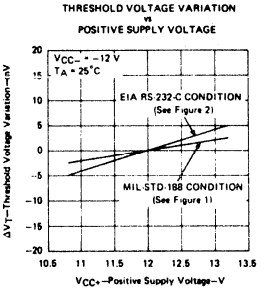


FIGURE 9

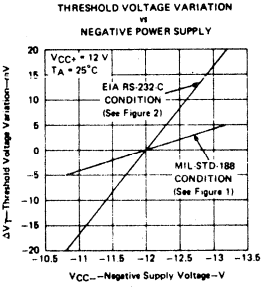


FIGURE 10

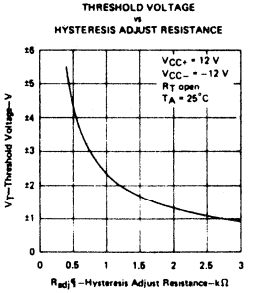


FIGURE 11

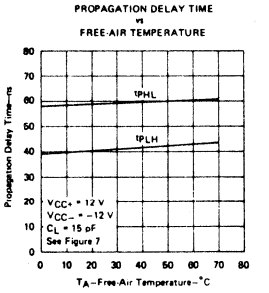


FIGURE 12

‡Differential input voltages (V_T and V_{ID}) are at the noninverting input terminal with respect to the inverting input terminal.
¶R_{adj} is connected between Hysteresis Adjust terminal and V_{CC-}.

TYPICAL APPLICATIONS

Some typical applications of the SN75152 are as follows:

- MIL-STD-188 Interface Receiver
- EIA RS-232-C Interface Receiver
- Single-Ended Line Receiver
- Differential Line Receiver
- High-Noise-Immunity Line Receiver
- Schmitt Trigger
- High-Voltage-Logic-to-TTL Translator
- MOS to TTL Converter
- Pulse Generator
- Threshold detector
- Pulse Shaper

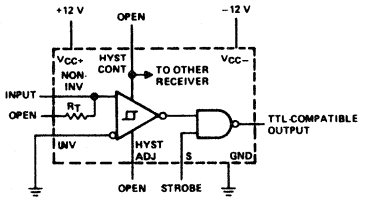
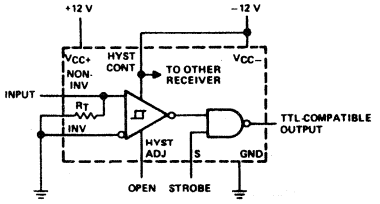
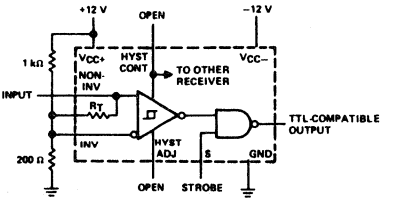


FIGURE 13—MIL-STD-188 SINGLE-ENDED LINE RECEIVER



NORMAL OPERATION



FAIL-SAFE OPERATION

FIGURE 14—EIA RS-232-C SINGLE-ENDED RECEIVER

TYPICAL APPLICATIONS

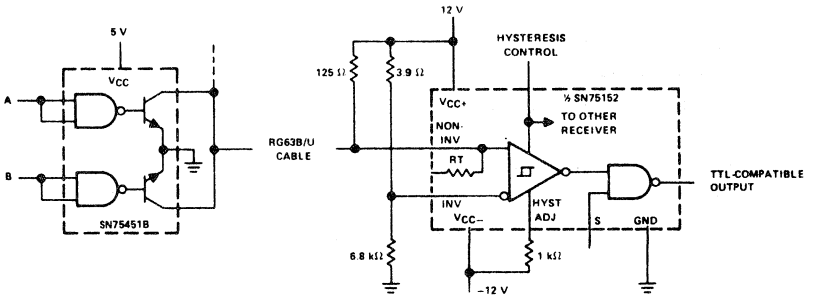
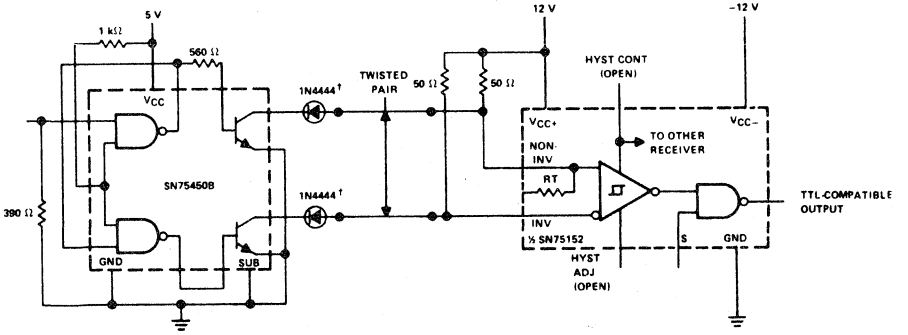


FIGURE 15–SINGLE-ENDED TRANSMITTER WITH DRIVER "OR" CAPABILITY AND RECEIVER WITH ADJUSTABLE NOISE IMMUNITY



Frequency to 0.5 MHz
Common-Mode Voltage . . . –12 V to +10 V

† The 1N4444 diodes are required only for negative common-mode protection at the driver outputs.

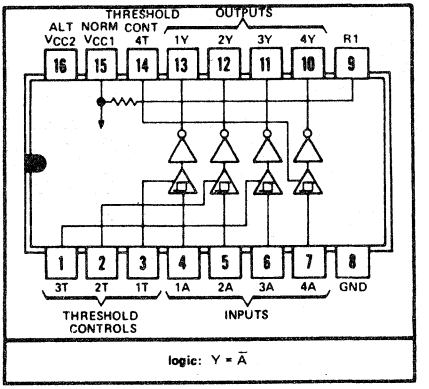
FIGURE 16–BALANCED LINE OPERATION WITH HIGH COMMON-MODE-VOLTAGE CAPABILITY

TYPE SN75154
QUADRUPLE LINE RECEIVER

BULLETIN NO. DL-S 11389, NOVEMBER 1970 – REVISED JANUARY 1977

- Satisfies Requirements of EIA Standard RS-232-C
- Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible with DTL or TTL
- Output with Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single five-volt supply; however, a built-in option allows operation from a 12-volt supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage (pin 15), V_{CC1} (see Note 1)	7 V
Alternate supply voltage (pin 16), V_{CC2}	14 V
Input voltage	±25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75154 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage (pin 15), V_{CC1}	4.5	5	5.5	V
Alternate supply voltage (pin 16), V_{CC2}	10.8	12	13.2	V
Input voltage			±15	V
Normalized fan-out from each output, N			10	
Operating free-air temperature, T_A	0		70	°C

REVISED JANUARY 1977

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage		1		3			V
V_{IL}	Low-level input voltage		1				−3	V
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.23	0.4	V
r_I	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.

‡ All typical values are at V_{CC1} = 5 V, T_A = 25°C.

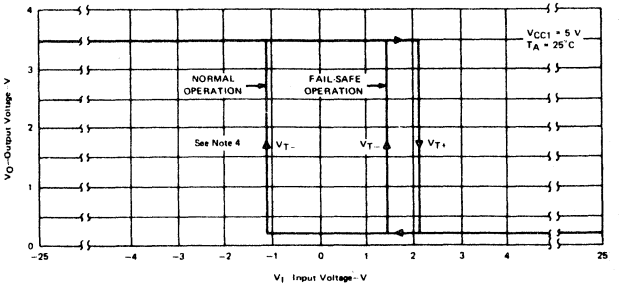
NOTE 3: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output				20		ns
t_{TLH}	Transition time, low-to-high-level output				9		ns
t_{THL}	Transition time, high-to-low-level output				6		ns

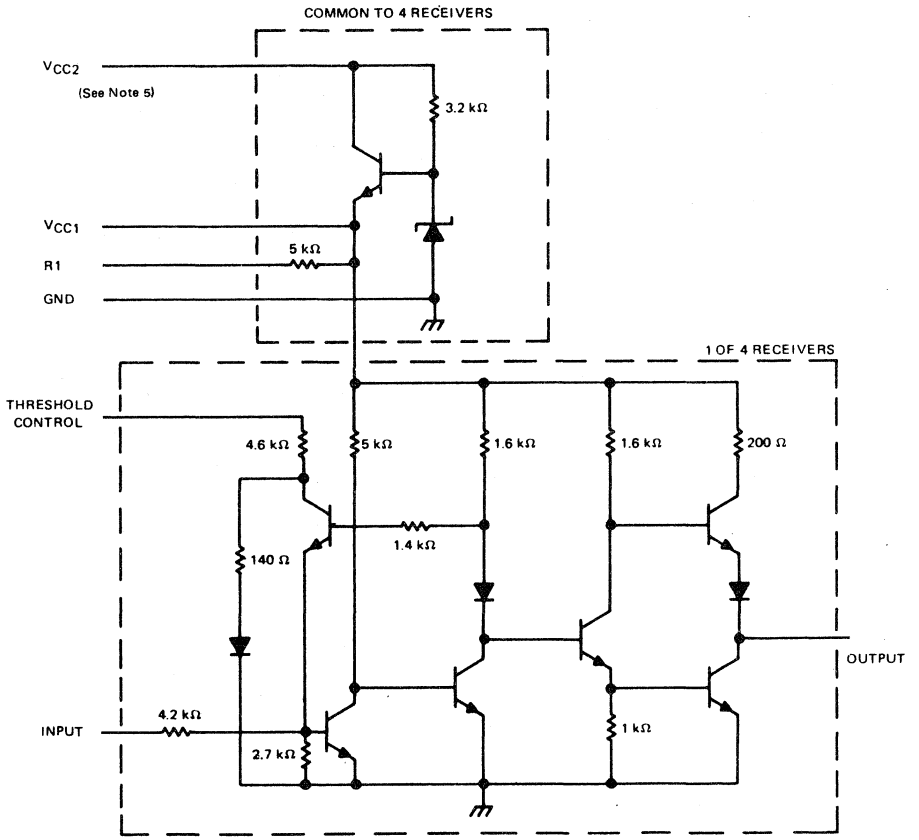
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 4: For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

schematic



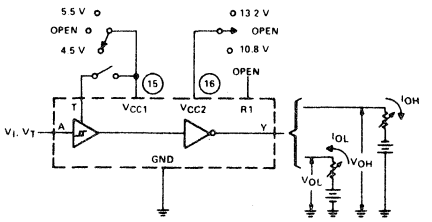
Component values shown are nominal

⏚ . . . Substrate

NOTE 5: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

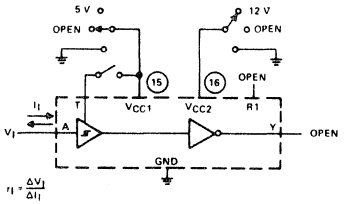


NOTES. A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

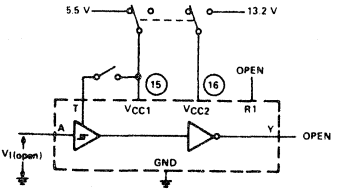
FIGURE 1 – V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

FIGURE 2–r_I



TEST TABLE

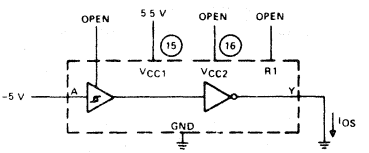
T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3–$V_{I(open)}$

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

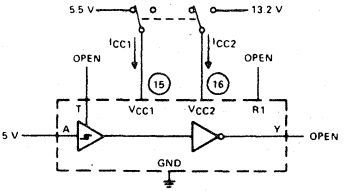
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



Each output is tested separately.

FIGURE 4–I_{OS}

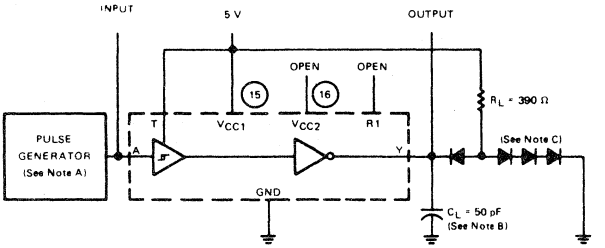


All four line receivers are tested simultaneously.

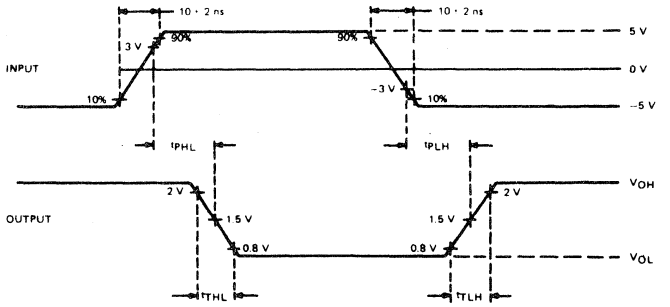
FIGURE 5–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle < 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

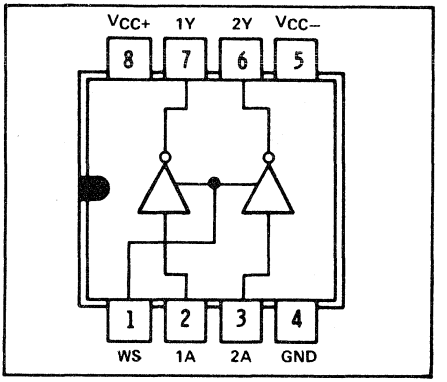
FIGURE 6–SWITCHING TIMES

TYPE SN75156
DUAL LINE DRIVER

OCTOBER 1980

- Meets EIA Standards RS-232C and RS-423A
- Wide Supply Voltage Range . . . ±7.5 V To ±15 V
- Low Supply Current . . . 4.5 mA Max per Channel
- Wave Shaping with External Resistor
- Inputs Compatible with TTL and CMOS
- Outputs at High Impedance when Power Is Off
- Positive- and Negative-Current Limiting
- Designed for Interchangeability with uA9636A
- Quad Version is SN75186

JG OR P PACKAGE
(TOP VIEW)



5

description

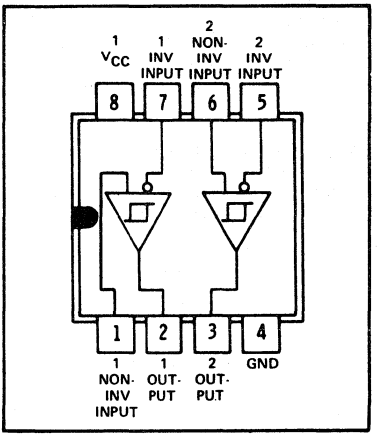
The SN75156 is a single-ended line driver designed to meet the requirements of EIA Standards RS-232C and RS-423A, CCITT Recommendations V.10, V.28, and X.26, and Federal Standard FIPS 1030. This device maintains regulated high and low output levels of 5.5 volts and –5.5 volts, respectively, over a wide range of power supply voltages. The output transition time for both drivers can be adjusted from 1 microsecond to 100 microseconds by means of an external resistor at the wave shaping (WS) pin. A high output impedance is maintained without the use of an external blocking diode.

TYPE SN75157
DUAL DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12783, SEPTEMBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package
- Similar to uA9637AC But With Standard V_{CC} and Ground Pin Position

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

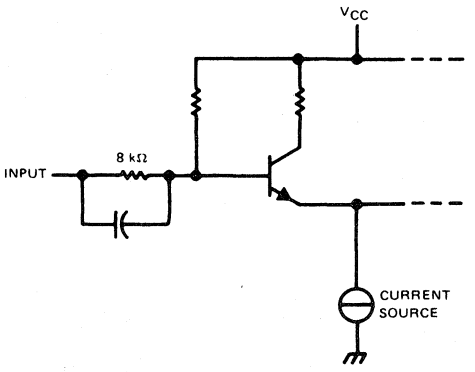
description

The SN75157 is a dual differential line receiver designed to meet EIA standards RS-422A and RS-423A. It utilizes Schottky† circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

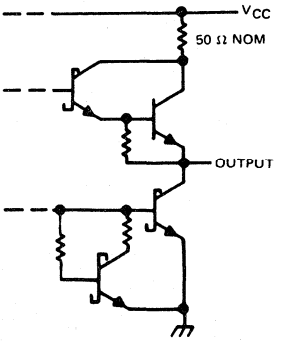
The SN75157 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mA
P package . . . . . 1000 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to the network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW. In the JG package, SN75157 chips are glass-mounted.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})	See Note 5		−0.2		0.2	V
				−0.4		0.4	
$V_{T+} - V_{T-}$	Hysteresis				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 6	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit input current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

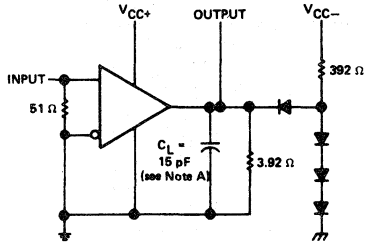
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

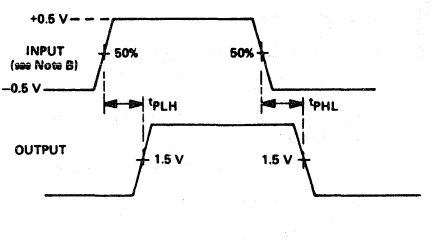
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f = 5$ ns, PRR 5 MHz, duty cycle = 10%.

FIGURE 1–TRANSITION TIMES

TYPICAL CHARACTERISTICS

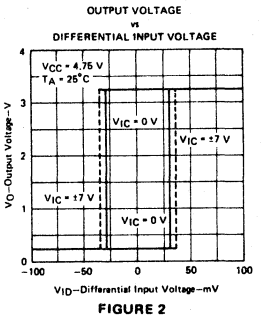


FIGURE 2

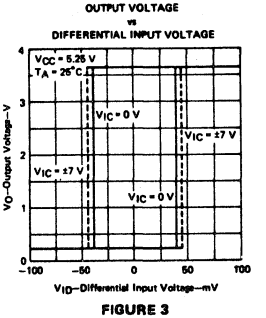


FIGURE 3

TYPICAL APPLICATION DATA

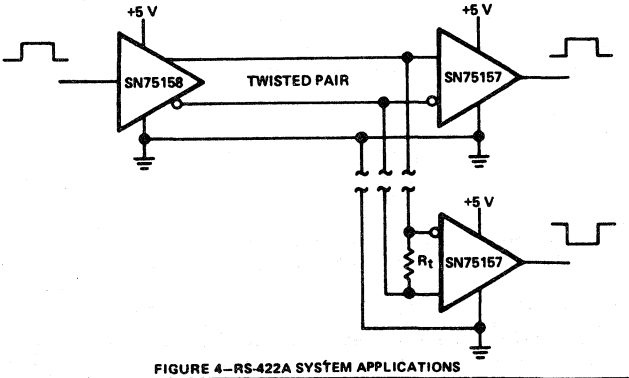


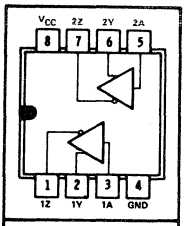
FIGURE 4–RS-422A SYSTEM APPLICATIONS

TYPES SN55158, SN75158
DUAL DIFFERENTIAL LINE DRIVERS

BULLETIN NO. DL-S 12497, JANUARY 1977

- Meets EIA Standard RS-422
- Single 5-V Supply
- Balanced-Line Operation
- TTL-, DTL-Compatible
- High Output Impedance in Power-Off Condition
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Input Clamp Diodes

SN55158 . . . JG DUAL-IN-LINE PACKAGE
SN75158 . . . JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



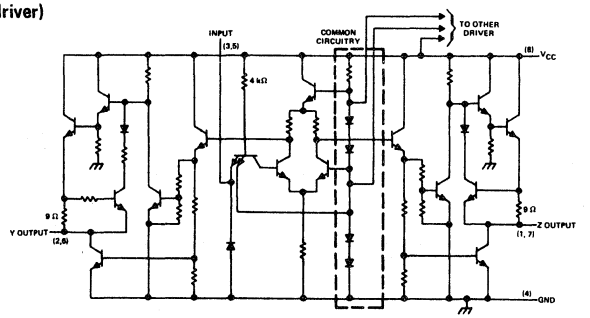
Y = A
Z = $\overline{A}$

5

description

The SN55158 and SN75158 are dual complementary-output line drivers designed to satisfy the requirements set by the EIA RS-422 standard interface specifications. The inputs are standard TTL. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

schematic (each driver)



Components within the dashed box are common to both drivers. Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55158	−55°C to 125°C
SN75158	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values except, differential output voltage V_{OD}, are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN55158 chips are alloy-mounted; SN75158 chips are glass-mounted.

recommended operating conditions

	SN55158			SN75158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55158			SN75158			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA	2	3.0		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA		0.2	0.4		0.2	0.4	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.5	$2V_{OD2}$		3.5	$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	3.0		2	3.0		V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage §	V_{CC} = MIN			±0.02	±0.4		±0.02	±0.4	V
V_{OC}	Common-mode output voltage ¶	V_{CC} = MAX			1.9	3		1.8	3	V
		V_{CC} = MIN			1.4	3		1.5	3	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage §	V_{CC} = MIN or MAX			±0.01	±0.4		±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100		0.1	100	μA
			V_O = −0.25 V		−0.1	−100		−0.1	−100	
			V_O = −0.25 V to 6 V			±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{OS}	Short-circuit output current #	V_{CC} = MAX		−40	−90	−150	−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load,	Inputs grounded, T_A = 25°C		37	50		37	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55158			SN75158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20		10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15		9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20		4	20	ns
	Overshoot factor	See Figure 2, Termination C			10			10	%

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PARAMETER MEASUREMENT INFORMATION

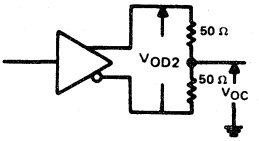
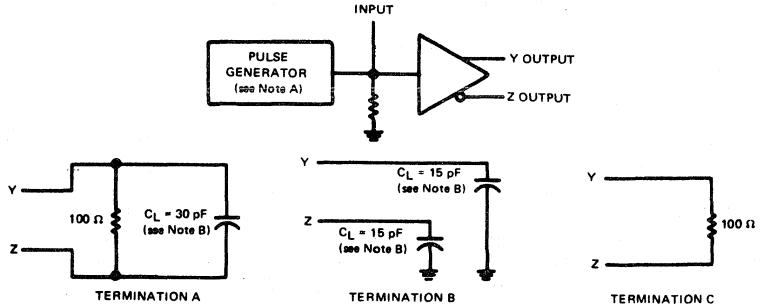


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 25 ns, PRR = 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

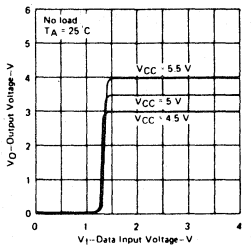


FIGURE 3

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

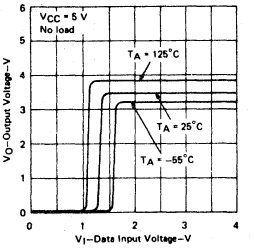


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

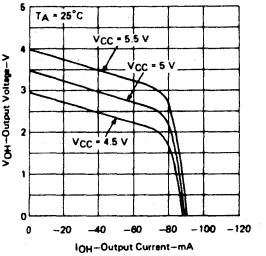


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

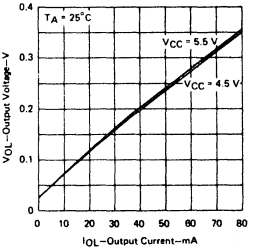


FIGURE 6

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

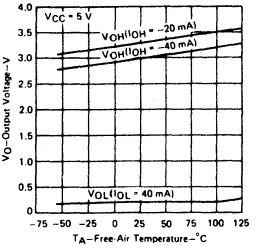


FIGURE 7

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

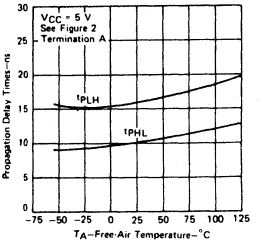


FIGURE 8

SUPPLY CURRENT (BOTH DRIVERS) vs SUPPLY VOLTAGE

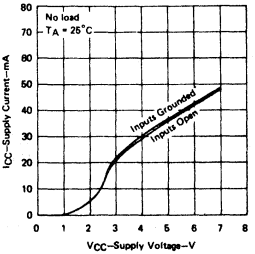


FIGURE 9

SUPPLY CURRENT (BOTH DRIVERS) vs FREE-AIR TEMPERATURE

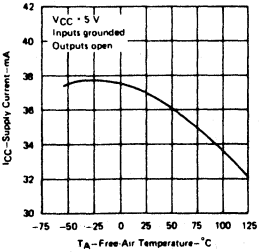


FIGURE 10

SUPPLY CURRENT (BOTH DRIVERS) vs FREQUENCY

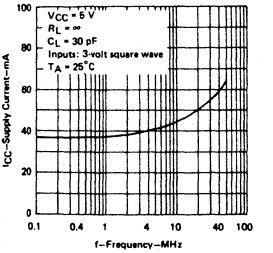


FIGURE 11

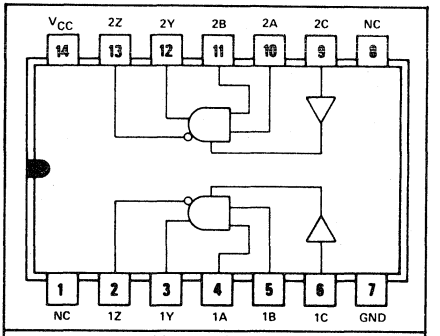
† Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPE SN75159
DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12501, JANUARY 1977

- Meets EIA Standard RS-422
- Single 5-V Supply
- Balanced Line Operation
- TTL and DTL Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

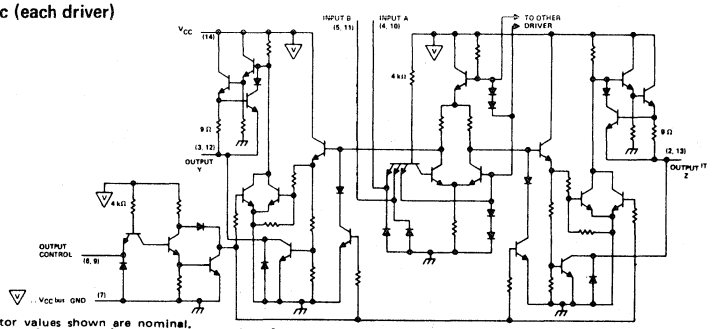


NC—No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75159 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = MAX,	I_O = −40 mA			−1.1	−1.5	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0			3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω,	See Figure 1	2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage §	V_{CC} = MIN				±0.02	±0.4	V
V_{OC}	Common-mode output voltage ¶	V_{CC} = MAX				1.8	3	V
		V_{CC} = MIN				1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage §	V_{CC} = MIN or MAX				±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current #	V_{CC} = MAX			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, T_A = 25°C	Inputs grounded,	No load,		47	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

PARAMETER MEASUREMENT INFORMATION

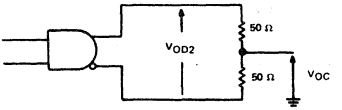
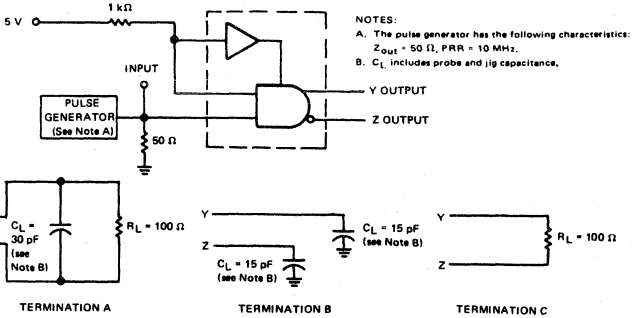
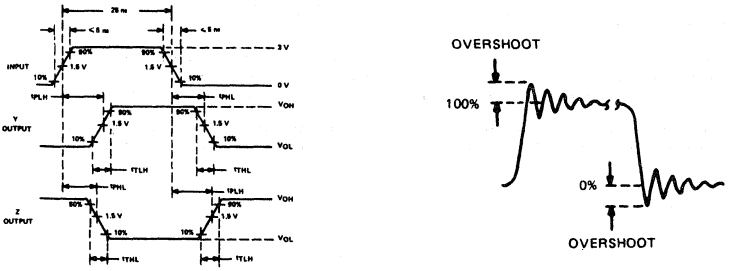


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



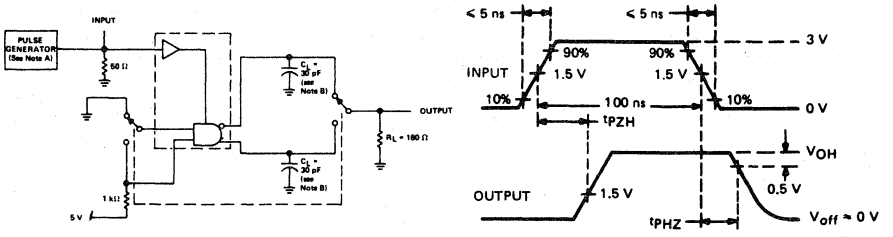
TEST CIRCUITS



VOLTAGE WAVEFORMS

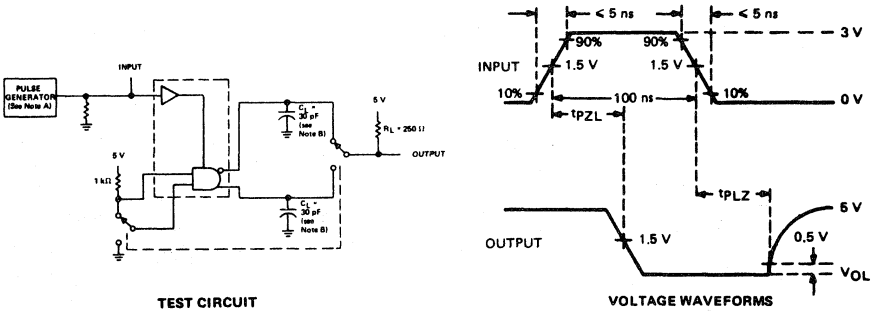
FIGURE 2–t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3—t_{PZH} AND t_{PHZ}



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4—t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

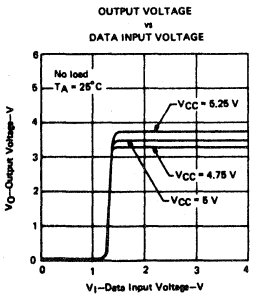


FIGURE 5

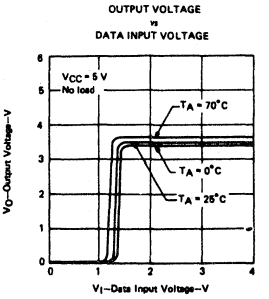


FIGURE 6

TYPICAL CHARACTERISTICS

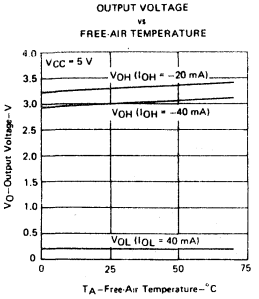


FIGURE 7

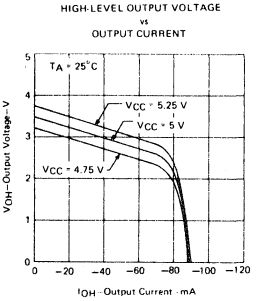


FIGURE 8

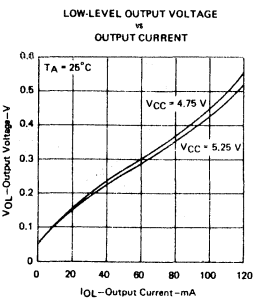


FIGURE 9

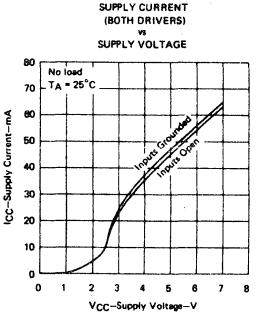


FIGURE 10

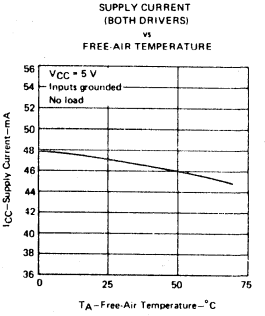


FIGURE 11

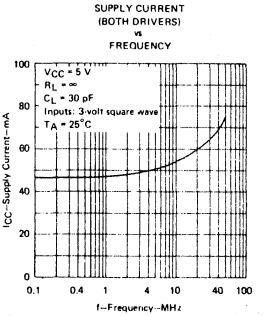


FIGURE 12

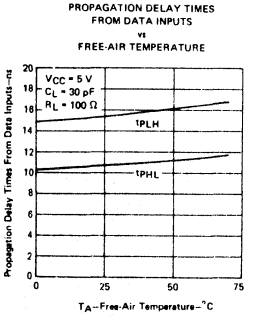


FIGURE 13

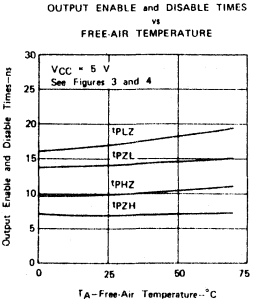


FIGURE 14

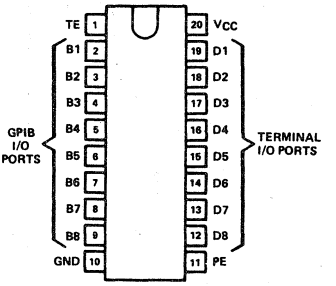
TYPE SN75160A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

BULLETIN NO. DL-S 12786, OCTOBER 1980

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed, Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 66 mW Max per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0 V)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

description

The SN75160A 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the open-collector or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of open-collector outputs when Pull-up Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active-turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high-impedance to the bus when V_{CC} = 0 volts. When combined with the SN75161A or SN75162A management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

FUNCTION TABLES

DRIVERS

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z*
X	L	X	Z*

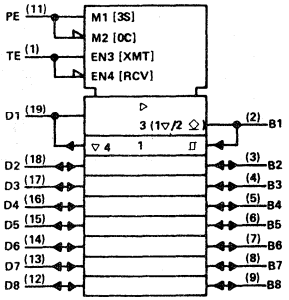
RECEIVERS

INPUTS			OUTPUTS
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

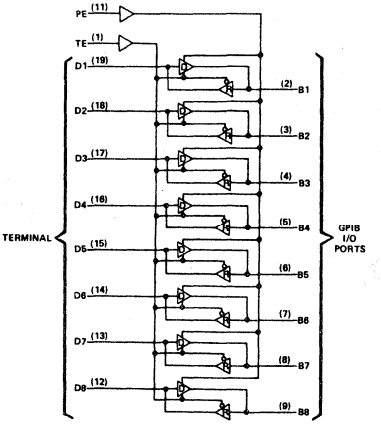
*This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol‡



‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

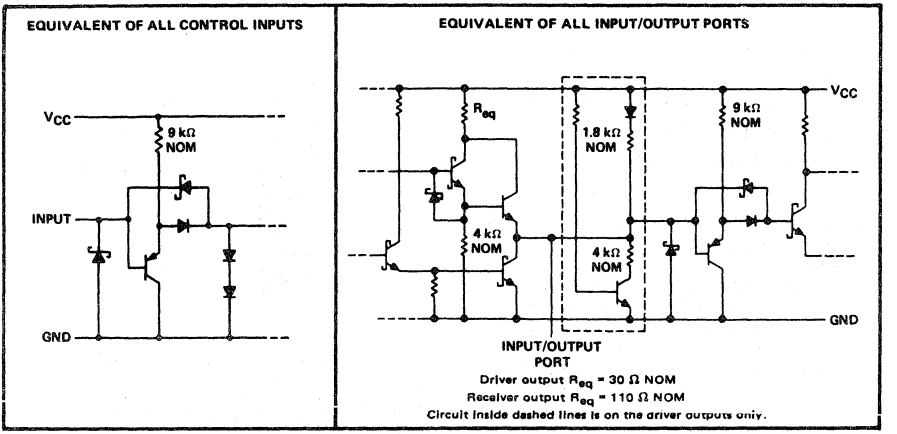
functional block diagram (positive logic)



TEXAS INSTRUMENTS
INCORPORATED

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1375 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75160A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.4	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		60	80	mA
				Drivers low and enabled		75	100	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

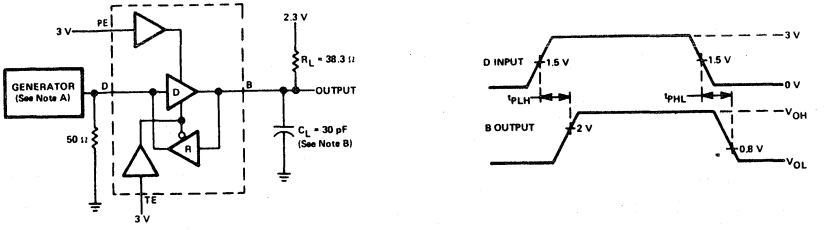
†All typical values are at V_{CC} = 5, T_A = 25°C.

‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 8.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

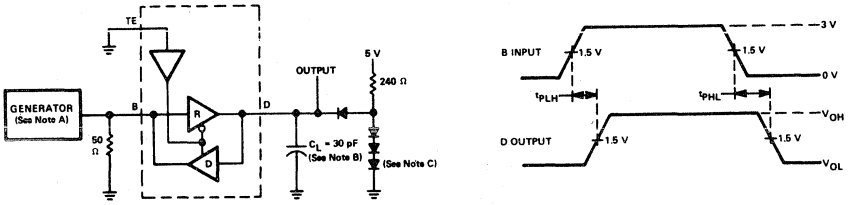
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V, See Figure 2		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE	Bus	R_L = 480 Ω to 0 V, See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V, See Figure 3		22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	R_L = 3 kΩ to 0 V, See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V, See Figure 4		23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Bus	R_L = 480 Ω to 0 V, See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

PARAMETER MEASUREMENT INFORMATION



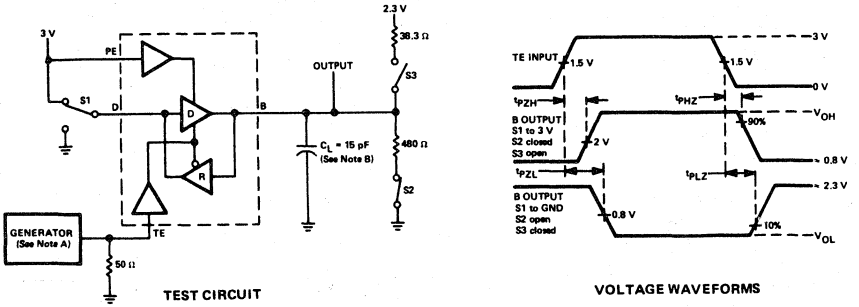
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1–TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2–BUS-TO-TERMINAL PROPAGATION DELAY TIMES

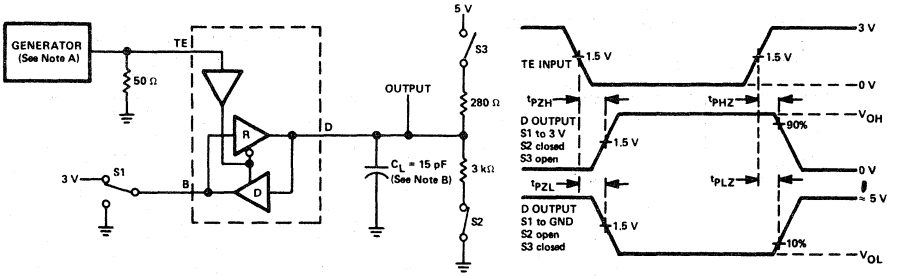


TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–TE-TO-BUS ENABLE AND DISABLE TIMES

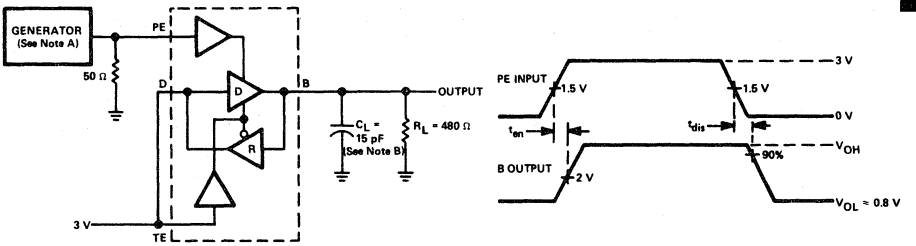
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4—TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5—PE-TO-BUS PULL-UP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

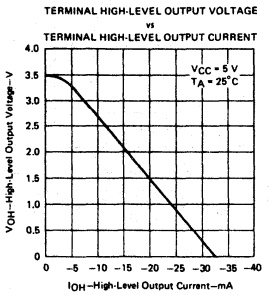


FIGURE 6

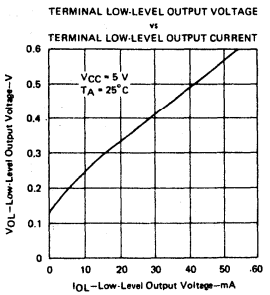


FIGURE 7

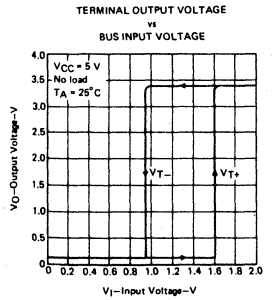


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

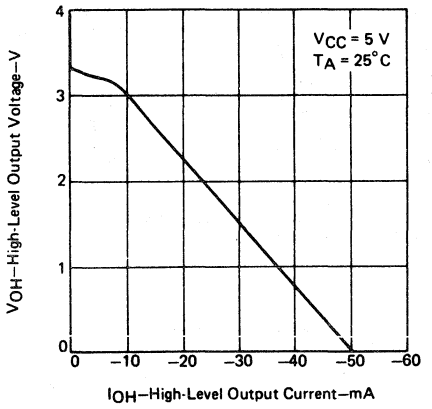


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

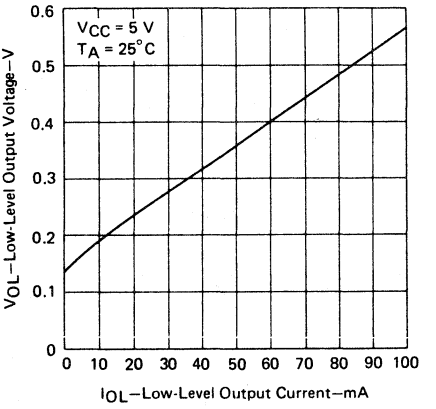


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

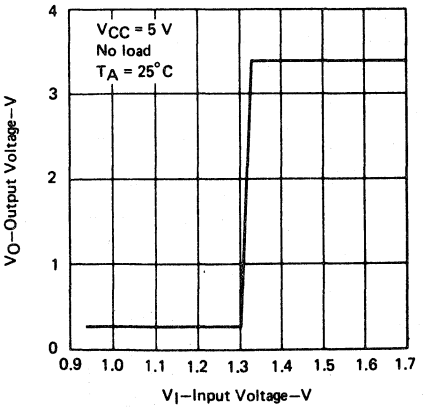


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

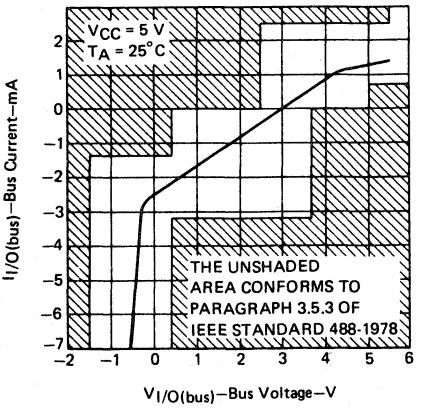


FIGURE 12

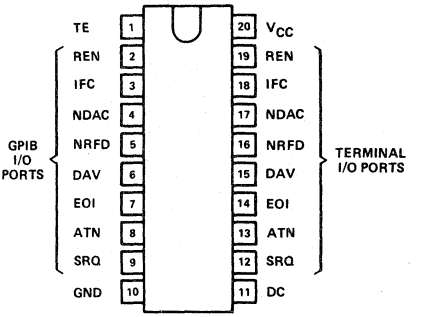
TYPES SN75161A, SN75162A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

BULLETIN NO. DL-S 12787, OCTOBER 1980

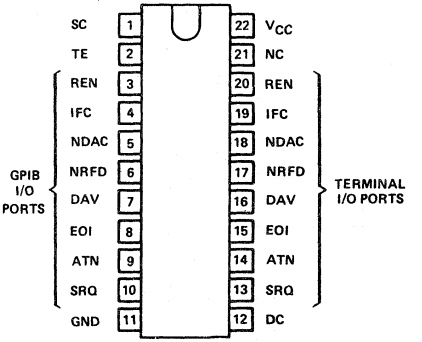
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- SN75161A Designed for Single Controller
- SN75162A Designed for Multi-Controllers
- High-Speed, Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 65 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus when Device is Powered Down (V_{CC} = 0 V)

SN75161A . . . J or N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75162A . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC = No internal connection

description

The SN75161A and SN75162A eight-channel general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160A octal bus transceiver, the SN75161A or SN75162A provides the complete 16-wire interface for the IEEE 488 bus.

The SN75161A and SN75162A each features eight driver-receiver pairs connected in a front-to-back configureation to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162A) enable signals. The SC input on the SN75162A allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high-impedance to the bus when V_{CC} = 0 volts. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high-input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high-impedance to the terminal when disabled.

The SN75161A is manufactured in a 20-pin dual-in-line package. The SN75162A is manufactured in a 22-pin 400-mil (10,2-mm) dual-in-line package. The SN75161A and SN75162A are characterized for operation from 0°C to 70°C.

TABLE OF ABBREVIATIONS

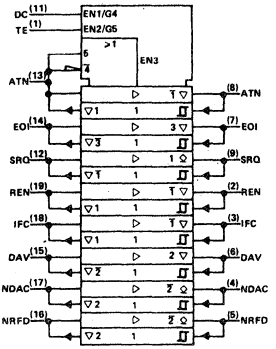
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162 only)	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Edentify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

TEXAS INSTRUMENTS
INCORPORATED

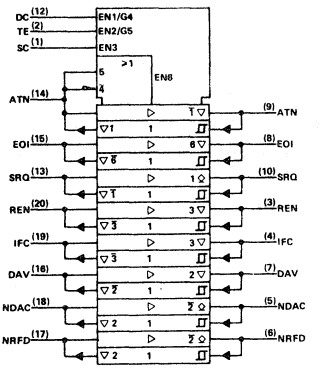
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbols†

SN75161A



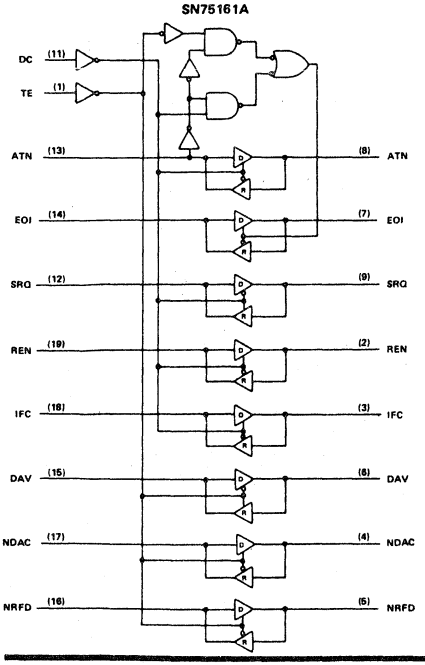
SN75162A



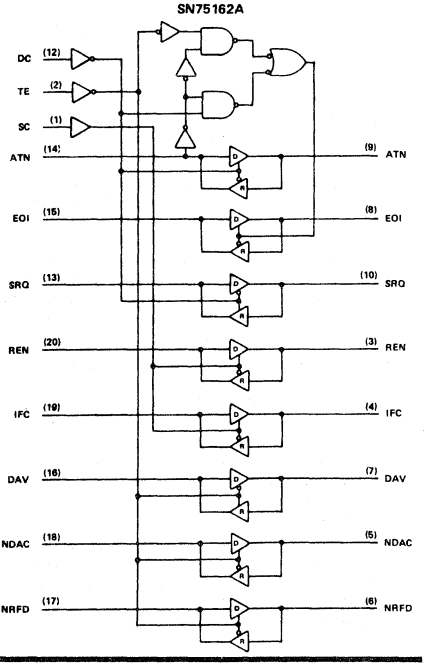
▽ designates 3-state output, ◇ designates open-collector outputs.
†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagrams (positive logic)

SN75161A



SN75162A



SN75161A

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162A

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

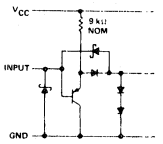
H = high level, L = Low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

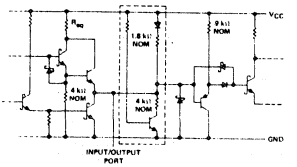
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

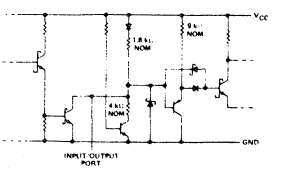


TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J Package . . . . . 1375 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75161A and SN75162A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

5

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis	Bus			0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 µA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	µA
$V_{(I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	µA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load, TE, DC, and SC low				100	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

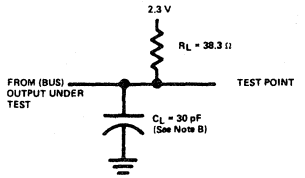
†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

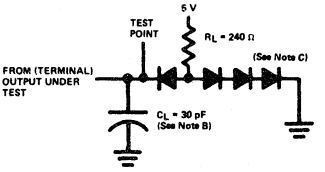
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V, See Figure 2		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	R_L = 480 Ω to 0 V, See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V, See Figure 3			60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	R_L = 3 kΩ to 0 V, See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V, See Figure 4			45	
t_{PLZ}	Output disable time from low level						55	

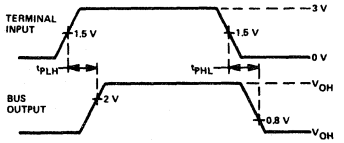
5

PARAMETER MEASUREMENT INFORMATION



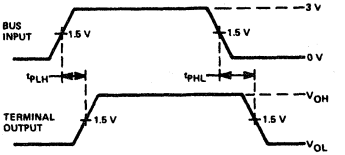
LOAD CIRCUIT





VOLTAGE WAVEFORMS

FIGURE 1 – TERMINAL-TO-BUS PROPAGATION DELAY TIMES

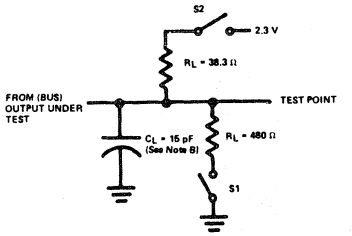


VOLTAGE WAVEFORMS

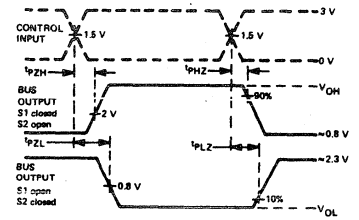
FIGURE 2 – BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

PARAMETER MEASUREMENT INFORMATION

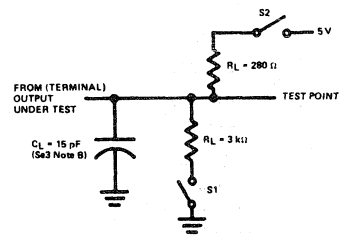


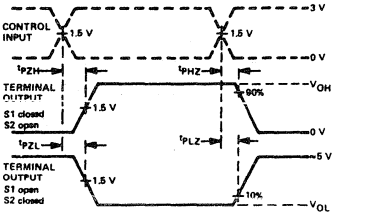
LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3 – BUS ENABLE AND DISABLE TIMES





VOLTAGE WAVEFORMS

FIGURE 4 – TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

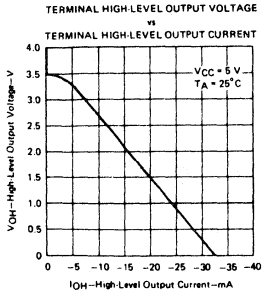


FIGURE 1

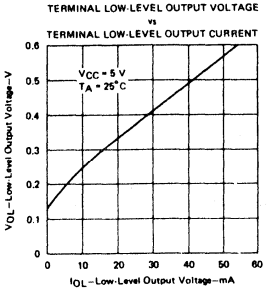


FIGURE 2

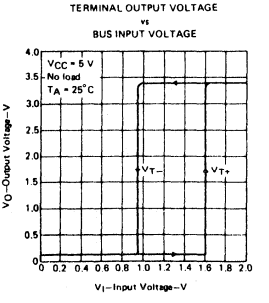


FIGURE 3

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

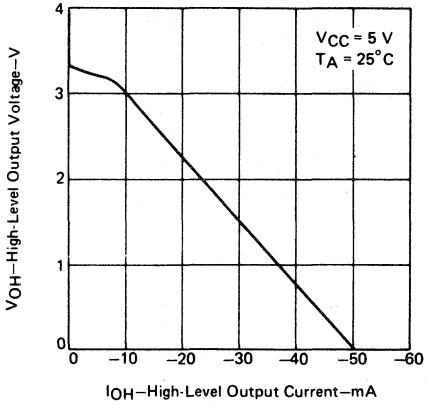


FIGURE 4

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

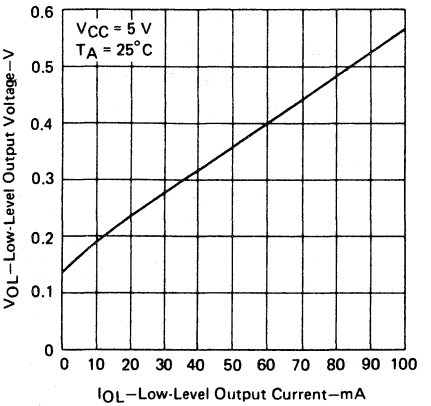


FIGURE 5

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

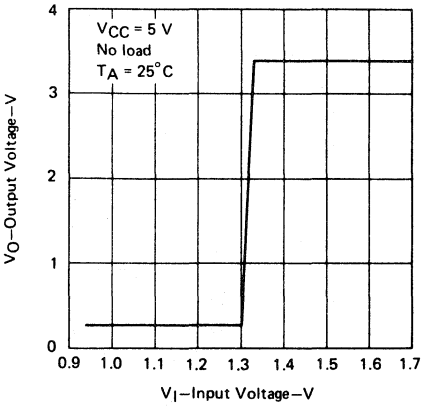


FIGURE 6

BUS CURRENT
vs
BUS VOLTAGE

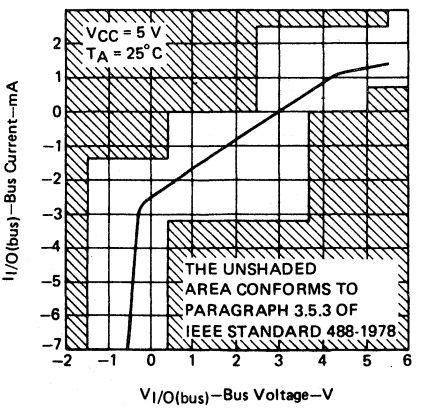


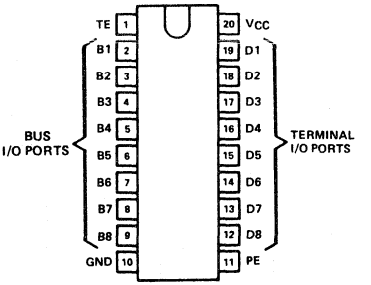
FIGURE 7

TYPE SN75163A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

BULLETIN NO. DL-S 12778, OCTOBER 1980

- 8-Channel Bidirectional Transceivers
- High-Speed Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 60 mW Max per Channel
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0 V)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75163A octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or three-state modes. If Talk Enable is high, these outputs have the characteristics of open-collector outputs when Pull-up Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 millivolts of guaranteed hysteresis for increased noise immunity.

The SN75163 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

DRIVERS

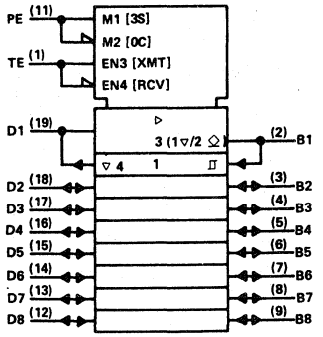
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

RECEIVERS

INPUTS			OUTPUTS
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

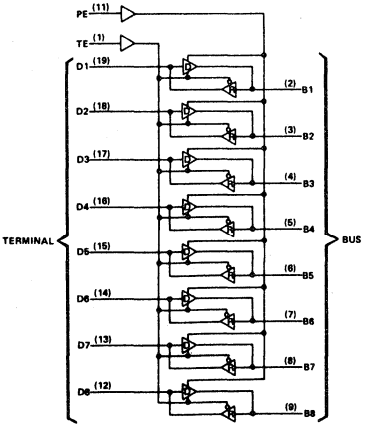
H = high level, L = low level, X = irrelevant, Z = High-impedance state.

logic symbol‡

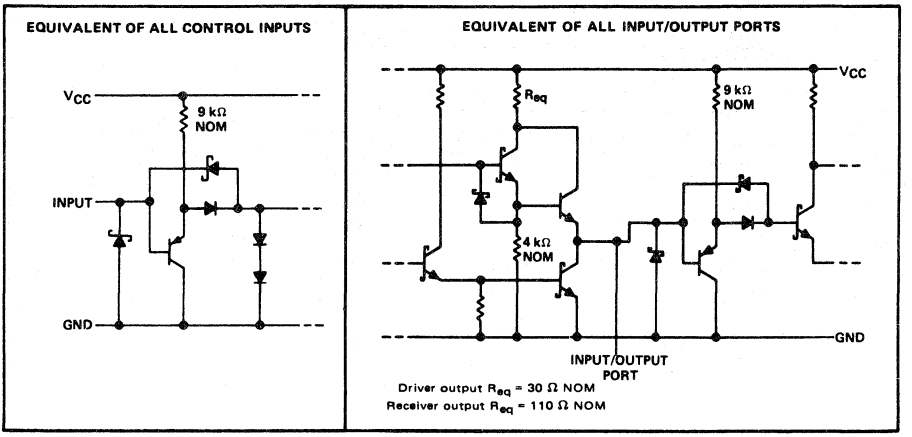


‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75163A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−10	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled			70	mA
				Drivers low and enabled			90	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5, T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE	Bus	R_L = 480 Ω to 0 V		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V		22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	R_L = 3 kΩ to 0 V		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V		23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Terminal	R_L = 480 Ω to 0 V		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

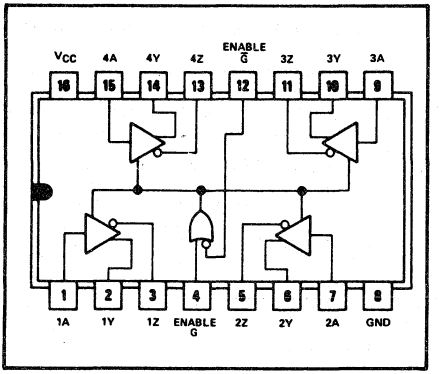
For test circuits and voltage waveforms, see SN75160A, pages 5-174 and 5-175.

TYPE SN75172
QUADRUPLE DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12769, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range . . . −7 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Functionally Interchangeable With AM26LS31

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



5

description

The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standard RS-422A and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

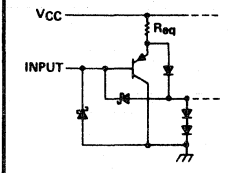
H = high level
L = low level
X = irrelevant
Z = high impedance (off)

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission-bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

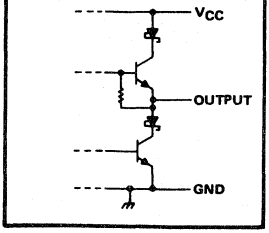
The SN75172 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75172 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode output voltage, V_{OC}	−7†		12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet with common-mode output voltage only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless other noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 60 Ω,	See Figure 1	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 60 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 2		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 3		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		18	30	ns

PARAMETER MEASUREMENT INFORMATION

5

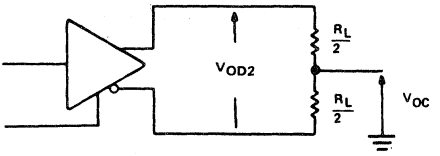
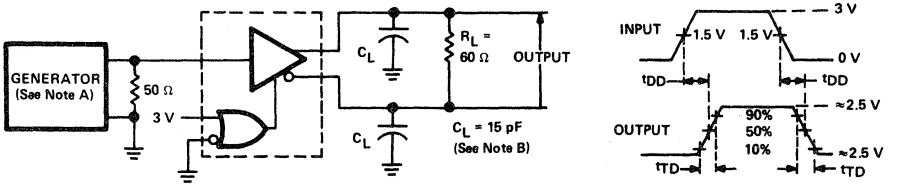


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

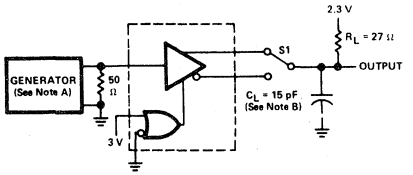


TEST CIRCUIT VOLTAGE WAVEFORMS

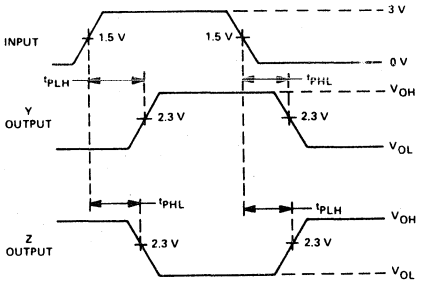
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 2–DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

PARAMETER MEASUREMENT INFORMATION

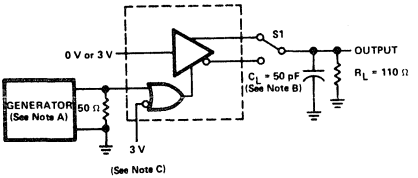


TEST CIRCUIT

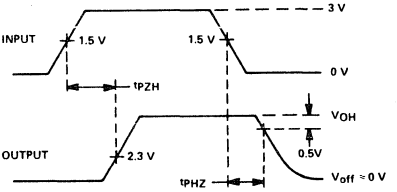


VOLTAGE WAVEFORMS

FIGURE 3–PROPAGATION DELAY TIMES

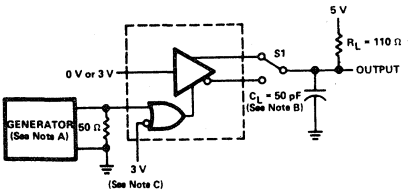


TEST CIRCUIT

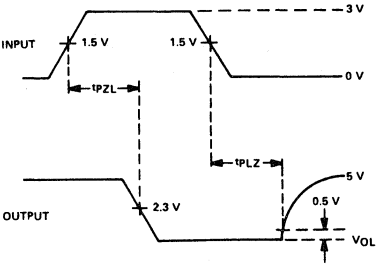


VOLTAGE WAVEFORMS

FIGURE 4–t_{PZH} AND t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5–t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} = 50 Ω.

B. C_L include probe and jig capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

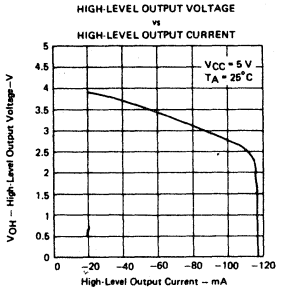


FIGURE 6

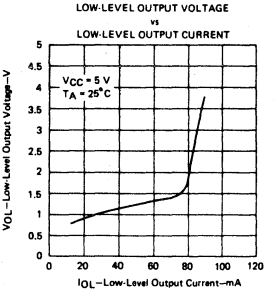


FIGURE 7

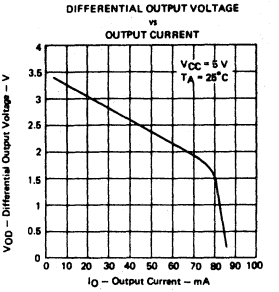


FIGURE 8

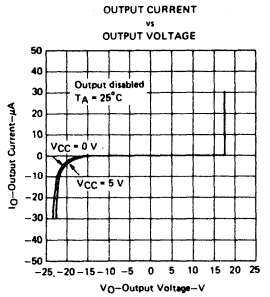


FIGURE 9

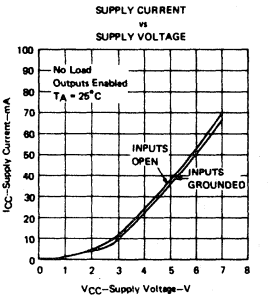


FIGURE 10

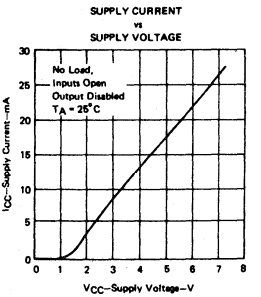


FIGURE 11

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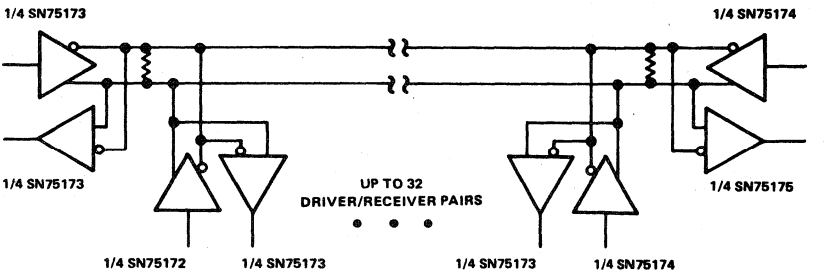
TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

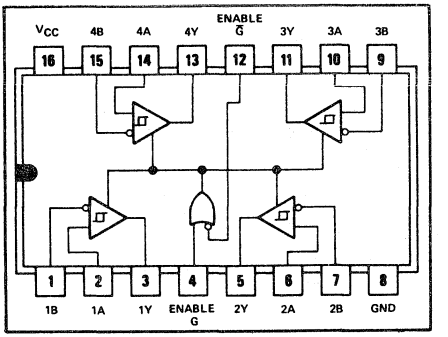
FIGURE 12

TYPE SN75173
QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12770, OCTOBER 1980

- Meets EIA Standards RS-422A and RS-423A
- **Meets CCITT Recommendations V.10, V.11 X.26, and X.27**
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range . . . −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- High Input Impedance . . . 12 kΩ Min
- **Operates from Single 5-Volt Supply**
- **Low Power Requirements**
- Plug-In Replacement for AM26LS32

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
−0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

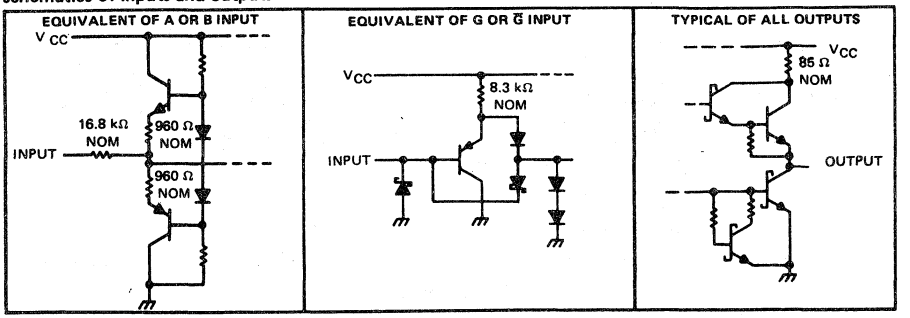
H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

description

The SN75173 is a monolithic quadruple differential line receiver with three state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features an active-high enable and an active-low enable common to all four receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN75173 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75173 chips are glass-mounted.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

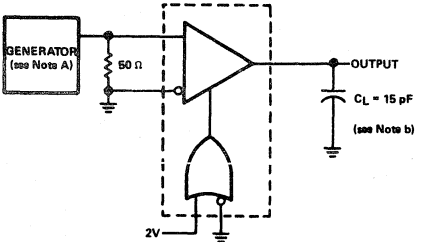
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA Standard RS-422A and RS-423A for exact conditions.

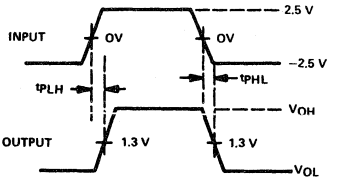
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,	C_L = 15 pF,		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

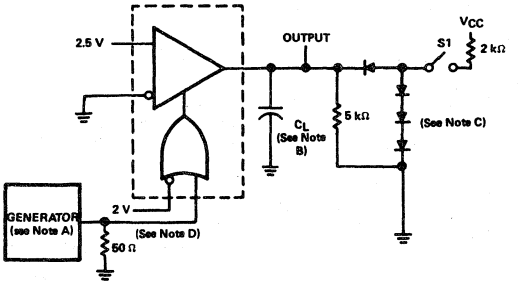


TEST CIRCUIT

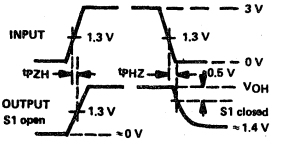


VOLTAGE WAVEFORMS

FIGURE 1 – t_{PLH}, t_{PHL}



TEST CIRCUIT

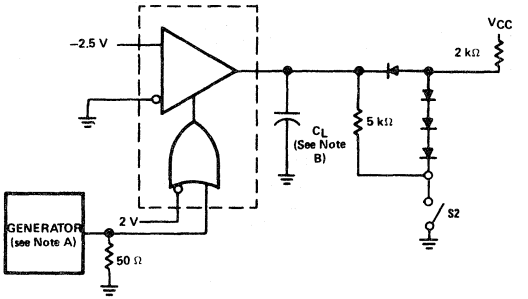


VOLTAGE WAVEFORMS

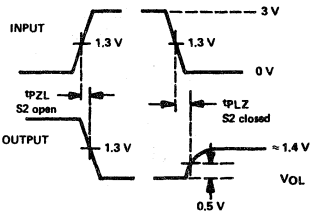
FIGURE 2 – t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are in 916 or equivalent.
D. To test the active low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle, = 50%, t_r = t_f = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are in 916 or equivalent.
D. To test the active low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

FIGURE 3 – t_{PZL}, t_{PLZ}

TYPICAL CHARACTERISTICS

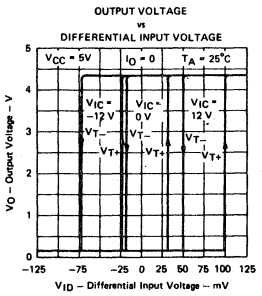


FIGURE 4

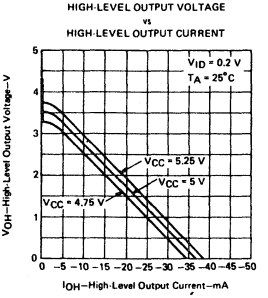


FIGURE 5

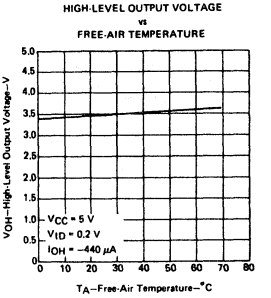


FIGURE 6

TYPICAL CHARACTERISTICS

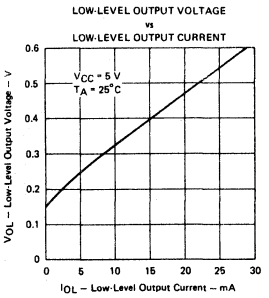


FIGURE 7

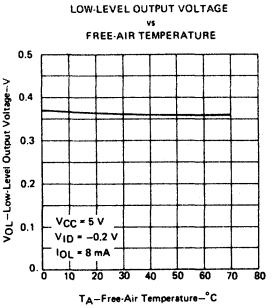


FIGURE 8

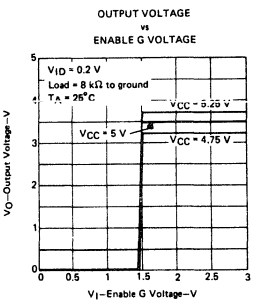


FIGURE 9

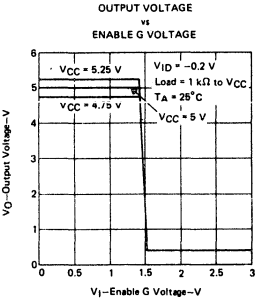
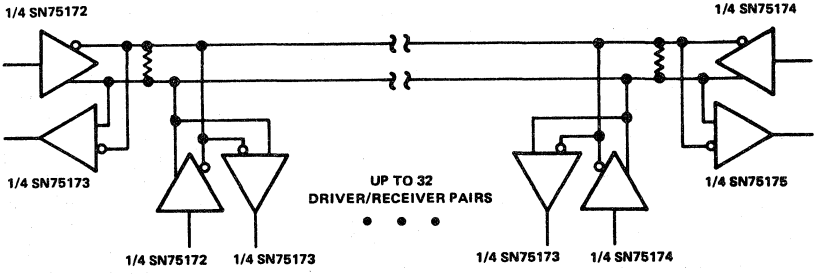


FIGURE 10

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

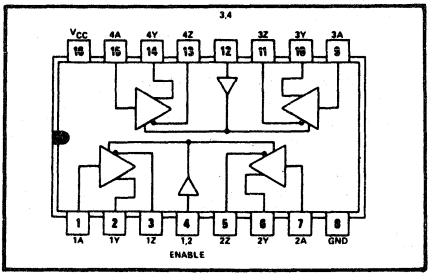
FIGURE 11

TYPE SN75174
QUADRUPLE DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12771, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range ... −7 V to 12 V
- Active-High Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Functionally Interchangeable with MC3487

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, L = TTL low level, X = irrelevant, Z = high impedance (off)

description

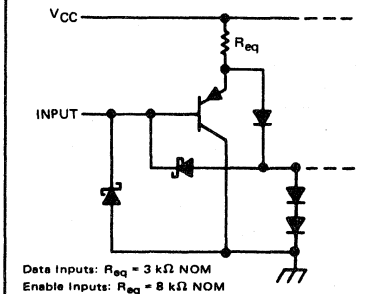
The SN75174 is a monolithic guadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standard RS-422A and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

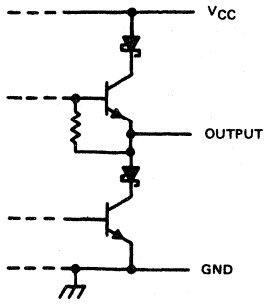
The SN75174 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75174 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode output voltage, V_{OC}	−7†		12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet with common-mode output voltage only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless other noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 33 mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 60 Ω,	See Figure 1	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 60 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 2		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 3		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		18	30	ns

PARAMETER MEASUREMENT INFORMATION

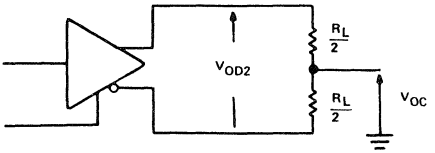
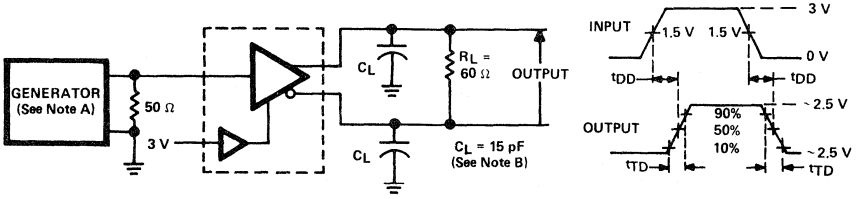


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

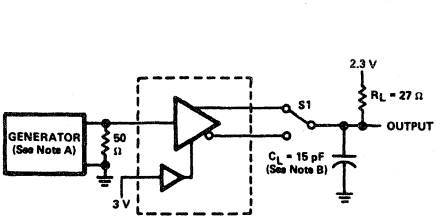


TEST CIRCUIT VOLTAGE WAVEFORMS

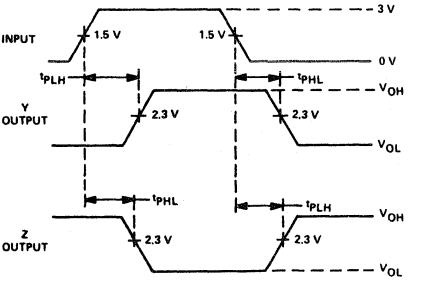
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are IN916 or IN3064.

FIGURE 2–DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

PARAMETER MEASUREMENT INFORMATION

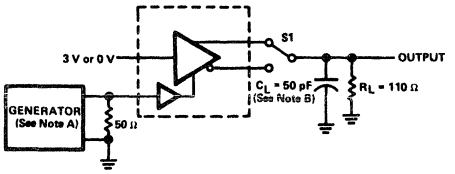


TEST CIRCUIT

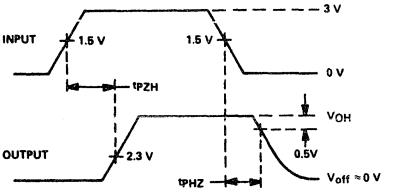


VOLTAGE WAVEFORMS

FIGURE 3–PROPAGATION DELAY TIMES

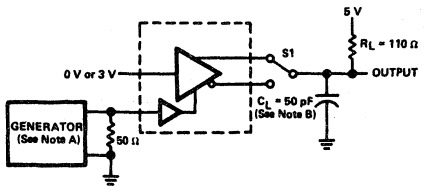


TEST CIRCUIT

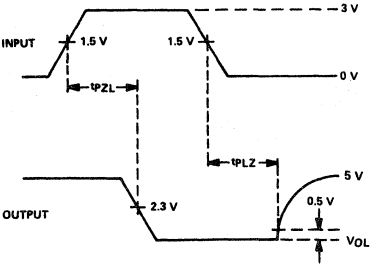


VOLTAGE WAVEFORMS

FIGURE 4–t_{PZH} AND t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5–t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_o = 50\ \Omega$.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

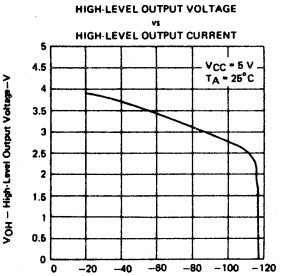


FIGURE 6

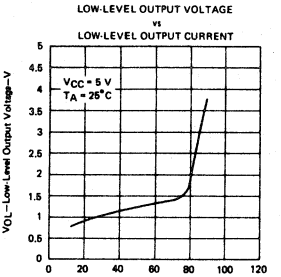


FIGURE 7

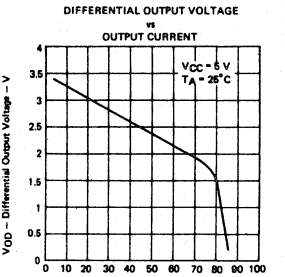


FIGURE 8

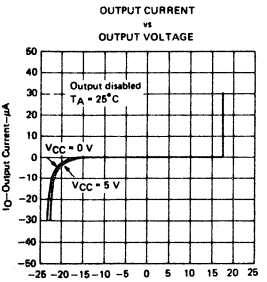


FIGURE 9

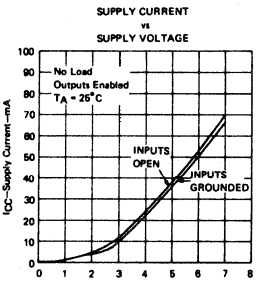


FIGURE 10

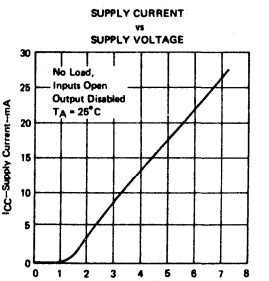
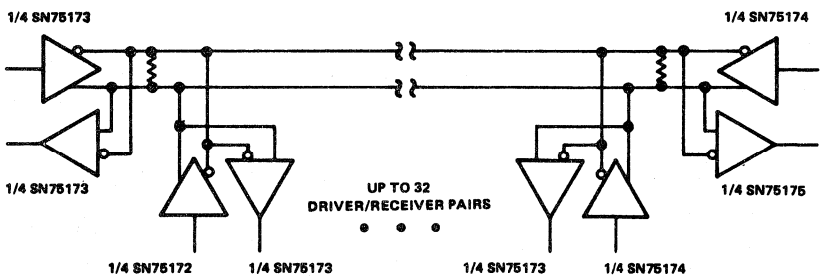


FIGURE 11

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

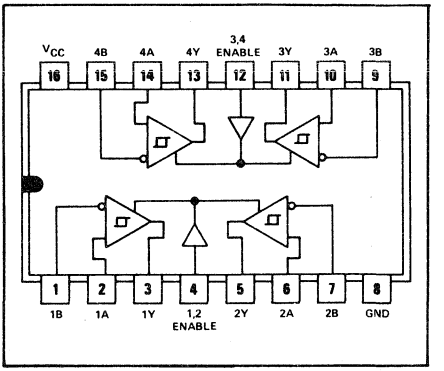
FIGURE 12

TYPE SN75175
QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12772, OCTOBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for MC3486

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

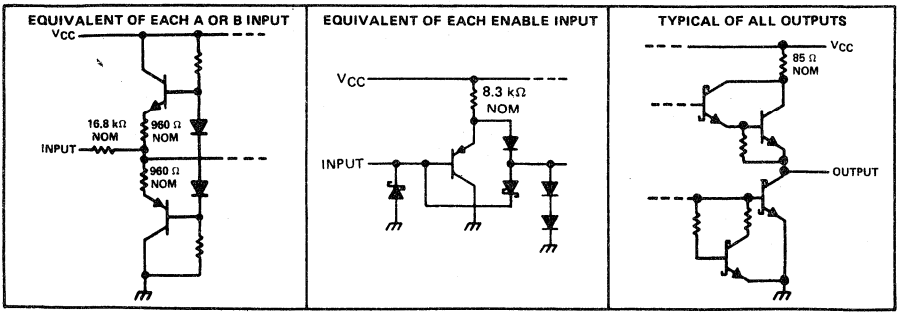
The SN75175 is a monolithic quadrupled differential line receiver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features two active-high enables, each common to two receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at a rate of 8.2 mW/°C and the N package to 736 mW at 70°C at a rate of 9.2 mW/°C. In the J package, SN75175 chips are glass-mounted.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA standards RS-422A and RS-423A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level				25	35	ns

PARAMETER MEASUREMENT INFORMATION

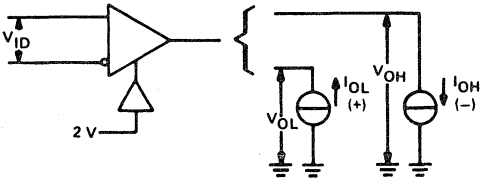


FIGURE 1–V_{OH}, V_{OL}

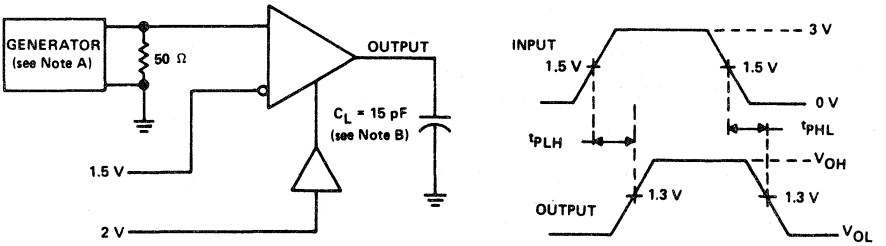
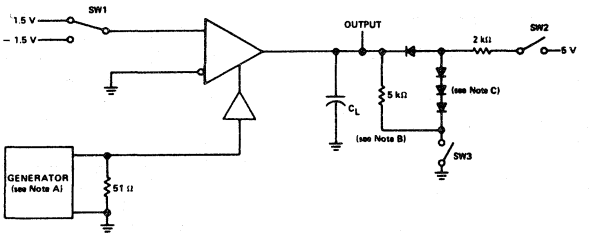


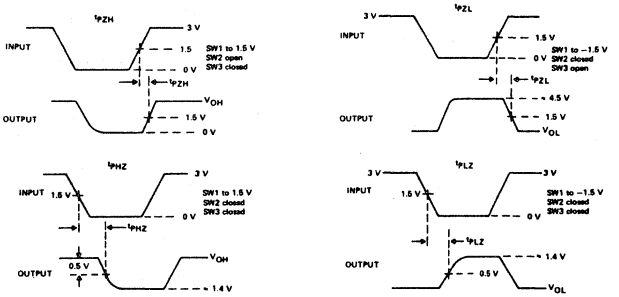
FIGURE 2–PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3–ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns, $Z_{out} = 50\ \Omega$.

B. C_L includes probe and stray capacitance

C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

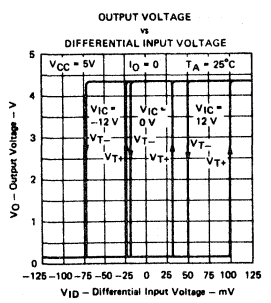


FIGURE 4

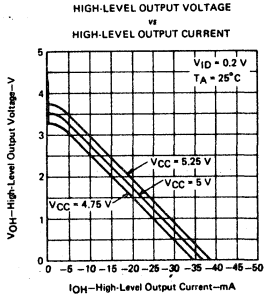


FIGURE 5

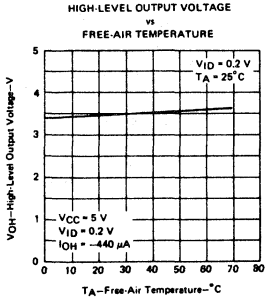


FIGURE 6

TYPICAL CHARACTERISTICS

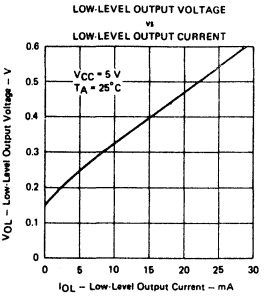


FIGURE 7

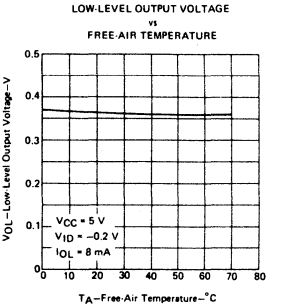


FIGURE 8

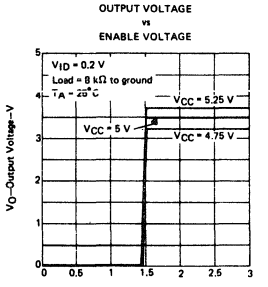


FIGURE 9

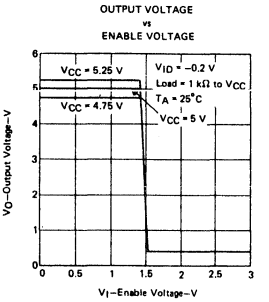


FIGURE 10

TYPICAL APPLICATION

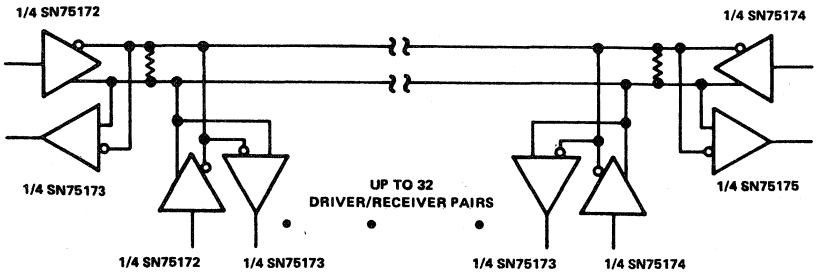


FIGURE 11

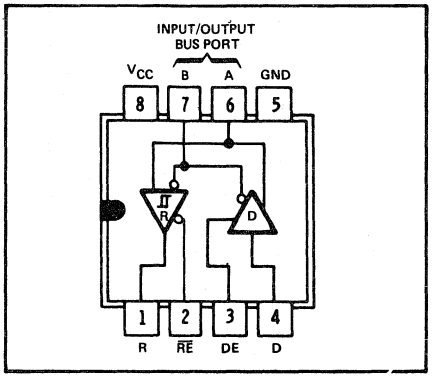
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

TYPE SN75176
DIFFERENTIAL BUS TRANSCEIVER

BULLETIN NO. DL-S 12790, OCTOBER 1980

- Bidirectional Transceiver
- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

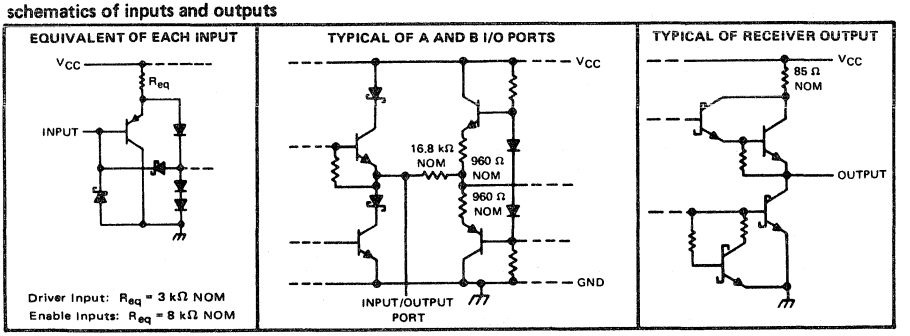
The SN75176 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A, the EIA Subcommittee TR30.1 Draft Standard PN1360, and CCITT Recommendations V.11 and X.27.

The SN75176 combines a three-state differential line driver and a differential-input line receiver both of which operate from a single 5-volt power supply. The driver and receiver have an active enable that can be externally connected to function as a direction control. The driver differential-outputs and the receiver differential-inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0 volts. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 milliamperes of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 millivolts, and a typical input hysteresis of 50 millivolts.

The SN75176 can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG Package . . . . . 825 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75176 chips are glass-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}		−7†		12	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 9	2	2.7		V
		R_L = 54 Ω,	See Figure 9	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 9			±0.2	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 11		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 12		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 13		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 14		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 13		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 14		18	30	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2¶			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 10		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 10	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,			26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 15		27	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 16		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 16		26	35	ns
t_{PLZ}	Output disable time from low level				27	35	ns

TYPICAL CHARACTERISTICS

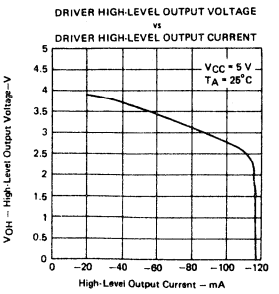


FIGURE 1

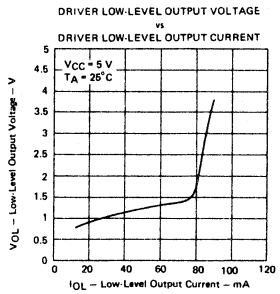


FIGURE 2

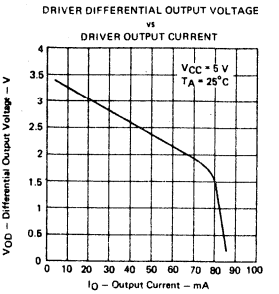


FIGURE 3

TYPICAL CHARACTERISTICS

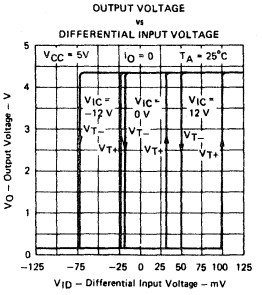


FIGURE 4

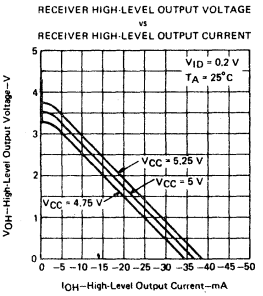


FIGURE 5

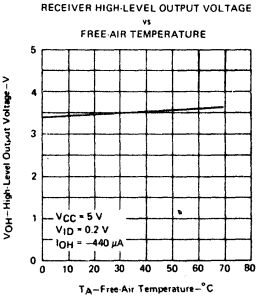


FIGURE 6

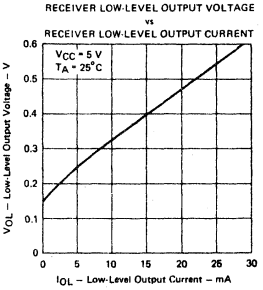


FIGURE 7

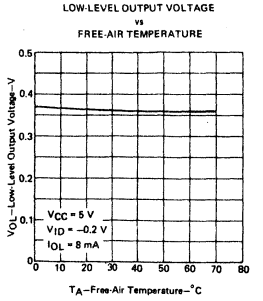


FIGURE 8

PARAMETER MEASUREMENT INFORMATION

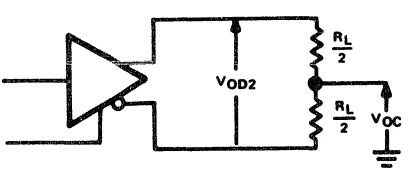


FIGURE 9–DRIVER V_{OD} AND V_{OC}

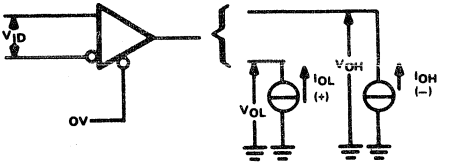
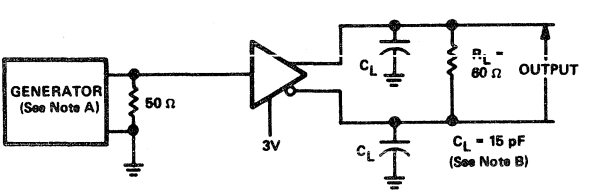
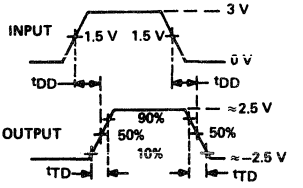


FIGURE 10–RECEIVER V_{OH} AND V_{OL}

5

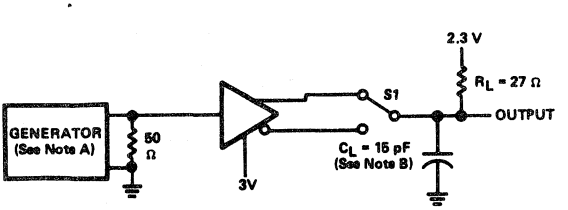


TEST CIRCUIT

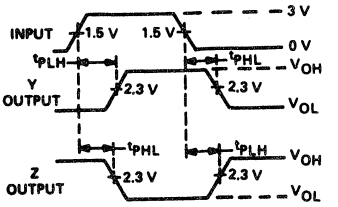


VOLTAGE WAVEFORMS

FIGURE 11–DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT

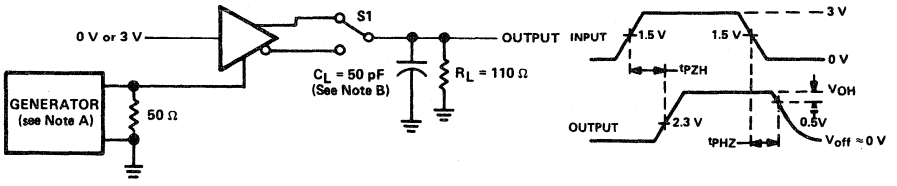


VOLTAGE WAVEFORMS

FIGURE 12–DRIVER PROPAGATION TIMES

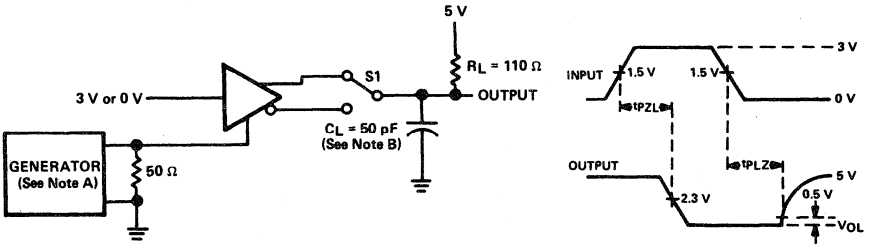
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



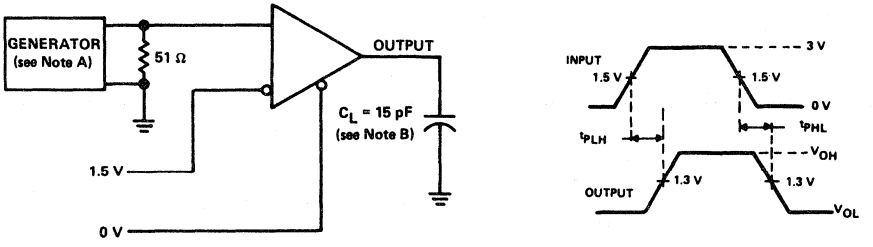
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 13–DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 14–DRIVER ENABLE AND DISABLE TIMES

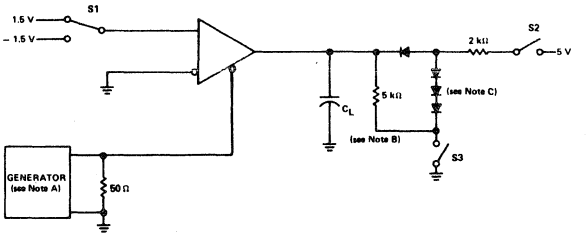


TEST CIRCUIT VOLTAGE WAVEFORMS

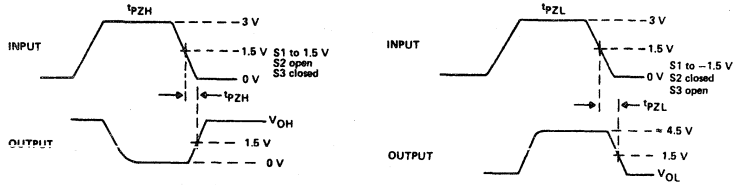
FIGURE 15–RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

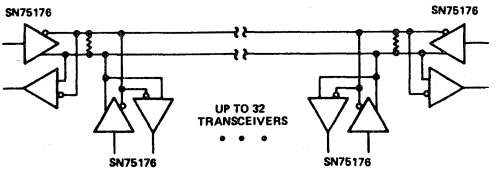


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 16–RECEIVER ENABLE AND DISABLE TIMES

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stubs lengths off the mainline should be kept as short as possible.

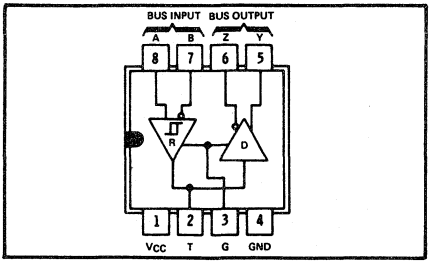
FIGURE 17

TYPES SN75177, SN75178 DIFFERENTIAL BUS REPEATERS

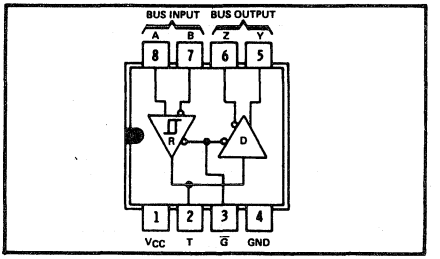
BULLETIN NO. DL-S 12793, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . –7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

SN75177 . . . JG or P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75178 . . . JG or P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

description

The SN75177 and SN75178 differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422A, EIA Subcommittee TR30.1 draft Standard PN1360, and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177 and SN75178 are identical except for the enable inputs, which are complementary, that is, on the SN75177 it is active-high and on the SN75178 it is active-low. These complementary enables allow the devices to be used in pairs for bidirectional communication.

SN75177 FUNCTION TABLE

DIFFERENTIAL INPUTS A–B	ENABLE G	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

SN75178 FUNCTION TABLE

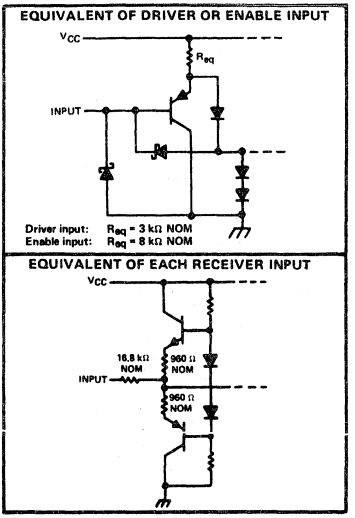
DIFFERENTIAL INPUTS A–B	ENABLE $\overline{G}$	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

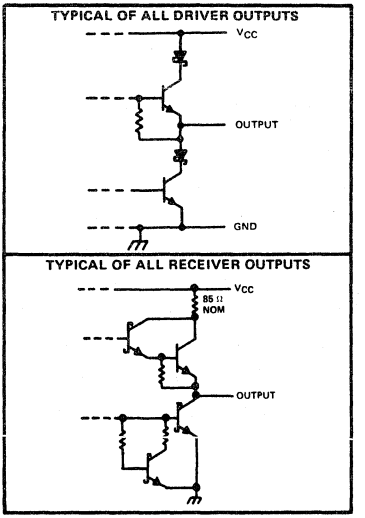
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

The SN75177 and SN75178 feature positive- and negative-current limiting and three-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of –12 volts to 12 volts. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150° C. The driver is designed to drive current loads up to 60 milliamperes maximum.

The SN75177 and SN75178 are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176 differential bus transceiver.

schematics of inputs and outputs





5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): JG Package . . . . . 830 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25° C free-air temperature, derate the JG package to 528 mW at 70° C at the rate of 6.6 mW/° C and the P package to 640 mW at 70° C at the rate of 8.0 mW/°C. In the JG package, SN75177 and SN75178 chips are glass-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in his data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 9	2	2.7		V
		R_L = 54 Ω,	See Figure 9	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 9			±0.2	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 11		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 12		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 13		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 14		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 13		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 14		18	30	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2¶			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 10		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 10	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				20	μA
						−360	
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: Refer to EIA standard RS-422A for exact conditions

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,			26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 15		27	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 16		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 16		26	35	ns
t_{PLZ}	Output disable time from low level				27	35	ns

TYPICAL CHARACTERISTICS

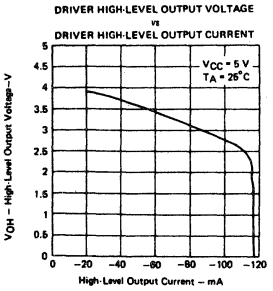


FIGURE 1

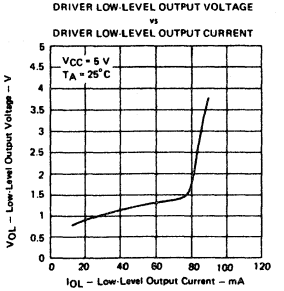


FIGURE 2

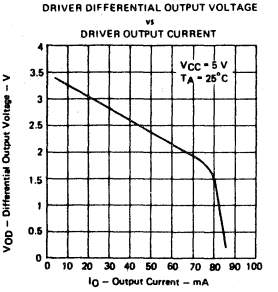


FIGURE 3

TYPICAL CHARACTERISTICS

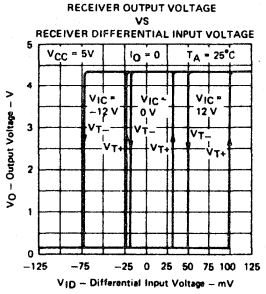


FIGURE 4

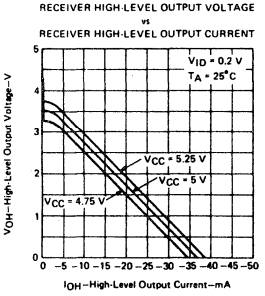


FIGURE 5

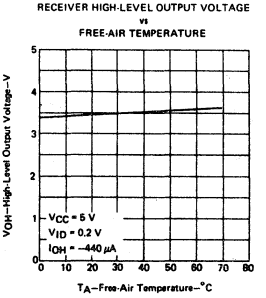


FIGURE 6

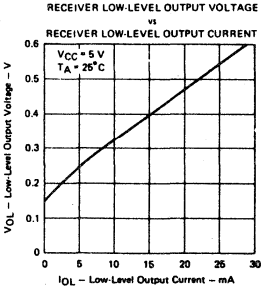


FIGURE 7

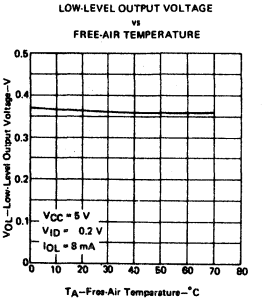


FIGURE 8

PARAMETER MEASUREMENT INFORMATION

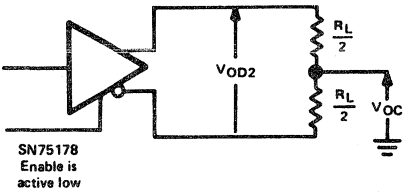


FIGURE 9–DRIVER V_{OD} AND V_{OC}

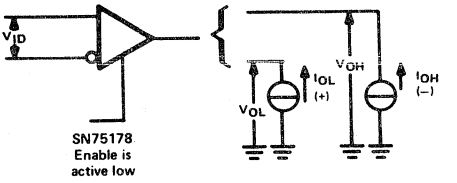


FIGURE 10–RECEIVER V_{OH} AND V_{OL}

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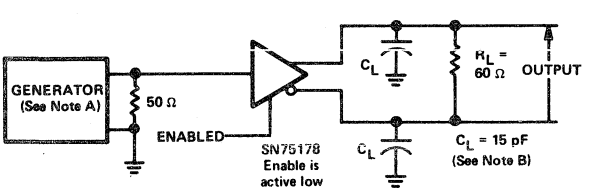
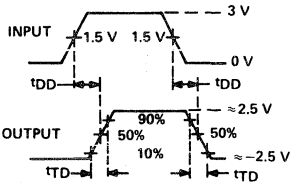
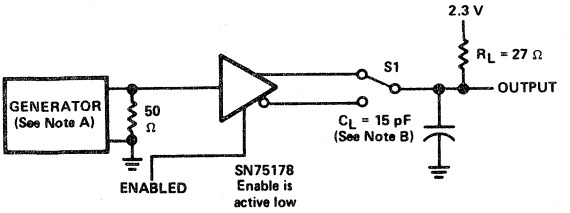


TEST CIRCUIT

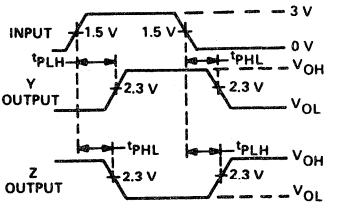


VOLTAGE WAVEFORMS

FIGURE 11–DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT

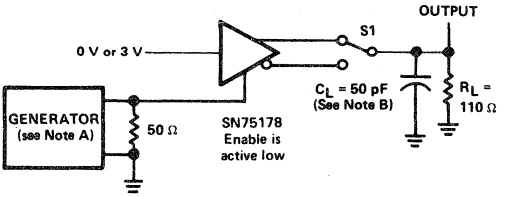


VOLTAGE WAVEFORMS

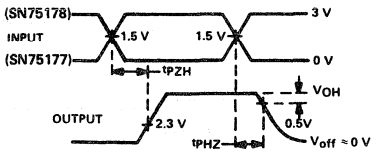
FIGURE 12–DRIVER PROPAGATION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

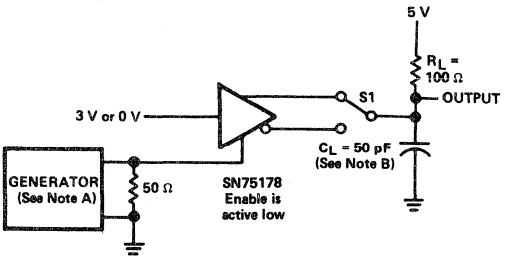


TEST CIRCUIT

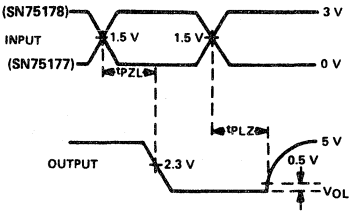


VOLTAGE WAVEFORMS

FIGURE 13–DRIVER ENABLE AND DISABLE TIMES (t_{PZH}, t_{PHZ})

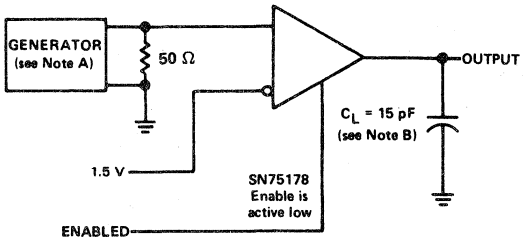


TEST CIRCUIT

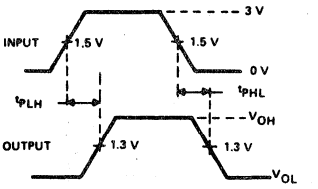


VOLTAGE WAVEFORMS

FIGURE 14–DRIVER ENABLE AND DISABLE TIMES (t_{PZL}, t_{PLZ})



TEST CIRCUIT

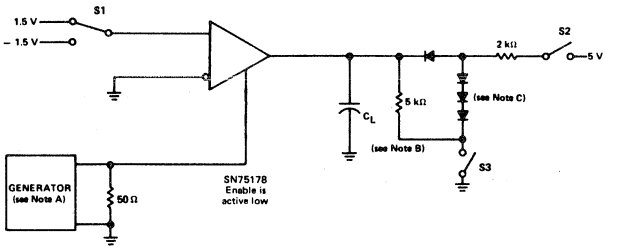


VOLTAGE WAVEFORMS

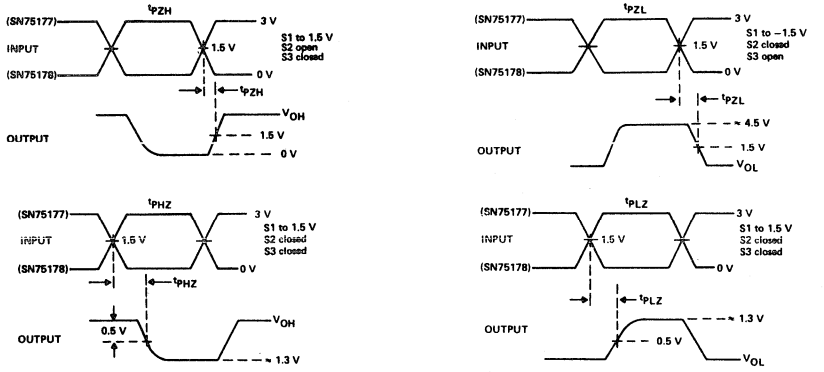
FIGURE 15–RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

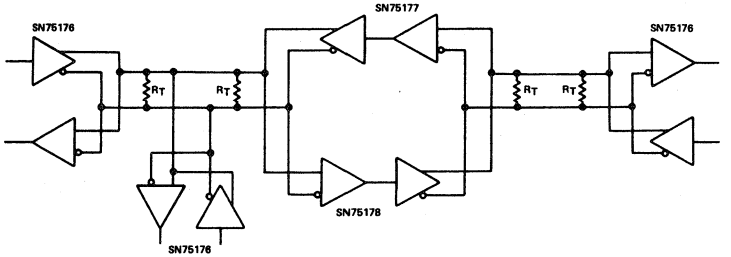


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 17–RECEIVER ENABLE AND DISABLE TIMES

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18

TYPES SN55182, SN75182, SN55183, SN75183 DUAL DIFFERENTIAL RECEIVERS AND DRIVERS

BULLETIN NO. DL-S 11767, OCTOBER 1972–REVISED JANUARY 1977

LINE CIRCUITS
featuring

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL/DTL Compatibility

additional features of SN55182 and SN75182 line receivers

- Designed to be Interchangeable with National Semiconductor DS7820A and DS8820A
- ±15 V Common-Mode Input Voltage Range
- ±15 V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls

additional features of SN55183 and SN75183 line drivers

- Designed to be Interchangeable with National Semiconductor DS7830 and DS8830
- Short-circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs

5

description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open-circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

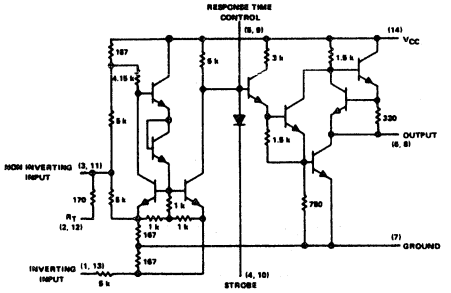
The SN55183 and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters as the output stages are similar to TTL totem-pole outputs.

Both the driver and receiver are of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55182 and SN55183 are characterized for operation over the full military temperature range of −55°C to 125°C and the SN75182 and SN75183 are characterized for operation from 0°C to 70°C. Both devices are available in either the ceramic (J) or plastic (N) dual-in-line package.

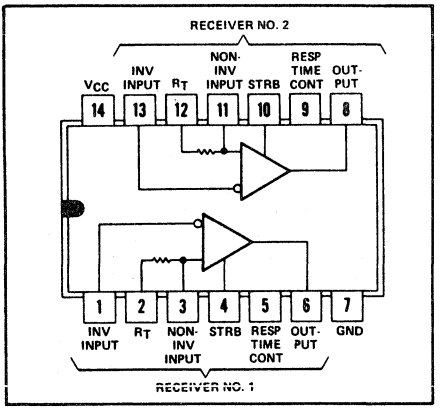
CONTENTS

schematic (each receiver)



Resistor values shown are nominal and in ohms.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

logic

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Common-mode input voltage	±20 V
Differential input voltage (see Note 2)	±20 V
Strobe input voltage	8 V
Output sink current	50 mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 3)	600 mW
Operating free-air temperature range: SN55182	−55°C to 125°C
SN75182	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
3. For operation of SN55182 above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, these chips are glass-mounted.

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

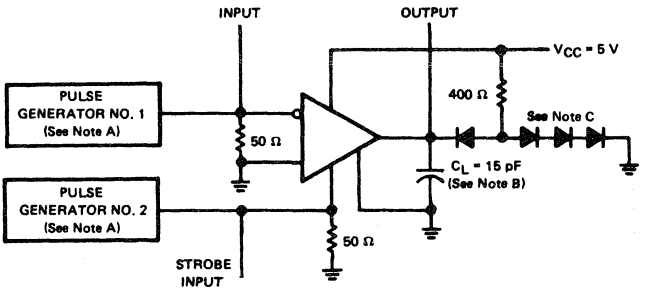
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{TH}	Differential input high-threshold voltage		V_O = 2.5 V, I_{OH} = −400 μA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{TL}	Differential input low-threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA,	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
$V_{IH(strobe)}$	High-level strobe input voltage				2.1		5.5	V
$V_{IL(strobe)}$	Low-level strobe input voltage				0		0.9	V
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 μA	V_{strobe} = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 μA	V_{strobe} = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	V_{strobe} = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0 V			0	0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0 V			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
I_{SH}	High-level strobe current		V_{strobe} = 5.5 V				5	μA
I_{SL}	Low-level strobe current		V_{strobe} = 0			−1	−1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
R_T	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

†Unless otherwise noted, $V_{strobe} \geq 2.1$ V or open.
‡All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

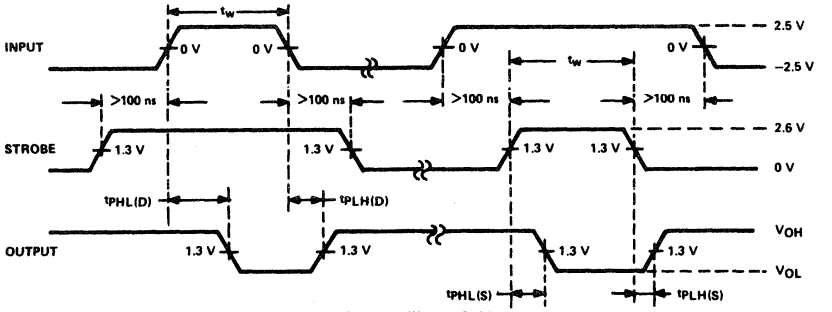
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ns, t_f = 10 ns, t_w = 0.5 ± 0.1 μs, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

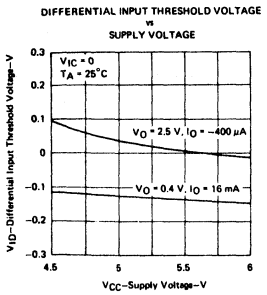


FIGURE 2

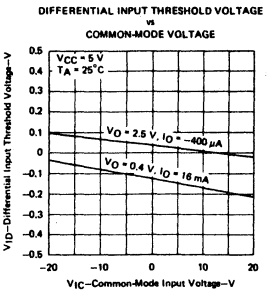


FIGURE 3

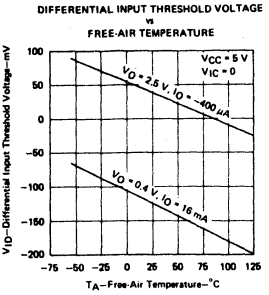


FIGURE 4

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

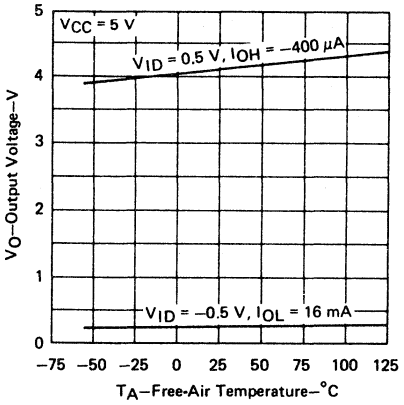


FIGURE 5

VOLTAGE TRANSFER CHARACTERISTICS

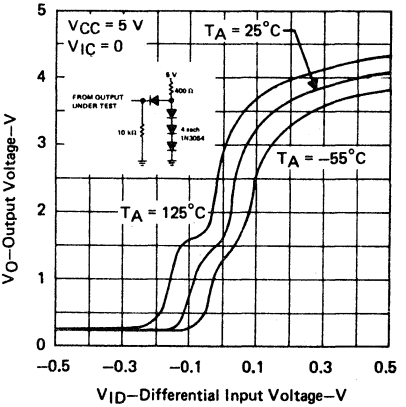


FIGURE 6

INPUT CURRENT
vs
INPUT VOLTAGE

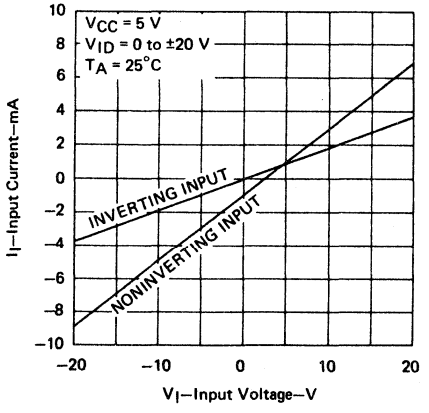


FIGURE 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

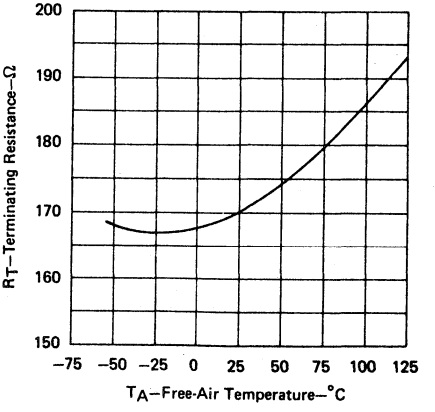


FIGURE 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE

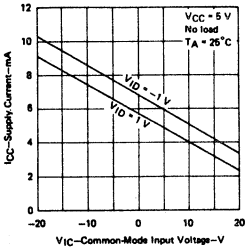


FIGURE 9

POWER DISSIPATION
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE

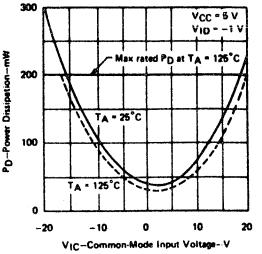


FIGURE 10

NOISE PULSE WIDTH
vs
RESPONSE-TIME-CONTROL CAPACITANCE

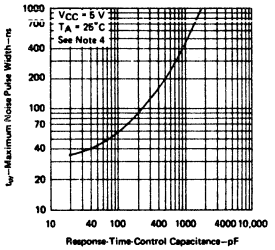
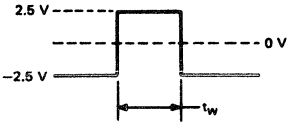


FIGURE 11



INPUT PULSE FOR FIGURE 11

PROPAGATION DELAY TIMES FROM
DIFFERENTIAL INPUT
vs
FREE-AIR TEMPERATURE

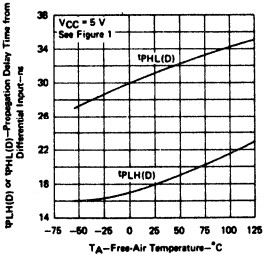


FIGURE 12

PROPAGATION DELAY TIMES FROM STROBE INPUT
vs
FREE-AIR TEMPERATURE

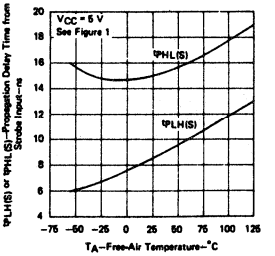
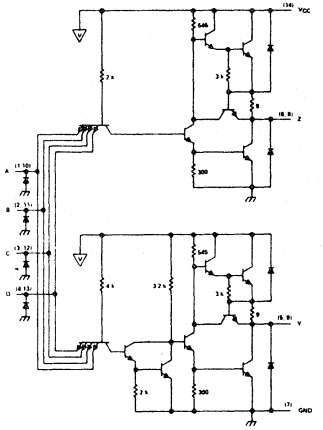


FIGURE 13

NOTE 4: Figure 11 shows the maximum width of the illustrated pulse that can be applied differentially without the output changing from the low to high level.

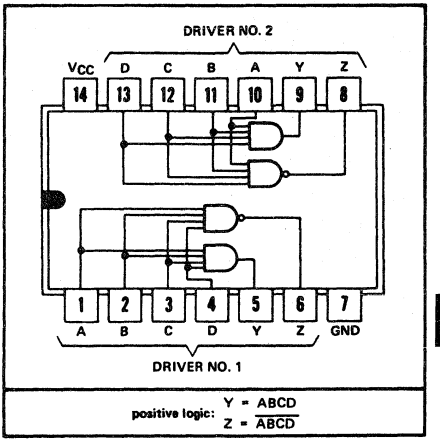
schematic (each driver)



Resistor values shown are nominal and in ohms.

▽ . . . V_{CC} bus

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Duration of output short-circuit (see Note 2) . . . . . 1 s
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3) . . . . . 600 mW
Operating free-air temperature range, SN55183 . . . . . −55°C to 125°C
SN75183 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at a time.
3. For operation of SN55183 above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, these chips are glass-mounted.

recommended operating conditions

	SN55183			SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	Y (AND) OUTPUT	V_{IH} = 2 V, I_{OH} = −0.8 mA	2.4			V
			V_{IH} = 2 V, I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IL} = 0.8 V, I_{OL} = 32 mA		0.2		V
			V_{IL} = 0.8 V, I_{OL} = 40 mA		0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) OUTPUT	V_{IL} = 0.8 V, I_{OH} = −0.8 mA	2.4			V
			V_{IL} = 0.8 V, I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IH} = 2 V, I_{OL} = 32 mA		0.2		V
			V_{IH} = 2 V, I_{OL} = 40 mA		0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V			120	μA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V			2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V			−4.8	mA
I_{OS}	Short-circuit output current§		V_{CC} = 5 V, T_A = 125°C	−40	−100	−120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V, All inputs at 5 V, No load		10	18	mA

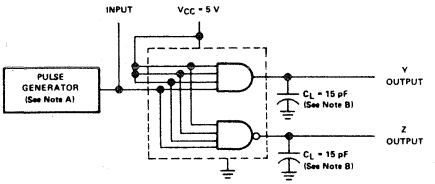
5

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one second.

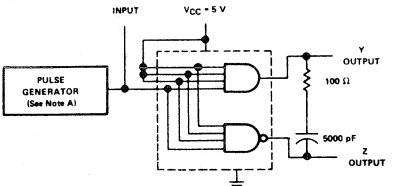
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Y output	AND gates	C_L = 15 pF, See Figure 14(a)		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Y output				12	18	ns
t_{PLH}	Propagation delay time, low-to-high-level Z output	NAND gates			6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Z output				6	8	ns
t_{PLH}	Propagation delay time, low-to-high-level differential output	Y output with respect to Z output	Z_L = 100 Ω in series with 5000 pF, See Figure 14(b)		9	16	ns
t_{PHL}	Propagation delay time high-to-low-level differential output				8	16	ns

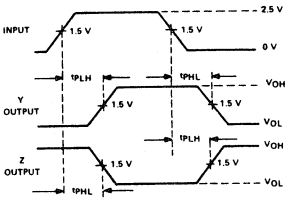
PARAMETER MEASUREMENT INFORMATION



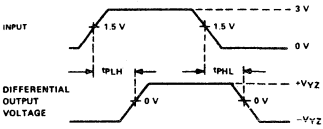
TEST CIRCUIT



TEST CIRCUIT



VOLTAGE WAVEFORMS
(a)—OUTPUTS Y AND Z



VOLTAGE WAVEFORMS
(b)—DIFFERENTIAL OUTPUT

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_r = 10 ns, t_f = 10 ns, t_w = 0.5 μs, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with R_{in} > 1 MΩ.

FIGURE 14—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

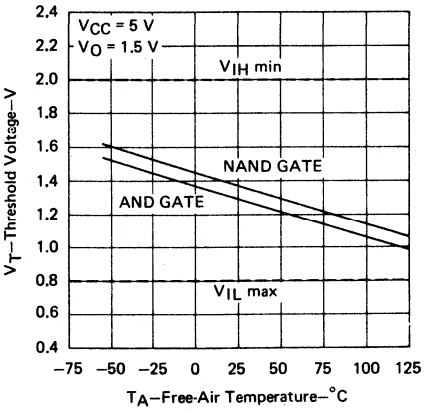


FIGURE 15

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

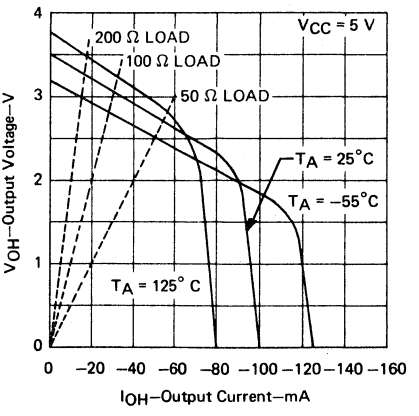


FIGURE 16

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

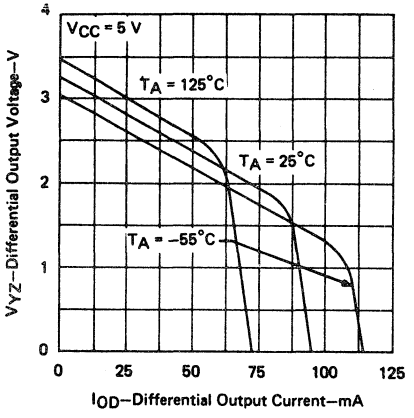


FIGURE 17

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

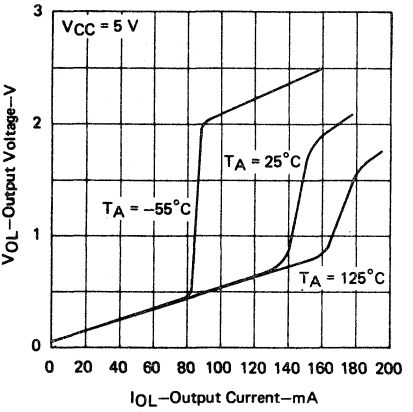


FIGURE 18

PROPAGATION DELAY TIME OF
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

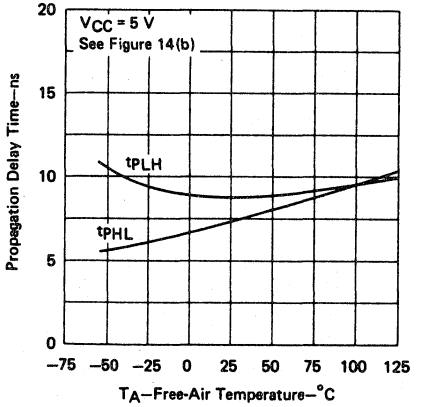


FIGURE 19

TOTAL POWER DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

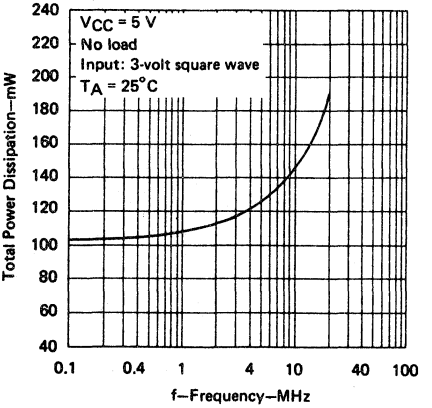
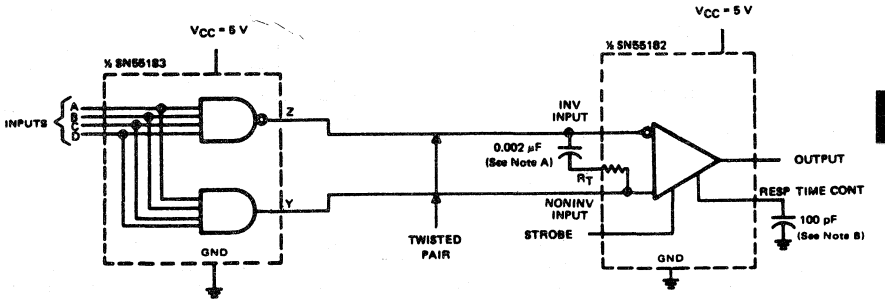


FIGURE 20

TYPICAL APPLICATION DATA



NOTES: A. When the inputs are open-circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\,(5 \times 10^{6})\,(0.002 \times 10^{-6})}$$

$$Z_C \approx 16\ \Omega$$

B. Use of a capacitor to control response time is optional.

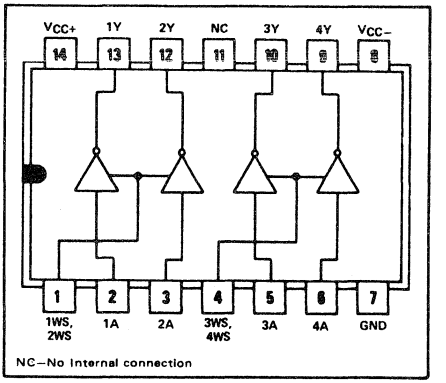
FIGURE 21—TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE

TYPE SN75186
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets EIA Standards RS-232C and RS-423A
- Wide Supply Voltage Range . . . ±7.5 V to ±15 V
- Low Supply Current . . . 4.5 mA Max per Channel
- Wave Shaping with External Resistors
- Inputs Compatible with TTL and CMOS
- Outputs at High Impedance when Power Is Off
- Positive- and Negative-Current Limiting
- SN75156 is Dual Version in 8-Pin Package

J OR N PACKAGE
(TOP VIEW)



NC—No Internal connection

description

The SN75186 consists of two pairs of single-ended line drivers designed to meet the requirements of EIA Standards RS-232C and RS-423A, CCITT Recommendations V.10, V.28, and X.26, and Federal Standard FIPS 1030. This device maintains regulated high and low output levels of 5.5 volts and −5.5 volts, respectively, over a wide range of power supply voltages. A high output impedance is maintained without the use of an external blocking diode. The output transition time of each pair of drivers can be adjusted from 1 microsecond to 100 microseconds by means of an external resistor at the waveshaping (WS) pin.

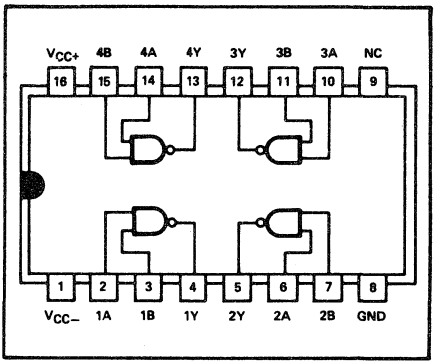
PRODUCT PREVIEW

TYPE SN75187
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets EIA Standard RS-423A
- Operates From ±5-V Supplies
- Minimum Unloaded Output Voltage Of ±4 V
- High-Impedance Output over ±6-V Common-Mode Range with Power Off (No external diode required)
- Low Power Dissipation . . . 60 mW Max per Channel
- Positive- and Negative-Current Limiting for Slew Rate Control

J OR N PACKAGE



description

The SN75187 is a single-ended line driver designed to meet the requirements of EIA Standard RS-423A. The unloaded output voltage is at least 4 volts and –4 volts for high and low levels, respectively, over the recommended ranges of supply voltage (±4.5 volts to ±5.5 volts) and temperature (0°C to 70°C). The fully loaded output voltages are greater than ±3.6 volts for the same conditions. The outputs maintain the high-impedance state when both power supplies are off over the common-mode input voltage range of –6 volts to 6 volts. Limiting is provided for both positive and negative currents to limit slew rates.

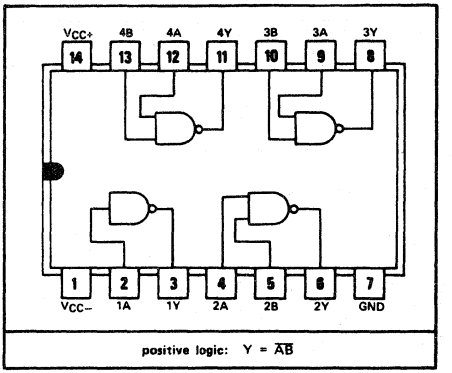
5

TYPE SN75188 QUADRUPLE LINE DRIVER

BULLETIN NO. DL-S 11874, SEPTEMBER 1973—REVISED JANUARY 1977

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with Motorola MC1488
- Current-Limited Output . . . 10 mA Typical
- Power-Off Output Impedance . . . 300 Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

description

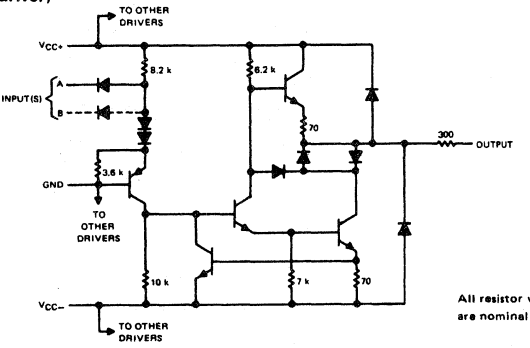
The SN75188 is a monolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C with a diode in series with each supply-voltage terminal as shown under typical applications. The device is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

schematic (each driver)



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2)	15 V
Supply voltage V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2)	−15 V
Input voltage range	−15 V to 7 V
Output voltage range	−15 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Maximum Supply Voltage Curve, Figure 6, and the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75188 chips are glass-mounted.

electrical characteristics over operating free-air temperature range, V_{CC+} = 9 V, V_{CC-} = −9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10	μA
I_{IL}	Low-level input current	V_I = 0				−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level ♦	V_I = 0.8 V,	V_O = 0	−6	−10	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level ♦	V_I = 1.9 V,	V_O = 0	6	10	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_{CC-} = 0, V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20	mA
			All inputs at 0.8 V		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25	
			All inputs at 0.8 V		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34	
			All inputs at 0.8 V			12	
I_{CC-}	Supply current from V_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17	mA
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23	
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34	
			All inputs at 0.8 V			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576	

†All typical values are at T_A = 25°C.
♦Not more than one output should be shorted at a time.

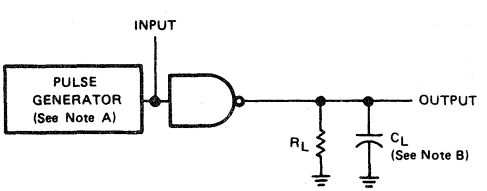
NOTE 4: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 9 V, V_{CC-} = −9 V, T_A = 25°C

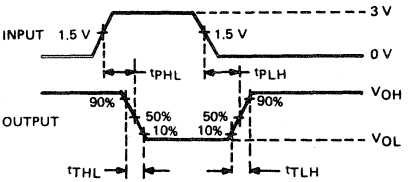
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ, C_L = 15 pF, See Figure 1		220	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	175	ns
t_{TLH}	Transition time, low-to-high-level output‡			55	100	ns
t_{THL}	Transition time, high-to-low-level output‡			45	75	ns
t_{TLH}	Transition time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		2.5		μs
t_{THL}	Transition time, high-to-low-level output§			3.0		μs

‡Measured between 10% and 90% points of output waveform.
§Measured between +3 V and −3 V points on the output waveform (EIA RS-232C conditions)

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS

5

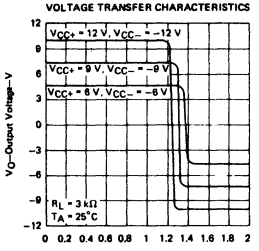


FIGURE 2

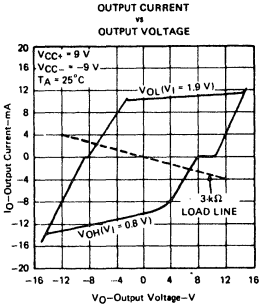


FIGURE 3

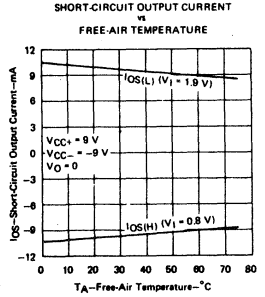


FIGURE 4

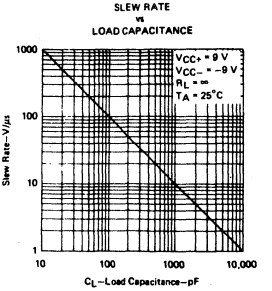


FIGURE 5

THERMAL INFORMATION

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

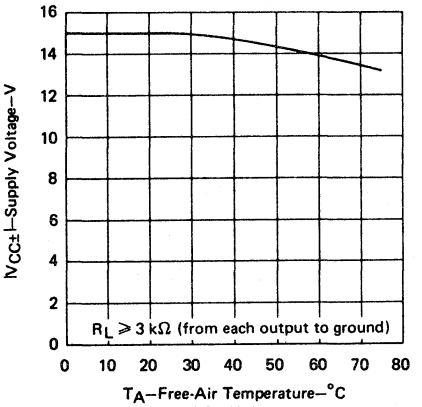


FIGURE 6

TYPICAL APPLICATION DATA

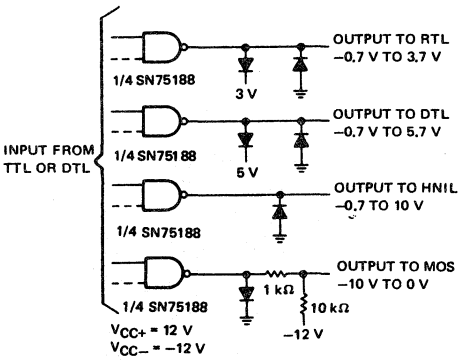


FIGURE 7—LOGIC TRANSLATOR APPLICATIONS

Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

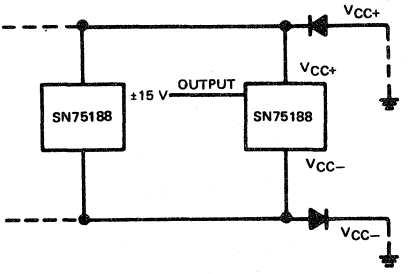


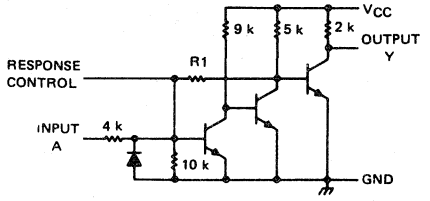
FIGURE 8—POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF EIA STANDARD RS-232C

TYPES SN75189, SN75189A QUADRUPLE LINE RECEIVERS

BULLETIN NO. DL-S 12035, SEPTEMBER 1973 – REVISED SEPTEMBER 1980

- Input Resistance . . . 3 kΩ to 7 kΩ
- Input Signal Range . . . ±30 V
- Fully Interchangeable with Mototola MC1489, MC1489A
- Operates From Single 5-V Supply
- Built-in Input Hysteresis (Double Thresholds)
- Response Control Provides:
  Input Threshold Shifting
  Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

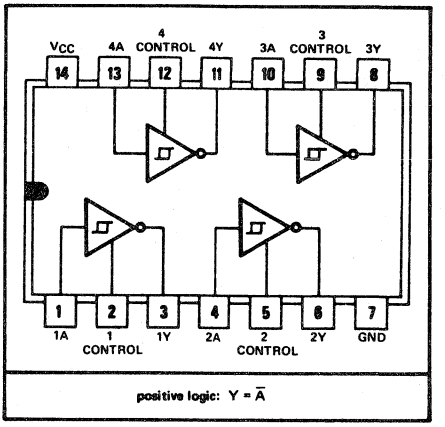
schematic (each receiver)



	SN75189	SN75189A
R1	10 k	2 k

Resistor values shown are nominal and in ohms.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

description

The SN75189 and SN75189A are monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage	±30 V
Output current	20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75189 and SN75189A chips are glass-mounted.

electrical characteristics over operating free-air temperature range, V_{CC} = 5V ± 1%, (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†		SN75189 MIN	SN75189 TYP‡	SN75189 MAX	SN75189A MIN	SN75189A TYP‡	SN75189A MAX	UNIT
V_{T+} Positive-going threshold voltage	1		T_A = 25°C	1		1.5	1.75	1.9	2.25	V
				0.9		1.6	1.55		2.25	
V_{T-} Negative-going threshold voltage	1		T_A = 25°C	0.75		1.25	0.75	0.97	1.25	V
				0.65		1.25	0.65		1.25	
V_{OH} High-level output voltage	1	V_I = 0.75 V,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	V
		Input open,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	
V_{OL} Low-level output voltage	1	V_I = 3 V,	I_{OL} = 10 mA		0.2	0.45		0.2	0.45	V
I_{IH} High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
		V_I = 3 V		0.43			0.43			
I_{IL} Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
		V_I = −3 V		−0.43			−0.43			
I_{OS} Short-circuit output current	3				−3			−3		mA
I_{CC} Supply current	2	V_I = 5 V,	Outputs open		20	26		20	26	mA

†All characteristics are measured with the response control terminal open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	4	C_L = 15 pF, R_L = 3.9 kΩ		25	85	ns
t_{PHL} Propagation delay time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		25	50	
t_{TLH} Transition time, low-to-high-level output		C_L = 15 pF, R_L = 3.9 kΩ		120	175	ns
t_{THL} Transition time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION§

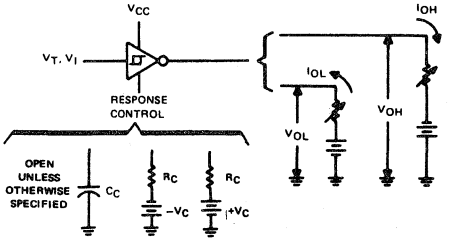
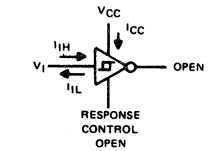


FIGURE 1–V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously

FIGURE 2–I_{IH}, I_{IL}, I_{CC}

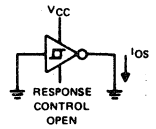
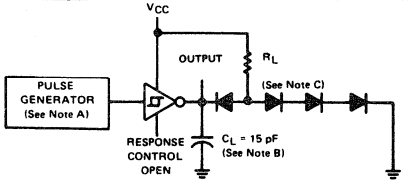
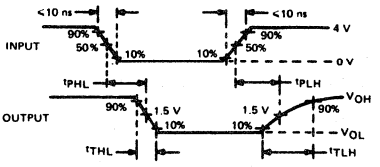


FIGURE 3–I_{OS}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, t_w = 500 ns.
B. C_L includes probe and jig capacitance. C. All diodes are 1N3064 or equivalent.

FIGURE 4–SWITCHING TIMES

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TYPICAL CHARACTERISTICS

SN75189
OUTPUT VOLTAGE vs INPUT VOLTAGE

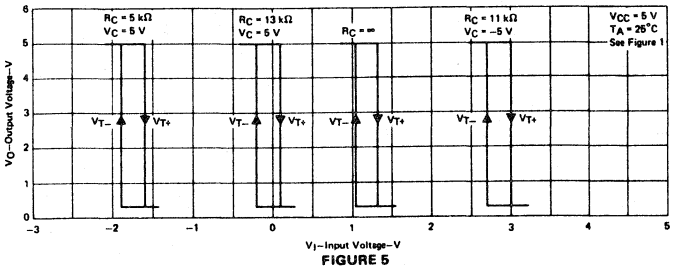


FIGURE 5

SN75189A
OUTPUT VOLTAGE vs INPUT VOLTAGE

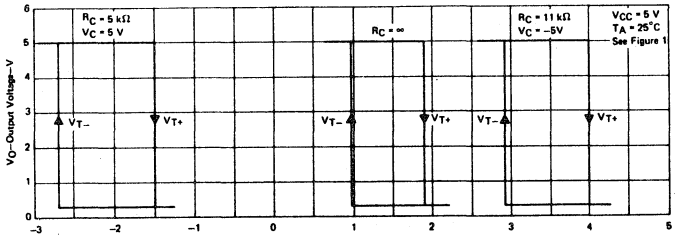


FIGURE 6

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

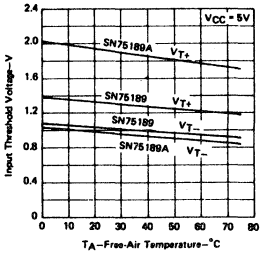


FIGURE 7

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

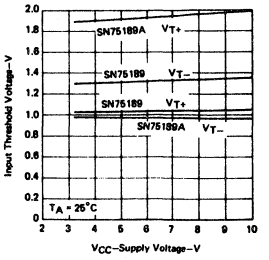


FIGURE 8

TYPICAL CHARACTERISTICS

SN75189
NOISE REJECTION

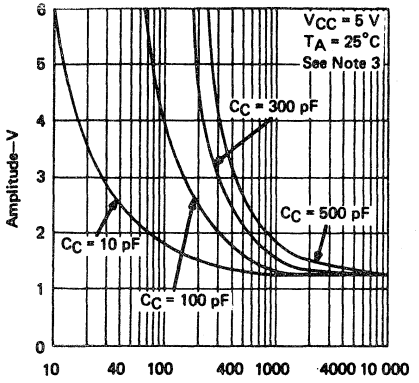


FIGURE 9

SN75189A
NOISE REJECTION

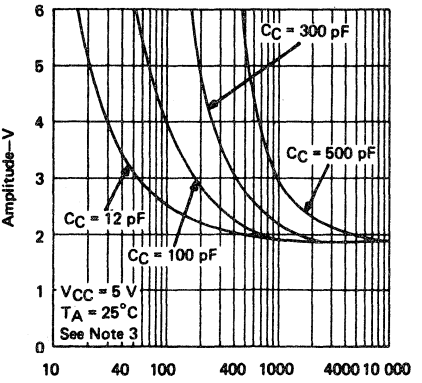


FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

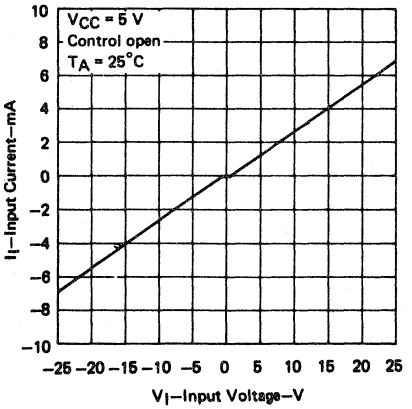


FIGURE 11

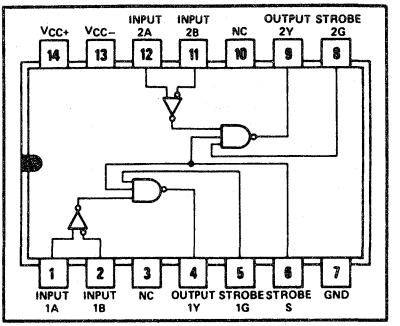
NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

TYPES SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

BULLETIN NO. DL-S 11793, JULY 1973–REVISED JANUARY 1977

- Plug-in Replacement for SN75107A, SN75107B, SN75108A, SN75108B with Improved Characteristics
- ±10 mV Guaranteed Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- '208 and '208B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN75207, SN75207B, SN75208, and SN75208B are pin-for-pin replacements for the SN75107A, SN75107B, SN75108A, and SN75108B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output. The '208 and '208B each features an open-collector output that permits wired-AND logic connections with similar output configurations. These devices are designed for operation from 0°C to 70°C and are available in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

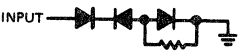
FUNCTION TABLE

DIFFERENTIAL INPUTS	STROBES		OUTPUT
A-B	G	S	Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

The essential difference between the unsuffixed and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

UNSUFFIXED VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

design characteristics

The '207, '207B, '208, and '208B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

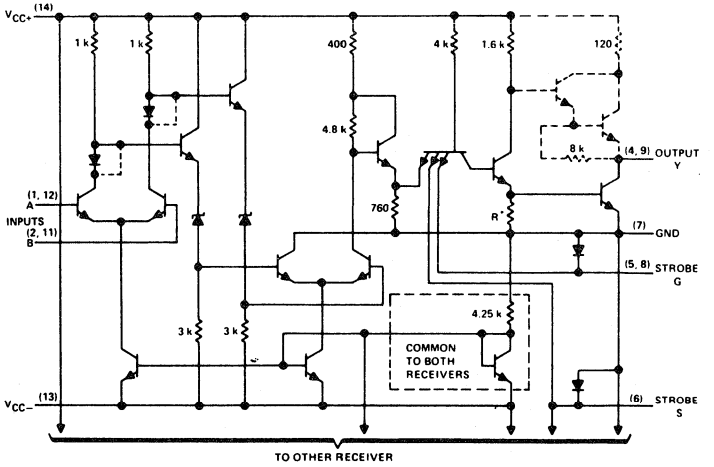
The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

5

schematic (each receiver)



*R = 1 kΩ for '207 and '207B, 750 Ω for '208 and '208B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '207 and '207B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '207 and '208.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

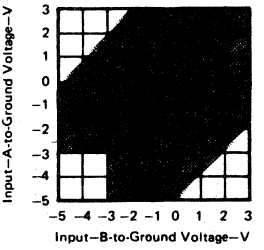
recommended operating conditions (see note 4)

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16	mA
Differential input voltage, V_{ID} (see Note 5)	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage range, any differential input to ground (see Note 5)	−5†		3	V
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
6. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.01	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.01	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

†The algebraic convention, where the more positive (less negative) limit is designated maximum, is used in this data sheet with logic input voltage levels only.

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

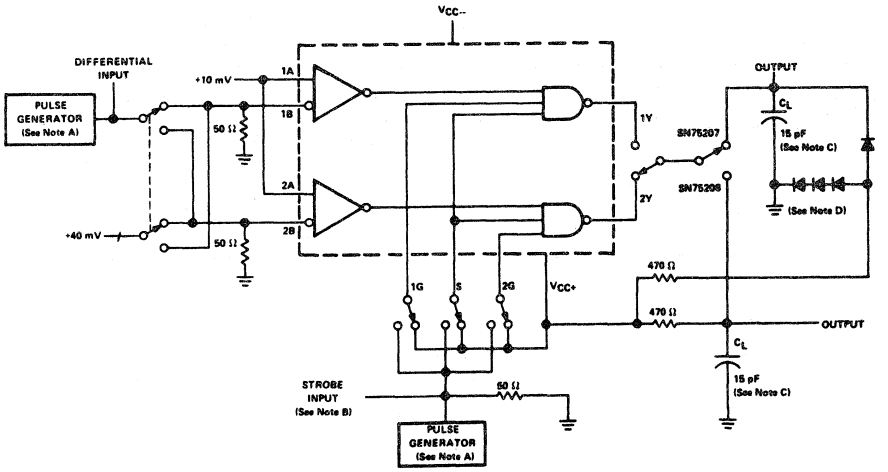
PARAMETER			TEST CONDITIONS‡		'207, '207B MIN	'207, '207B TYP§	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP§	'208, '208B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V	V_{IDH} = 10 mV,	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V	V_{IDL} = −10 mV,			0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

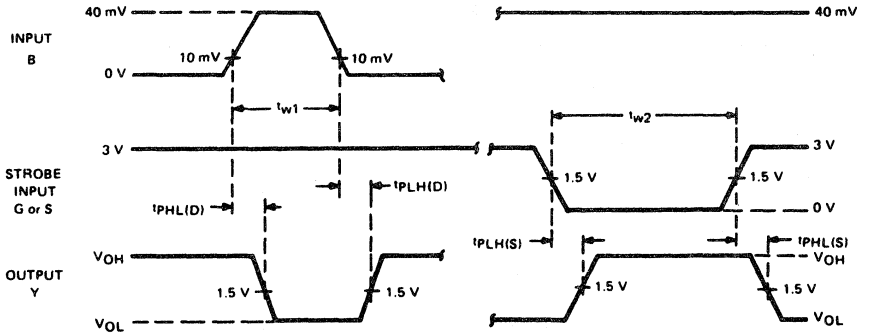
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'207, '207B MIN	'207, '207B TYP	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP	'208, '208B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 15 pF, See Figure 1			35			35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B				20			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S				17			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S				17			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

FIGURE 1—PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

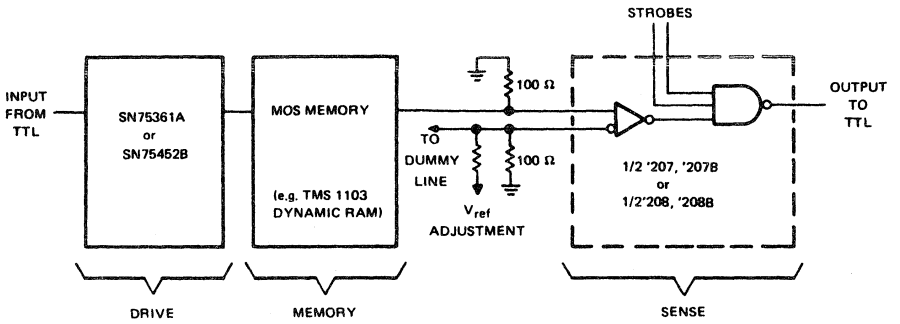
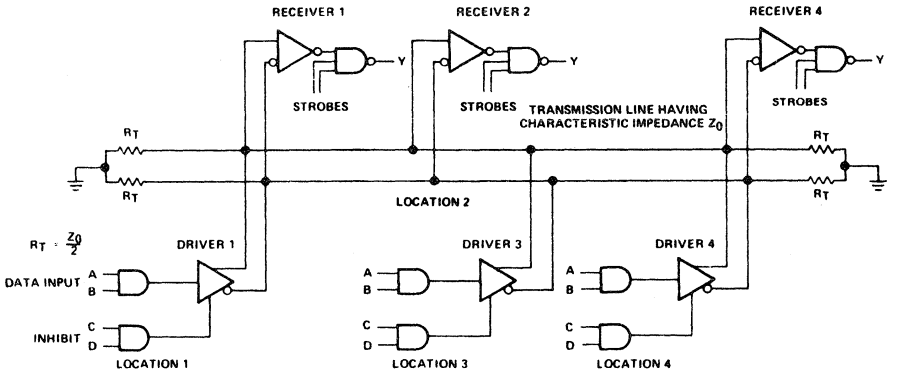


FIGURE 2–MOS MEMORY SENSE AMPLIFIER



Receivers are '207, '207B, '208, or '208B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3–DATA-BUS OR PARTY-LINE SYSTEM

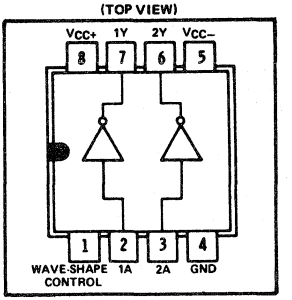
PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

TYPE uA9636AC
DUAL LINE DRIVERS WITH ADJUSTABLE SLEW RATE

BULLETIN NO. DL-S 12774, OCTOBER 1980

- **Meets EIA Standards RS-423, RS-232C, and Federal Standard 1030**
- **Slew Rate Control**
- **Output Short-Circuit-Current Limiting**
- **Wide Supply Voltage Range**
- **8-Pin Dual-In-Line Package**
- **Designed to be Interchangeable With Fairchild 9636A**

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The uA9636AC is a dual single-ended line driver designed to meet EIA Standards RS-423, RS-232C, and Federal Standard 1030. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS}, connected between the wave-shape-control terminal and ground. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode-protected against negative transients. This device operates from ±12 volts and is supplied in an 8-pin dual-in-line package.

The uA9636AC is characterized for operation from 0°C to 70°C.

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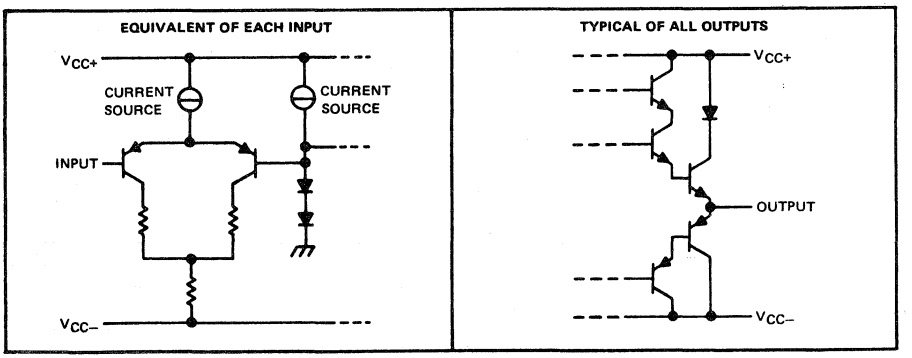
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage range, V_{CC+} (see Note 1) . . . . . V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} . . . . . 0.5 V to −15 V
Output voltage . . . . . ±15 V
Output current . . . . . ±150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate at the rate of 6.6 mW/°C for the JG package and 8.0 mW/°C for the P package.

5

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	−10.8	−12	−13.2	V
Operating free-air temperature, T_A	0		70	°C
Wave-shaping resistor, R_{WS}	10		1000	kΩ

electrical characteristics over recommended range of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

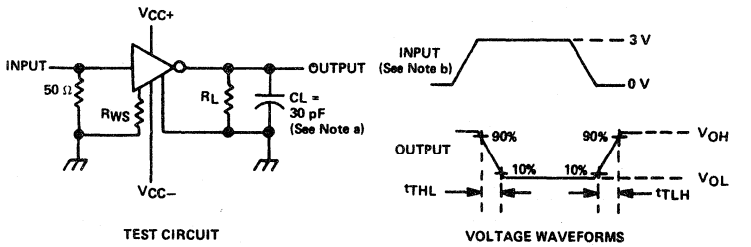
PARAMETER		TEST CONDITIONS		MIN	TYP† (See Note 3)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −15 mA			−1.1	−1.5	V
V_{OH}	High-level output voltage	V_I = 0.8 V	R_L = ∞	5	5.6	6	V
			R_L = 3 kΩ to ground	5	5.6	6	
			R_L = 450 Ω to ground	4	5.4	6	
V_{OL}	Low-level output voltage	V_I = 2 V	R_L = ∞	−6	−5.7	−5	V
			R_L = 3 kΩ to ground	−6	−5.6	−5	
			R_L = 450 Ω to ground	−6	−5.4	−4	
I_{IH}	High-level input current	V_I = 2.4 V				10	μA
		V_I = 5.5 V				100	
I_{IL}	Low-level input current	V_I = 0.4 V			−20	−80	μA
I_O	Output current (power off)	$V_{CC±}$ = 0,	V_O = ±6 V			±100	μA
I_{OS}	Short-circuit output current‡	V_I = 2 V		15	25	150	mA
		V_I = 0 V		−15	−40	−150	
r_o	output resistance	R_L = 450 Ω			25	50	Ω
I_{CC+}	Positive supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0 V, Output open		13	18	mA
I_{CC-}	Negative supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0 V, Output open		−13	−18	mA

†All typical values are at V_{CC} ± 12 V, T_A = 25°C.
‡Not more than one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one-second.
NOTE 3: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when −5 V is the maximum, the minimum is a more-negative voltage.

switching characteristics, $V_{CC\pm}$ = 12 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	µs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 MΩ	80	110	140	
t_{THL}	Transition time, high-to-low-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	µs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 MΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



NOTES: a. C_L includes probe and jig capacitance.
b. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f = 10$ ns, $Z_{out} = 50\ \Omega$, PRR = 1 kHz, duty cycle = 10%.

FIGURE 1 – TRANSITION TIMES

TYPICAL APPLICATION DATA

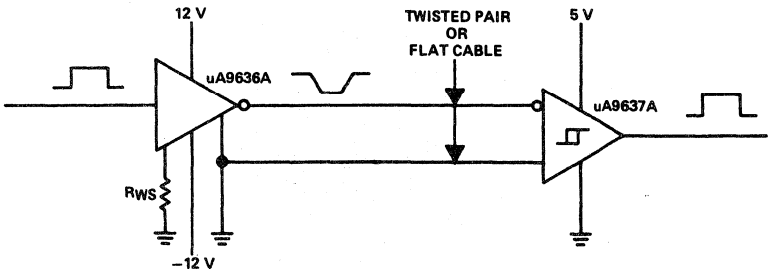


FIGURE 2 – RS-423 SYSTEM APPLICATION

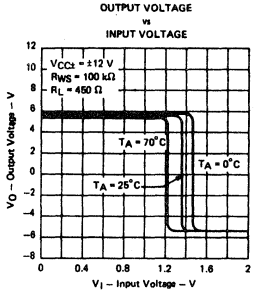


FIGURE 3

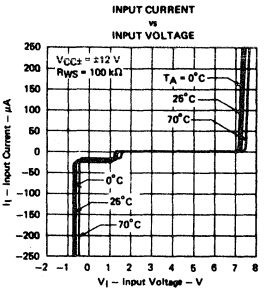


FIGURE 4

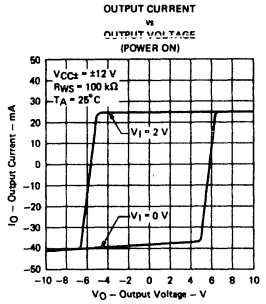


FIGURE 5

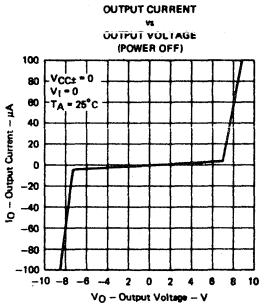


FIGURE 6

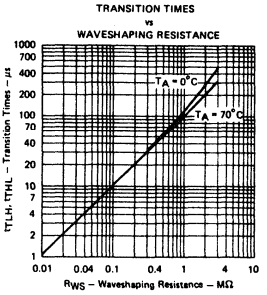


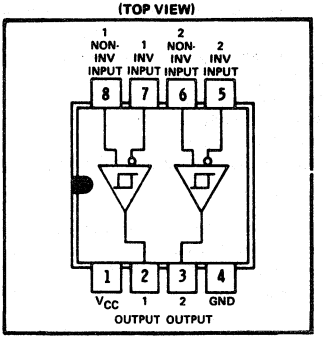
FIGURE 7

TYPE uA9637AC
DUAL DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12775, SEPTEMBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Input Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



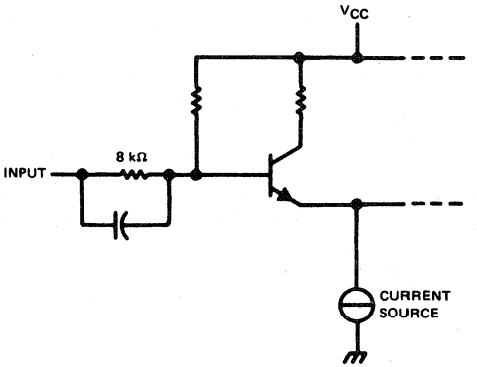
description

The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422A and RS-423A. It utilizes Schottky† circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

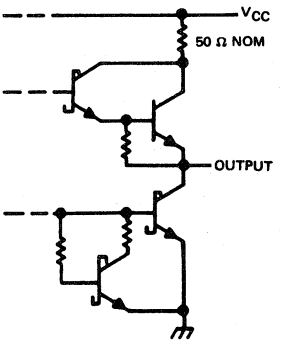
The uA9637AC is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mA
P package . . . . . 1000 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to the network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW. In the JG package, uA9637AC chips are glass-mounted.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP† (See Note 4)	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
$V_{T+} - V_{T-}$	Hysteresis				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit input current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

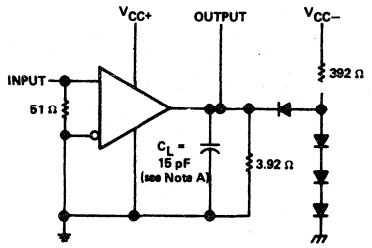
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

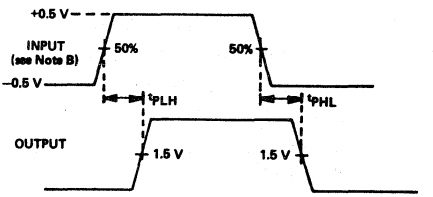
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f = 5$ ns, PRR = 5 MHz, duty cycle = 10%.

FIGURE 1–TRANSITION TIMES

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TYPICAL CHARACTERISTICS

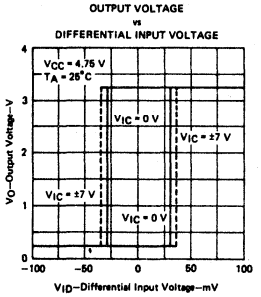


FIGURE 2

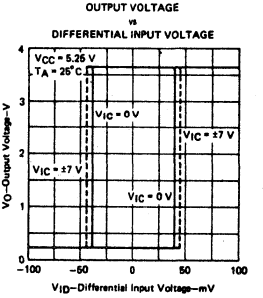


FIGURE 3

TYPICAL APPLICATION DATA

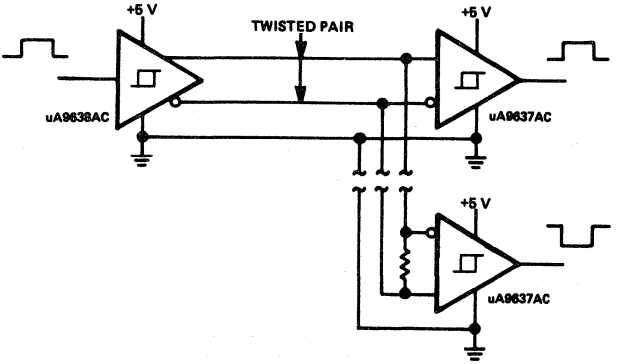


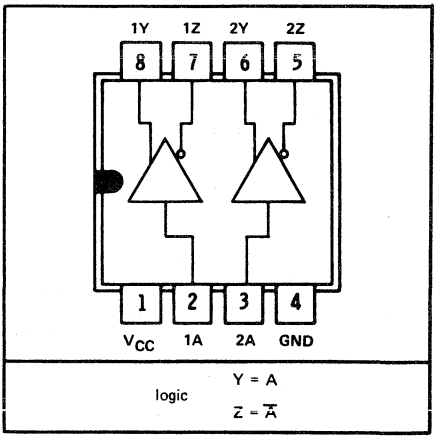
FIGURE 4–RS-422A SYSTEM APPLICATIONS

TYPE uA9638C
DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12780, OCTOBER 1980

- Meets EIA Standard RS-422A
- Operates From a Single 5-V Supply
- TTL and CMOS Input Compatibility
- Output Short-Circuit Protection
- Schottky Circuitry
- Designed to be Interchangeable with Fairchild 9638

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic

$Y = A$

$Z = \overline{A}$

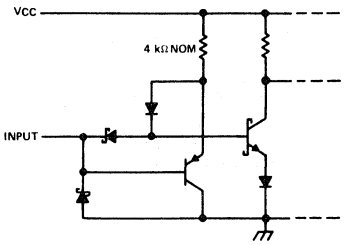
description

The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors† are used to minimize propagation delay time. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

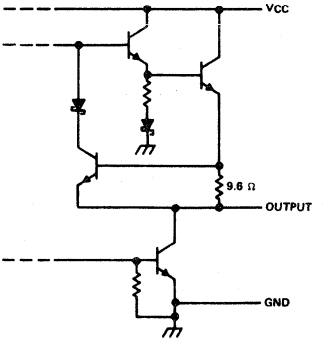
The uA9638C is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage range	−0.5 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 30 seconds: JG package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values except differential output voltages are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

TEXAS INSTRUMENTS
INCORPORATED

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
JG (Glass-Mounted Chip)	800 mW	6.6 mW/°C	29°C
P	800 mW	8.0 mW/°C	50°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −18 mA			−1	−1.2	V
V_{OH}	High level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.5	3.5		V
				I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1			2			V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of‡ differential output voltage						±0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of‡ common-mode output voltage						±0.4	V
I_O	Output current with power off	V_{CC} = 0,		V_O = 6 V		0.1	100	μA
				V_O = −0.25 V		−0.1	−100	
				V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V,	V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,			−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V,	No load,	All inputs at 0 V		45	65	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

¶Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		10	15	ns
t_{TD}	Differential-output transition time			10	15	ns
	Skew					ns

PARAMETER MEASUREMENT INFORMATION

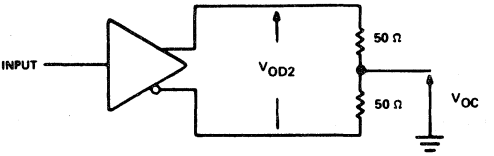
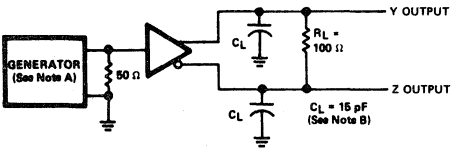
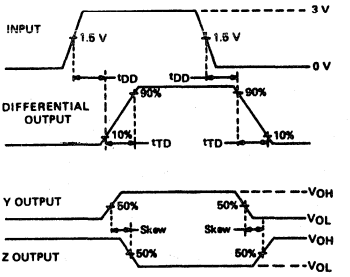


FIGURE 1– DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: a. The input pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
b. C_L includes probe and jig capacitance.

FIGURE 2 – SWITCHING TIMES

introduction

The systems designer is constantly faced with the problem of interfacing subsystems and of transmitting data over a distance, whether it is a few inches on a circuit board or many feet to another unit in the system. The quality of the signal reproduced in the receiving unit is dependent on:

A. Transmission line characteristics
   1. Length and attenuation
   2. Geometry (single wire, coaxial, parallel wires, twisted pair, shielded or unshielded, etc.)
      a. Characteristic impedance and line termination
      b. Distributed capacitance and inductance

B. General layout and noise environment

C. Receiver characteristics
   1. Input impedance
   2. Sensitivity, hysteresis, and input threshold
   3. Frequency response (switching time)

D. Driver characteristics
   1. Output impedance
   2. Output peak current capability
   3. Frequency response

E. Bit rate and pulse duration $\left(\text{bit rate} = \frac{2}{\text{period}}\right)$

The impact of many of these factors is discussed on the following pages and in several data sheets. Other applications where line circuit characteristics can be used to advantage are also discussed. For convenient access to all the application information in this data book, a topical index is provided on the next page.

additional circuit design information

Bulletin CA-130, *Line Drivers and Receivers: SN55107 Series*, and Bulletin CA-146, *Data Transmission with SN55107 Series*, are available from Texas Instruments upon request.

The Texas Instruments videotape course "Linear and Interface Integrated Circuits" is available for a nominal fee.

INDEX TO APPLICATION TOPICS

line terminations

The voltage across an impedance terminating a transmission line is a function of the real and imaginary components of the impedance, the characteristic impedance of the line, and the incident power. When the impedance is a pure resistance (see Note 1) and the transmission line is ideal, then:

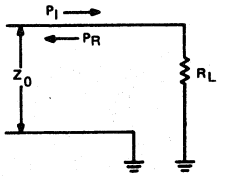


FIGURE 1

$$P_R = P_I \left(\frac{R_L - Z_0}{R_L + Z_0} \right)^2 \quad (1)$$

$$P_L = P_I - P_R = P_I \left[1 - \left(\frac{R_L - Z_0}{R_L + Z_0} \right)^2 \right] \quad (2)$$

$$V_L = \sqrt{P_L R_L} = \sqrt{I_L^2 R_L^2} \quad (3)$$

where

P_I = incident power
P_L = power delivered to R_L
P_R = reflected power
Z_0 = line characteristic impedance
R_L = load resistance

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When $R_L = Z_0$, the numerators of the fractional terms in Equations 1 and 2 become zero and the reflected power is zero. With reflections reduced to zero, one source of signal distortion and noise is eliminated. Equation 3 shows the relationship between P_L, R_L, V_L, and I_L.

In line circuit design R_L is a lumped value representing the combination of a termination resistor and the input resistance of a line receiver.

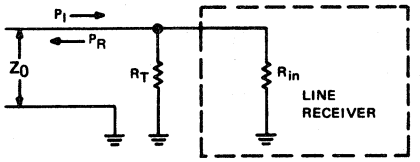


FIGURE 2

$$V_L = \sqrt{P_L \frac{R_{in} \times R_T}{R_{in} + R_T}} \quad (4)$$

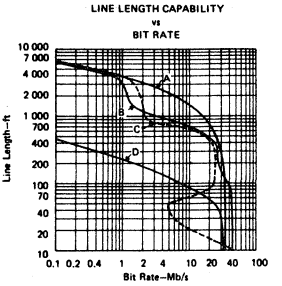
When $R_{in} \gg R_T$, the incoming signal power and noise power are shunted to ground by R_T, decreasing the effective power to the input of the receiver.

NOTE 1: The assumption that the terminating impedance is a pure resistance simplifies this discussion. In practice, the reactive components of impedance can usually be neglected.

line terminations (continued)

Figure 3 illustrates how much the line length versus bit rate boundary for acceptable TTL signals was affected by variation of the termination resistor values. Case A clearly provides the best capability for high bit rates and long transmission lines, while Cases B and C show irregularities primarily due to reflected signals.

	R1	R2
Case A	100 Ω	100 Ω
Case B	∞	100 Ω
Case C	∞	122 Ω
Case D	∞	205 Ω



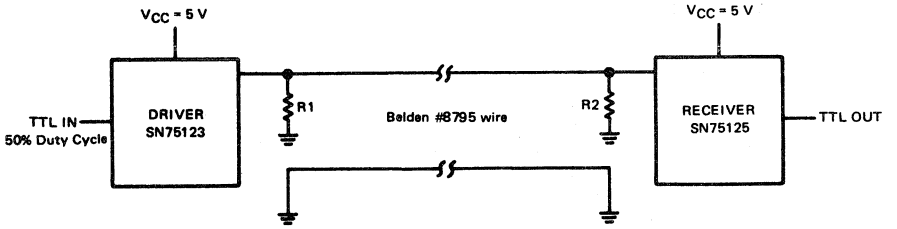
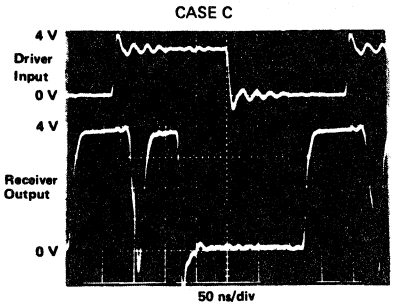


FIGURE 3

The voltage waveform for Case C at a line length of 50 feet shows a large negative transient in the receiver output due to a reflection. At 10 feet, the bit rate capability (see Figure 3) has increased to 45 Mb/s compared to 47 Mb/s for Case B.

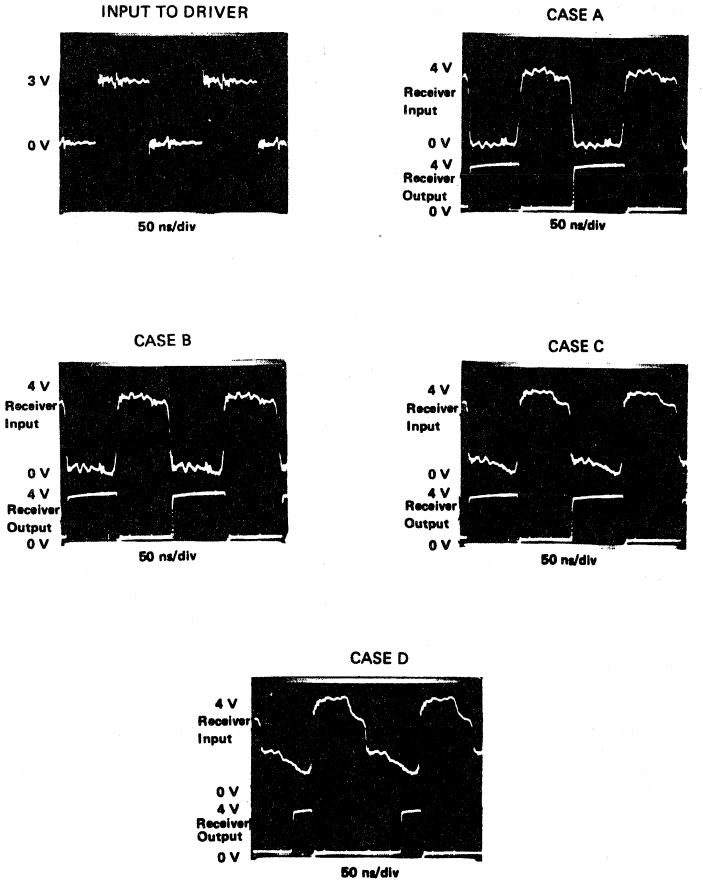


Bit Rate = 5.4 Mb/s
Line Length = 50 feet
VOLTAGE WAVEFORM

line terminations (continued)

The waveforms below offer an interesting comparison of the driver input signal to the resulting signals that appear at the receiver input and at the receiver output. The circuit of Figure 3 with 100 feet of line and a bit rate of 2 Mb/s was used. Note that the pulse duration for Case D receiver output is much shorter than the apparent duration of the input pulse. Case C, with somewhat less distortion, produces input and output pulse widths of about the same value.

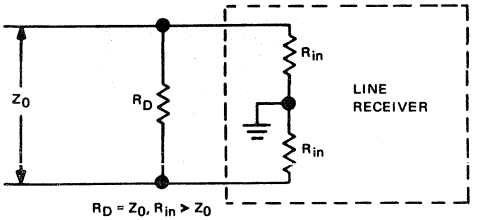
VOLTAGE WAVEFORMS



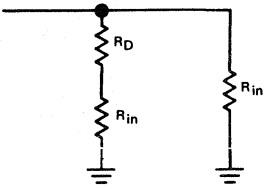
noise

The environment of any transmission line will produce noise from many sources. That noise will be transmitted to the input of the line receiver and can cause severe signal distortion. The familiar differential-line technique has provided a means of reducing the effect of common-mode noise on low-level signals in linear, digital, and rf transmission for some time, and is thoroughly discussed in the literature. One method of reducing the common-mode noise on balanced lines will be presented in this topic.

The noise power present on a line terminated in a resistance will act in the same manner as the signal power in Equations 1 through 4 under Line Terminations. Specifically, the noise will be shunted to ground and will not provide power to the receiver input if the line is terminated in a low-value resistor to ground. Examples 1 and 2 below show two typical means of terminating differential lines at the receiver.



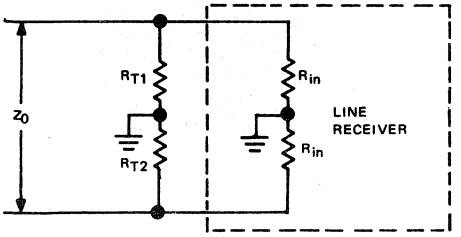
$R_D = Z_0$, $R_{in} > Z_0$



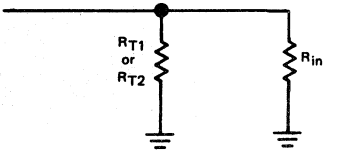
Equivalent Circuit of Each Input

EXAMPLE 1

Since the shunting resistance, $R_D + R_{in}$, is high, most of the noise on each conductor will appear at the receiver input.



$R_{T1} = R_{T2}$, $R_{T1} + R_{T2} = Z_0$, $R_{in} > Z_0$



Equivalent Circuit of Each Input

EXAMPLE 2

Most of the noise power on each conductor of the balanced line will be shunted to ground by R_{T1} or R_{T2} because of their low value compared to R_{in}.

noise (continued)

Figure 1 below illustrates the effectiveness of the differential-line technique in rejecting noise from an external source.

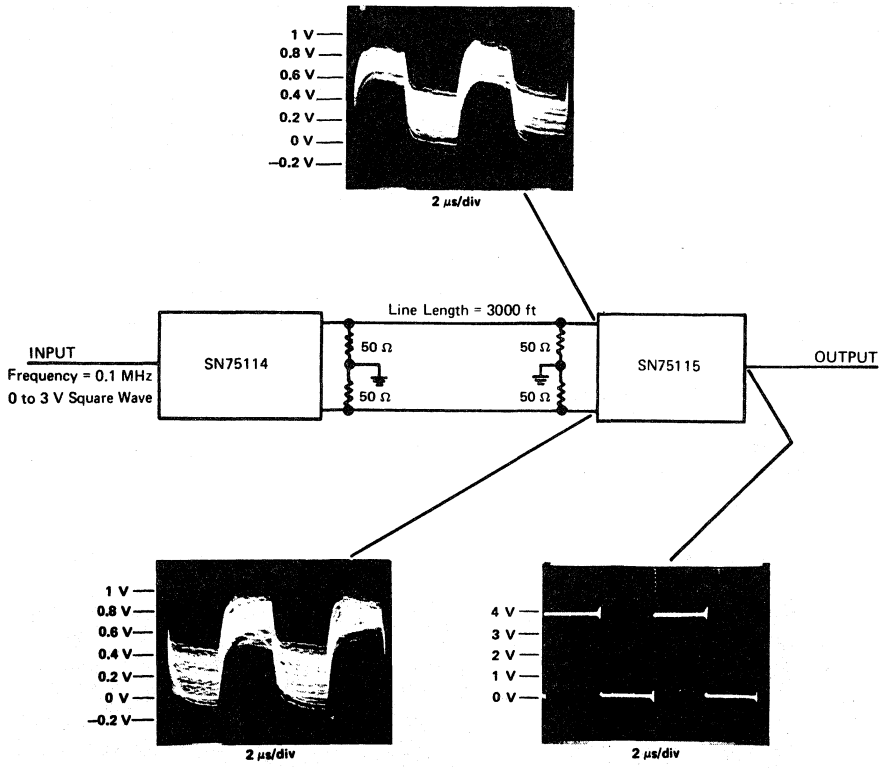


FIGURE 1

line length capability vs bit rate

The data presented in this section is intended to assist the designer who must choose a combination of line driver and receiver to meet line length and bit rate requirements. It does not represent the complete set of available options, but offers a means of comparison for many device types in typical applications. Each graph is associated with a specific line termination scheme, and all measurements utilized Belden #8795 wire as transmission line (see Note 1).

The duty cycle value refers to the time at TTL high level divided by the period length.

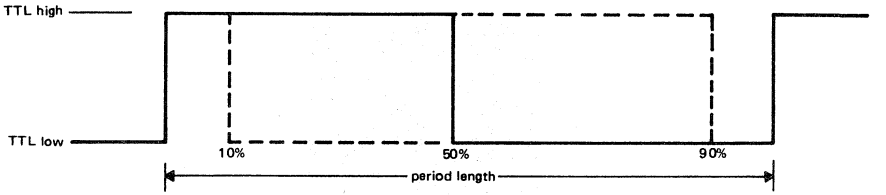


FIGURE 1– PERIOD AND DUTY CYCLE

Duty cycle and bit rate values will yield the high-level pulse duration by means of the formula:

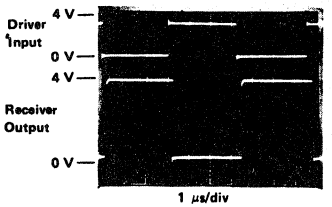
$$\text{Pulse duration} = \text{period} \times \text{duty cycle} = \frac{2}{\text{bit rate}} \times \text{duty cycle}$$

The data on the following pages was obtained in each case by monitoring the output of the receiver. Acceptable waveforms exhibited:

1. TTL low level less than 0.4 V
2. TTL high level greater than 2.4 V
3. No oscillations

Figures 2 and 3 show examples of acceptable and unacceptable voltage waveforms with regard to oscillations of the SN75112 driver and SN75207 receiver.

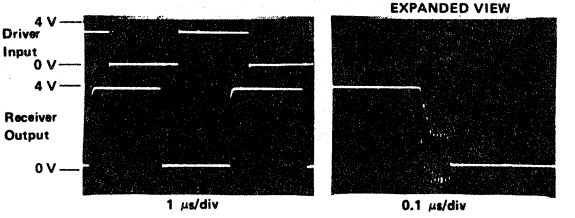
ACCEPTABLE VOLTAGE WAVEFORM



Bit Rate = 0.3 Mb/s
Line Length = 2000 ft

FIGURE 2

UNACCEPTABLE VOLTAGE WAVEFORMS



Bit Rate = 0.3 Mb/s, Line Length = 5000 ft

FIGURE 3

NOTE 1: Belden #8795 twisted-pair wire is 22 AWG and exhibits the following characteristics: $Z_0 \approx 100\ \Omega$, C ≈ 15 pF/ft, propagation delay ≈ 1.3 ns/ft.

LINE LENGTH CAPABILITY vs BIT RATE

INDEX TO DATA

DRIVER APPLICATIONS

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SN75121	31
SN75123	32, 33
SN75138	34
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SN75158	41
SN75183	11, 14
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SN75450B	44
SN75451B	16, 17, 18, 19, 20
SN75361A	21, 22, 23, 24, 25
DS8831	12, 15, 26, 27, 28, 29, 30
DS8832	12, 15, 26, 27, 28, 29, 30

RECEIVER APPLICATIONS

TYPE	FIGURE NUMBERS
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SN75116	42
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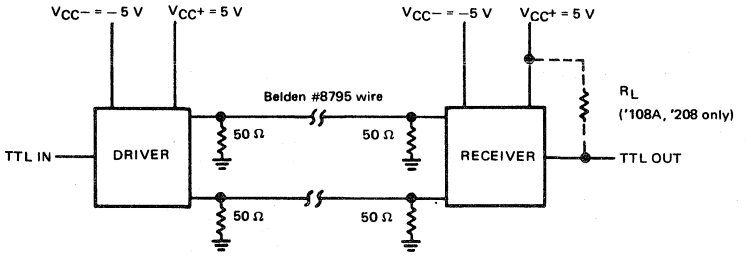
SN75189	35, 39
SN75189A	36, 40
SN75207	4, 5, 6
SN75208	7, 8, 9, 41

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 4 THRU 9

5

DRIVER SN75109A
RECEIVER SN75107A, SN75207

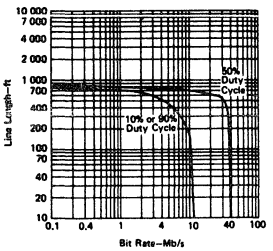


FIGURE 4

DRIVER SN75110A
RECEIVER SN75107A, SN75207

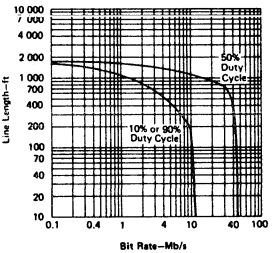


FIGURE 5

DRIVER SN75112
RECEIVER SN75107A, SN75207

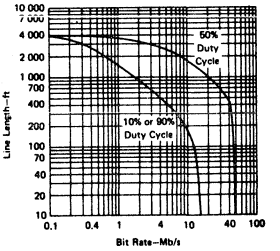


FIGURE 6

DRIVER SN75109A
RECEIVER SN75108A, SN75208

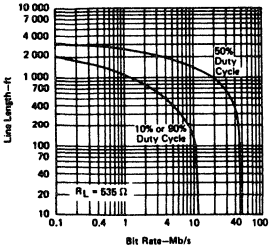


FIGURE 7

DRIVER SN75110A
RECEIVER SN75108A, SN75208

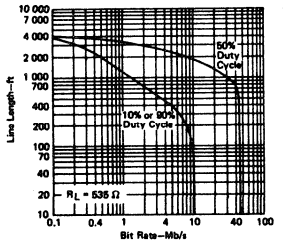


FIGURE 8

DRIVER SN75112
RECEIVER SN75108A, SN75208

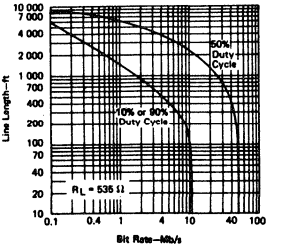
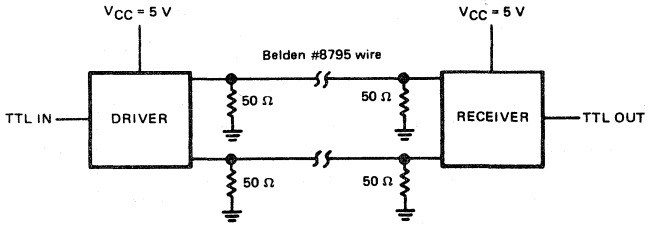


FIGURE 9

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 10 THRU 15

5

DRIVER . .SN75113, SN75114
RECEIVER SN75182

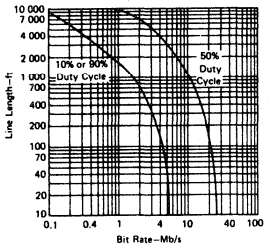


FIGURE 10

DRIVER SN75183
RECEIVER SN75182

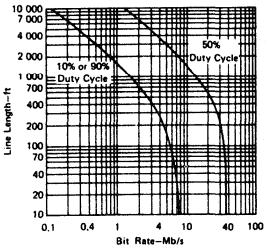


FIGURE 11

DRIVER . . .DS8831, DS8832
RECEIVER SN75182

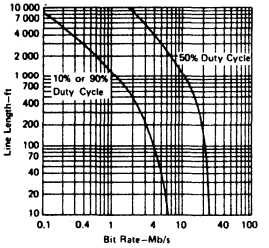


FIGURE 12

DRIVER . . .SN75113, SN75114
RECEIVER SN75115

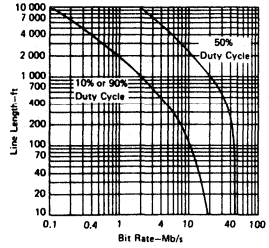


FIGURE 13

DRIVER SN75183
RECEIVER SN75115

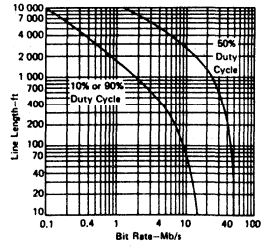


FIGURE 14

DRIVER . . .DS8831, DS8832
RECEIVER SN75115

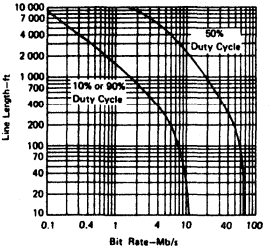
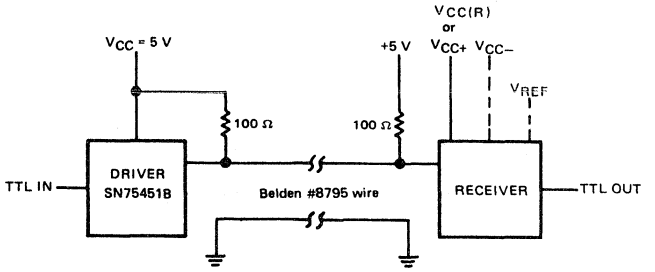


FIGURE 15

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 16 THRU 20

5

RECEIVER SN75115

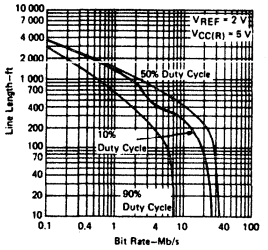


FIGURE 16

RECEIVER SN75122

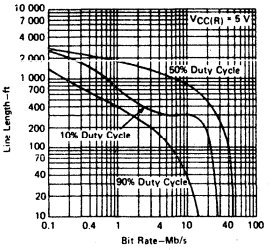


FIGURE 17

RECEIVER SN75140

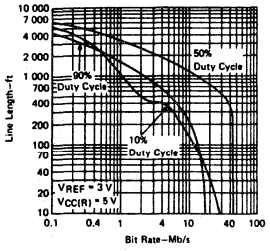


FIGURE 18

RECEIVER SN75152

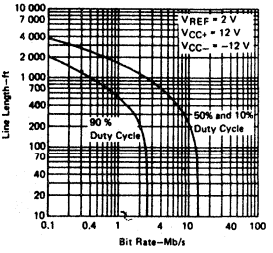


FIGURE 19

RECEIVER SN75182

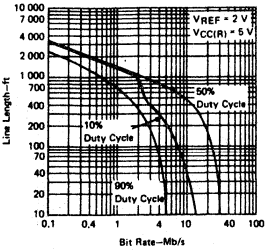
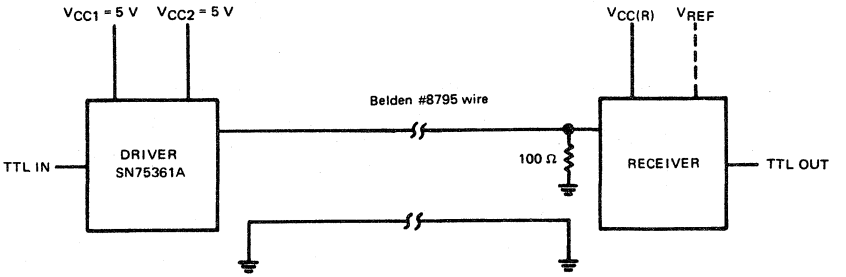


FIGURE 20

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 21 THRU 25

5

RECEIVER SN75115

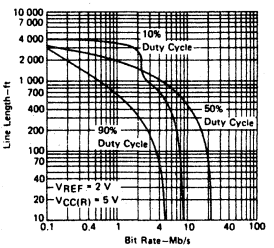


FIGURE 21

RECEIVER SN75122

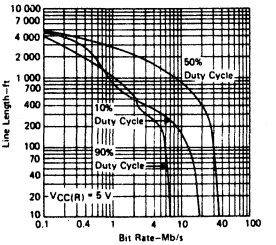


FIGURE 22

RECEIVER SN75140

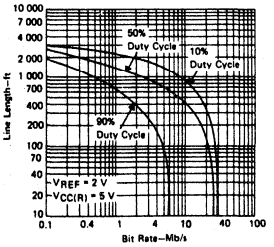


FIGURE 23

RECEIVER SN75152

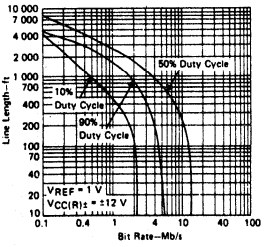


FIGURE 24

RECEIVER SN75182

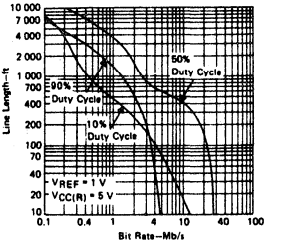
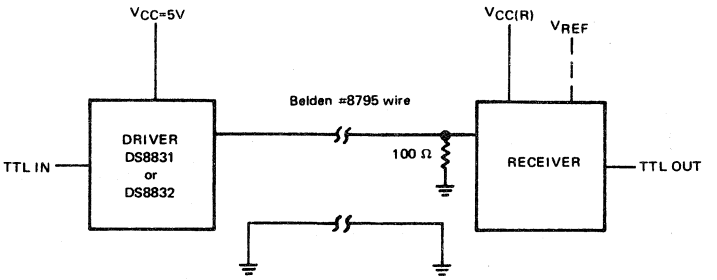


FIGURE 25

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 26 THRU 30

5

RECEIVER . . . SN75122

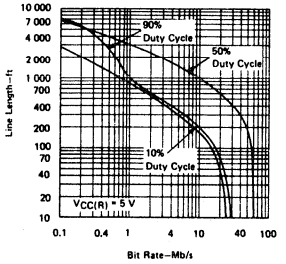


FIGURE 26

RECEIVER . . . SN75124

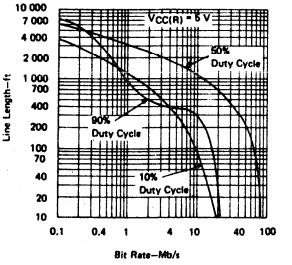


FIGURE 27

RECEIVER SN75125, SN75127

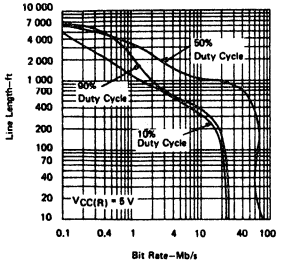


FIGURE 28

RECEIVER . . . SN75140

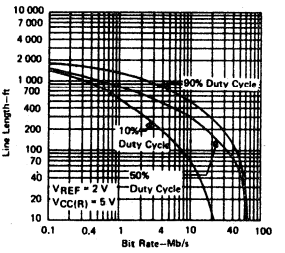


FIGURE 29

RECEIVER . . . SN75152

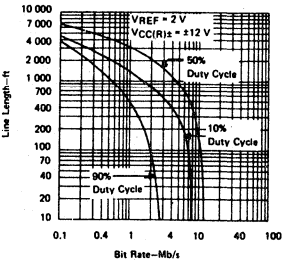
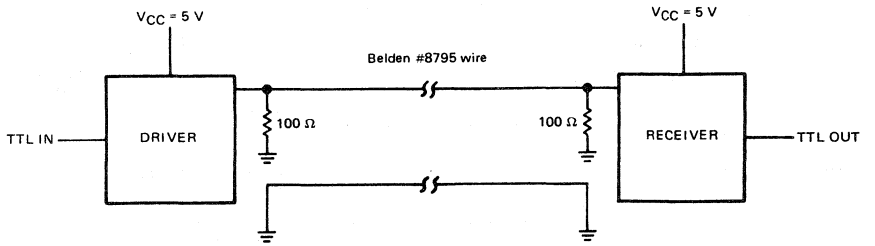


FIGURE 30

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 31 THRU 33

DRIVER SN75121
RECEIVER SN75122

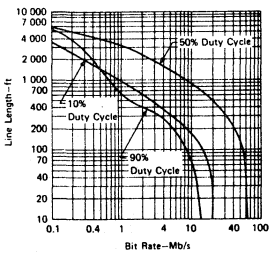


FIGURE 31

DRIVER SN75123
RECEIVER SN75124

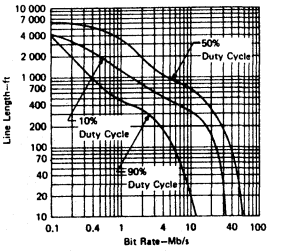


FIGURE 32

DRIVER SN75123
RECEIVER SN75125, SN75127

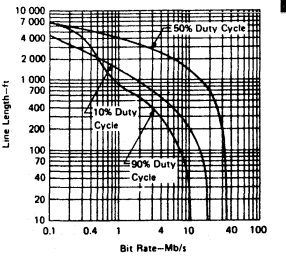
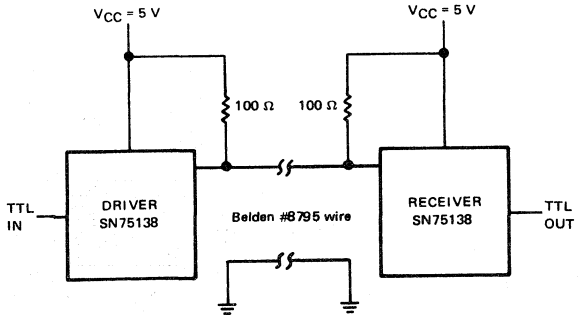


FIGURE 33



MEASUREMENT INFORMATION FOR FIGURE 34

DRIVER SN75138
RECEIVER SN75138

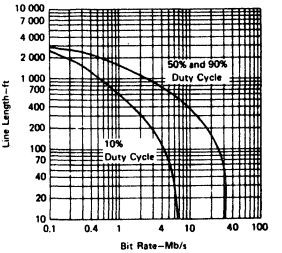
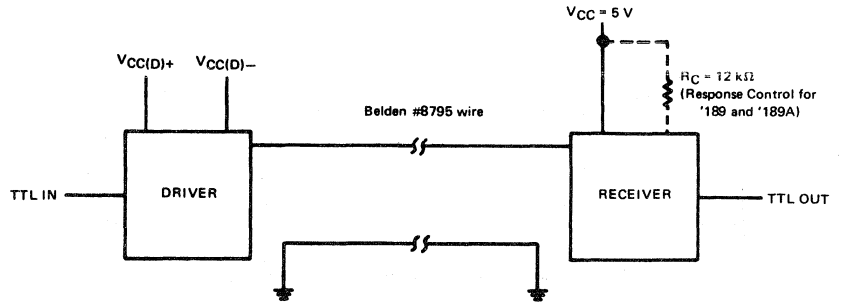


FIGURE 34

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 35 thru 37

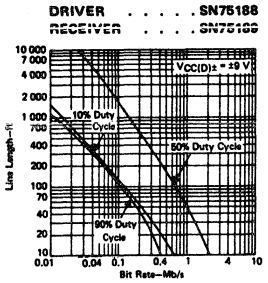


FIGURE 35

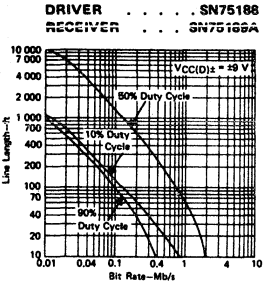


FIGURE 36

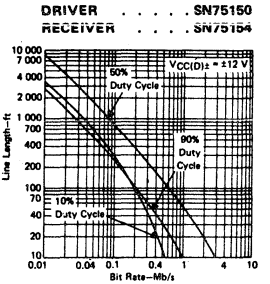
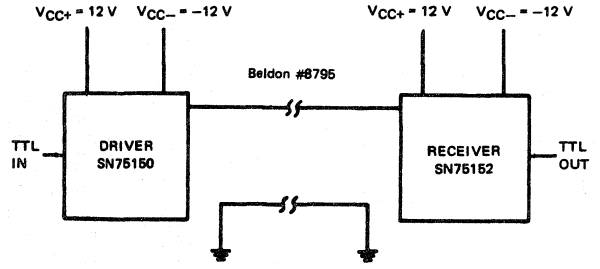


FIGURE 37



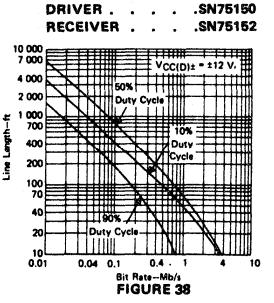
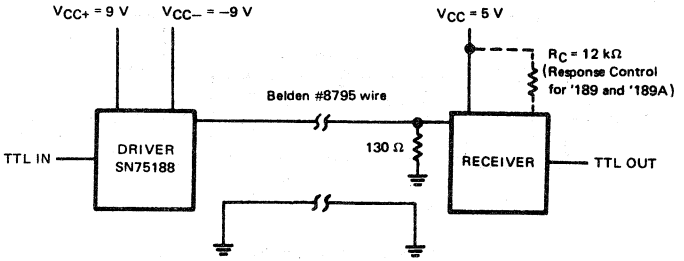


FIGURE 38

MEASUREMENT INFORMATION FOR FIGURE 38

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 39 AND 40

5

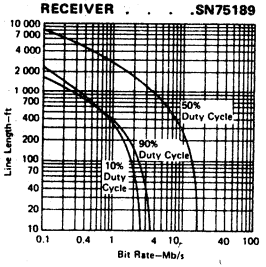


FIGURE 39

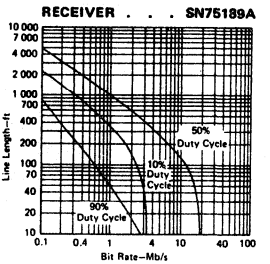
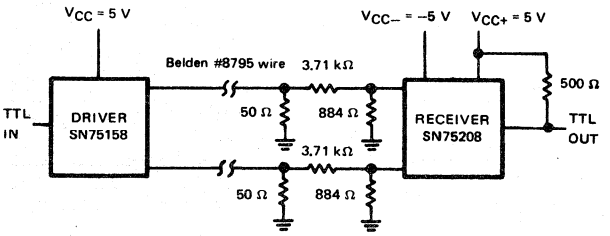


FIGURE 40



MEASUREMENT INFORMATION FOR FIGURE 41

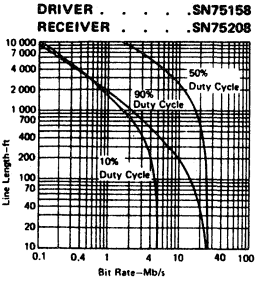
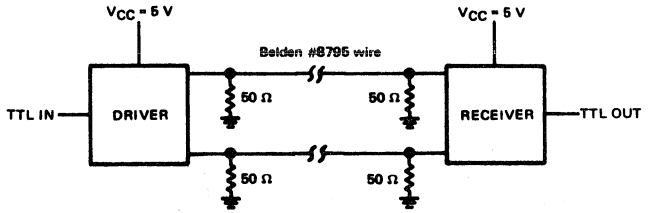


FIGURE 41

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 42 AND 43

5

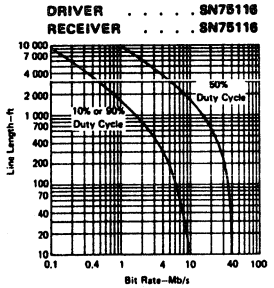


FIGURE 42

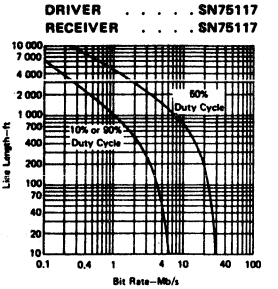
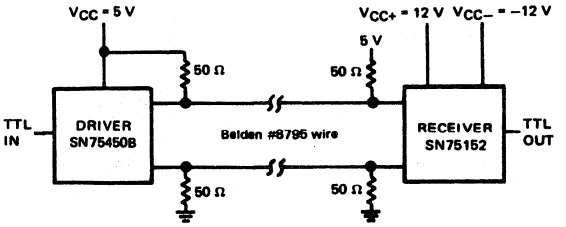


FIGURE 43



MEASUREMENT INFORMATION FOR FIGURE 44

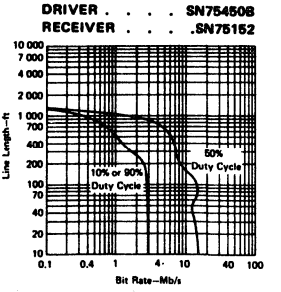


FIGURE 44

6

Sense Amplifiers

SENSE AMPLIFIERS

DESCRIPTION	THRESHOLD SENSITIVITY	COMMON-MODE RANGE	TYPE† OF OUTPUT	t_{PD}¶ TYPICAL	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	UNITS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
					−55°C to 125°C	0°C to 70°C				
CORE-MEMORY SENSE AMPLIFIERS	±4 mV	±2.5 V	R	35 ns	SN5520	SN7520	J J,N	1	• Provides memory data register • Complementary outputs	6–3
			O-C or R	30 ns	SN5522	SN7522	J J,N	1	• Dual input channels • Single-ended output	
			R	25 ns	SN5524	SN7524	J J,N	2	• Independent strobes	
			R	25 ns	SN5528	SN7528	J J,N	2	• Independent strobes • Test points for strobe timing adjustment	
			O-C	25 ns	SN55232	SN75232	J J,N	2	• Independent strobes • Internally compensated reference amplifier	
			R	25 ns	SN55234	SN75234	J J,N	2	• Independent strobes • Internally compensated reference amplifier	
			R	25 ns	SN55238	SN75238	J J,N	2	• Independent strobes • Internally compensated reference amplifier • Test points for strobe timing adjustment	
	±3 mV	±1.5 V	T-P	28 ns	SN55236	SN75236	W W	2	• Built in data buffer and data register • Reference amplifier inherently stable	See Note 1
MOS-TO-TTL CONVERTER ARRAY	500 μA		T-P	30 ns		SN75270	J,N	7	• 7 single-ended noninverting drivers per package • Single 5-V supply	6–59
MOS-MEMORY SENSE AMPLIFIERS	±25 mV	±3 V	T-P	17 ns	SN55107A	SN75107A	J J,N	2	• Independent strobes	5–49
	±25 mV	±3 V	O-C	19 ns	SN55108A	SN75108A	J J,N	2	• Independent strobes	
	±10 mV	±3 V	T-P	17 ns		SN75207	J,N	2	• Independent strobes	6–53
			O-C	19 ns		SN75208	J,N	2		
TMS 4062 I/O INTERFACE	±50 μA		R	25 ns		SN75370	J,N	2	• Combined driver and sense amplifier • Read enable and write enable controls	7–81

†T-P ≡ Totem Pole, O-C ≡ Open Collector, R ≡ Resistor Pull-Up

¶t_{PD} = Propagation Delay Time

NOTE 1: For additional information, contact your nearest TI field sales office.

SERIES 5520/7520 SENSE AMPLIFIERS

BULLETIN NO. DL-S 7711279, AUGUST 1973—REVISED APRIL 1977

HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

performance features

- High Speed and Fast Recovery Time
- Time and Amplitude Signal Discrimination
- Adjustable Input Threshold Voltage Levels
- Narrow Region of Threshold Voltage Uncertainty
- Multiple Differential-Input Preamplifiers
- High D-C Noise Margin . . . Typically One Volt
- Good Fan-Out Capability

ease-of-design features

- Choice of Output Circuit Function
- TTL or DTL Drive Capability
- Standard Logic Supply Voltages
- Plug-in Configuration Ideal for Flow-Soldering Techniques
- Pins on 100-mil Grid Spacings for Industrial-Type Circuit Boards

description

Series 5520/7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The SN5520 and SN7520 circuits may be used to perform the functions of a flip-flop or register that responds to the sense and strobe input conditions.

The SN5522 and SN7522 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an SN5520 or SN7520 circuit, or to perform the wired-AND function.

The SN5524 and SN7524 circuits provide for independent, dual-channel sensing with separate outputs. SN55234 and SN75234 are similar but have inverted outputs and internal compensation. SN55232 and SN75232 are identical to the SN55234 and SN75234, respectively, except that their output gates each feature an open-collector output.

The SN5528 and SN7528 circuits are identical to the SN5524 and SN7524, respectively, except that the output of each preamplifier is available as a test point. SN55238 and SN75238 are similar to SN5528 and SN7528, respectively, but have inverted outputs and internal compensation.

Series 5520 sense amplifiers are available in the J ceramic dual-in-line package and are characterized for operation over the full military temperature range of −55°C to 125°C. Series 7520 sense amplifiers are available in both the J (ceramic) and N (plastic) dual-in-line packages and are characterized for operation from 0°C to 70°C.

CONTENTS

SERIES 5520/7520
SENSE AMPLIFIERS

design characteristics

Series 5520/7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly sensitive to changes in the d-c levels throughout the amplifier. This was due primarily to the required tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of Series 5520/7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense-amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

circuit operation

The basic Series 5520/7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept that takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage that is distributed to the input amplifiers. Application of an external reference voltage, V_{ref}, establishes the input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T. The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier through changes in temperature or power-supply voltage levels are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.

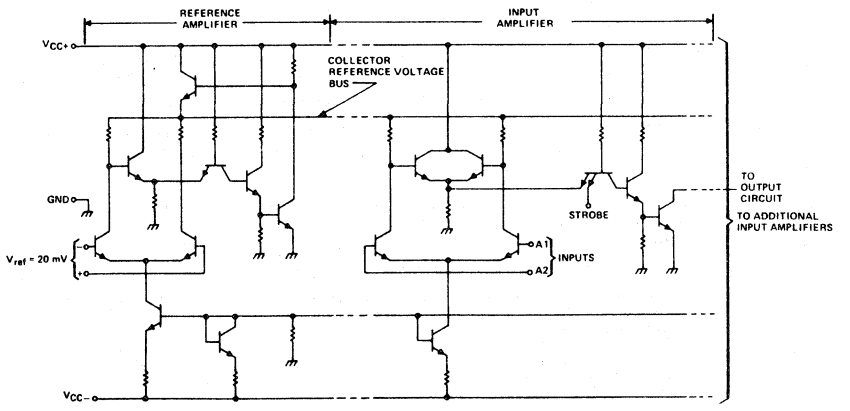


FIGURE A–BASIC SERIES 5520/7520 SENSE-AMPLIFIER CIRCUIT

circuit operation (continued)

The second stage of the input amplifier is a TTL gate. This gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

The logic inputs (i.e., gate and strobe) of Series 5520/7520 sense amplifiers are designed to be compatible with Series 54/74 TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same noise margin and logic threshold voltage as guaranteed for Series 54/74 are assured for each of the gate and strobe inputs. This is accomplished by testing each logic input under standard Series 54/74 test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

SN5520/SN7520 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output circuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Z input. Capacitive coupling from output Z to G_Y results in output pulse stretching. With either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of SN5520/SN7520 can be expanded by connecting the Y output of SN5522/SN7522 to the G_Y input of the circuit being expanded.

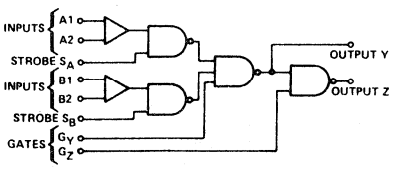


FIGURE B
SN5520/SN7520 LOGIC DIAGRAM

logic: $Y = \overline{G_Y} + A \cdot S_A + B \cdot S_B$

$Z = \overline{G_Z} + \overline{Y}$

$Z = \overline{G_Z} + G_Y (\overline{A} + \overline{S_A})(\overline{B} + \overline{S_B})$

SN5522/SN7522 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output that permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the SN5520/SN7520 circuit.

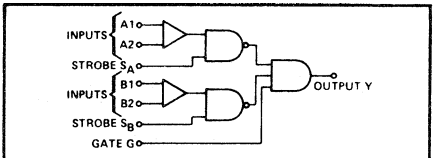


FIGURE C
SN5522/SN7522 LOGIC DIAGRAM

logic: $Y = G (\overline{A} + \overline{S_A})(\overline{B} + \overline{S_B})$

SN5524/SN7524 circuit

This circuit features two completely independent sense amplifiers in a single package. Each amplifier features high fan-out capability.

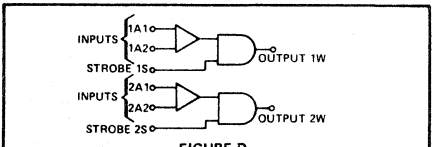


FIGURE D
SN5524/SN7524 LOGIC DIAGRAM
SN55232/SN75232 SAME EXCEPT INVERTED OPEN-COLLECTOR OUTPUT
SN55234/SN75234 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN5524 and SN7524

$W = \overline{AS}$ for SN55232, SN75232, SN55234, and SN75234

6

SN5528/SN7528 circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

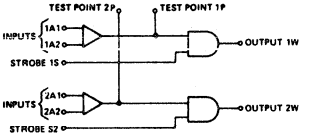


FIGURE E
SN5528/SN7528 LOGIC DIAGRAM
SN55238/SN75238 SAME EXCEPT INVERTED OUTPUT

logic: W = $\overline{AS}$ for SN5528 and SN7528
W = $\overline{AS}$ for SN55238 and SN75238

SN55232, SN75232, SN55234, SN75234, SN55238, and SN75238 circuits

The SN55234, SN75234, SN55238, and SN75238 dual sense amplifier circuits are the same as SN5524, SN7524, SN5528, and SN7528, respectively, except that an additional stage has been added to the output gate to provide an inverted output and internal compensation has been added. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added. The need for an external roll-off capacitor has been eliminated. SN55232 and SN75232 are identical to the SN55234 and SN75234, respectively, except that their output gates each have an open-collector output. This permits two or more outputs to be connected in wire-AND configuration.

reference voltage considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40 mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure F. This type of voltage divider may be used to supply an individual reference amplifier or to supply a number of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (nominally 30 μA); therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

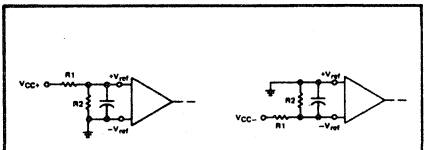


FIGURE F

input line layout considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors and use of a good ground plane to separate strobe and output lines from sense and reference input lines are recommended.

sense-input termination resistor considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values that will be compatible with the particular application. Matched termination resistors, (R_T, Figure G), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

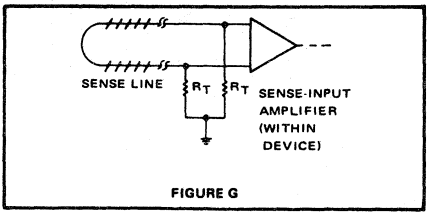


FIGURE G

output drive capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current. This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the SN5522/SN7522 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

logic input current requirements

Logic input current requirements are specified at worst-case power-supply conditions over the recommended operating free-air temperature range. The logic input currents are identical to those of, and compatible with, Series 54/74 TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1)
- V_{CC+} . . . . . 7 V
- V_{CC-} . . . . . −7 V

Differential input voltage, V_{ID} or V_{ref} . . . . . ±5 V
Voltage from any input to ground (see Note 2) . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 5.5 V
Operating free-air temperature range: SN55' circuits . . . . . −55°C to 125°C
SN75' circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values, except differential voltages are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

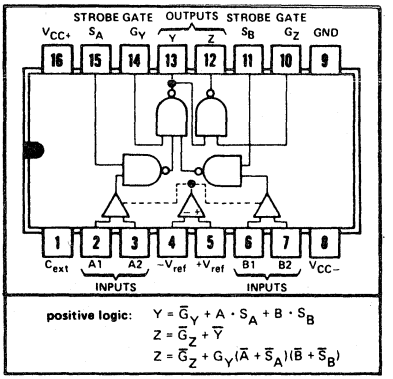
recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC+}	4.75	5	5.25	V
V_{CC-}	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

FUNCTION TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I > V_{IH}$ min	$V_I < V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature-range, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	1	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5520 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5520 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5520 only			100	μA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5520 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3				2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3						0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

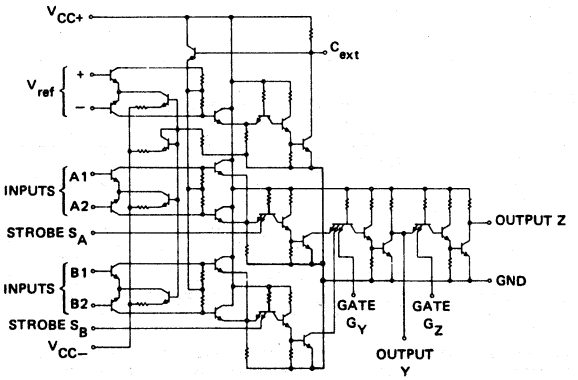
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	28	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	28	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	28	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	28	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	29	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	29	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	30	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

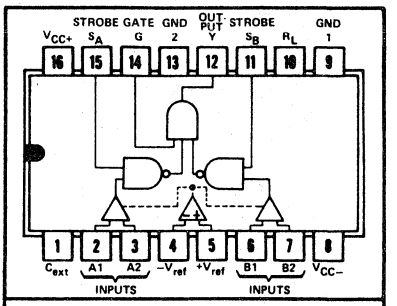
schematic



FUNCTION TABLE

INPUTS					OUTPUT
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I > V_{IH}$ min	$V_I < V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	7	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5522 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5522 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5522 only			100	µA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5522 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		µA
V_{IH}	High-level input voltage (strobe and gate inputs)	8				2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	8						0.8	V
V_{OH}	High-level output voltage	8	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 µA	2.4	4		V
V_{OL}	Low-level output voltage	8	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	µA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OH}	High-level output current	10	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	V_O = 5.25 V			250	µA
I_{OS}	Short-circuit output current	11	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		27	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2 OR B1-B2	Y	31	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(D)}$						30	45	
$t_{PLH(S)}$	STROBE A OR B	Y	31	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(S)}$						20	40	
$t_{PLH(G)}$	GATE	Y	32	C_L = 15 pF, R_L = 288 Ω		10		ns
$t_{PHL(G)}$						15	25	

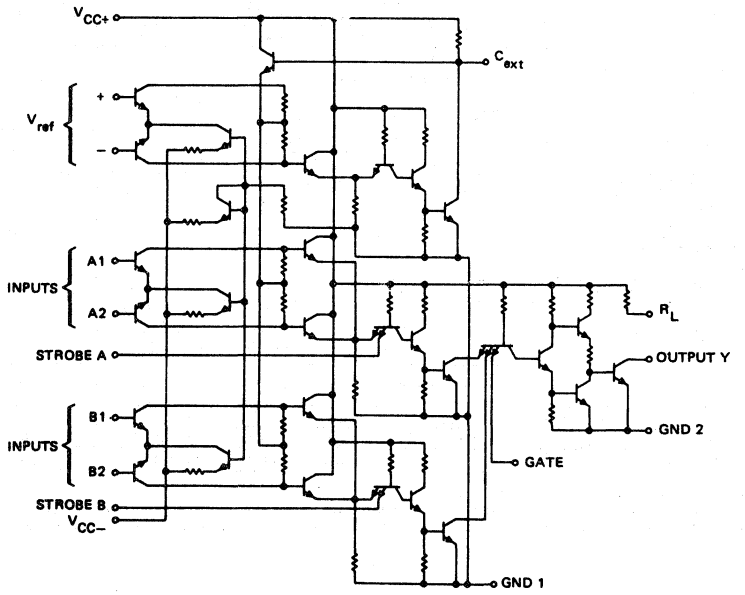
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6

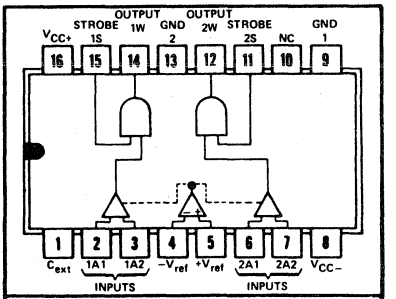
schematic



FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	12	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5524 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5524 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, *Common-mode input pulse:* $t_r \leq 15$ ns,	$V_{I(S)} = V_{IH}$ $t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN5524 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN5524 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	13				2			V
V_{IL}	Low-level input voltage (strobe inputs)	13						0.8	V
V_{OH}	High-level output voltage	13	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	13	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	14	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	14	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	15	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	33	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	33	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

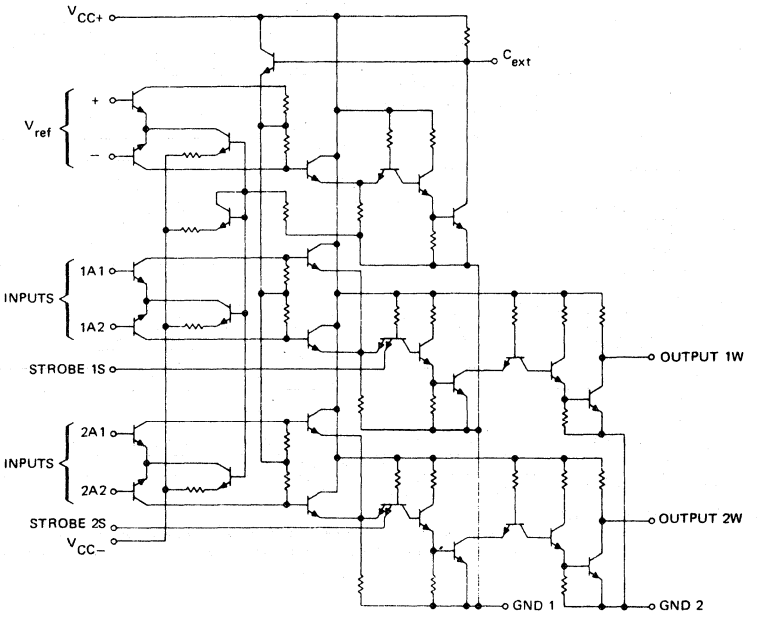
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6

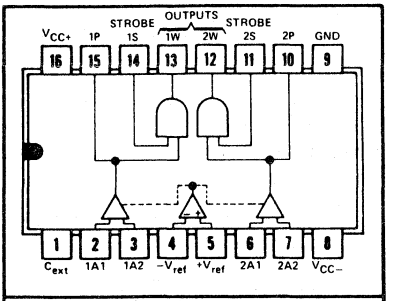
schematic



FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I > V_{IH}$ min	$V_I < V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	16	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5528 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5528 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5528 only			100	μA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5528 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	17				2			V
V_{IL}	Low-level input voltage (strobe inputs)	17						0.8	V
V_{OH}	High-level output voltage	17	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	17	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	18	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	18	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	19	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is th ...inimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

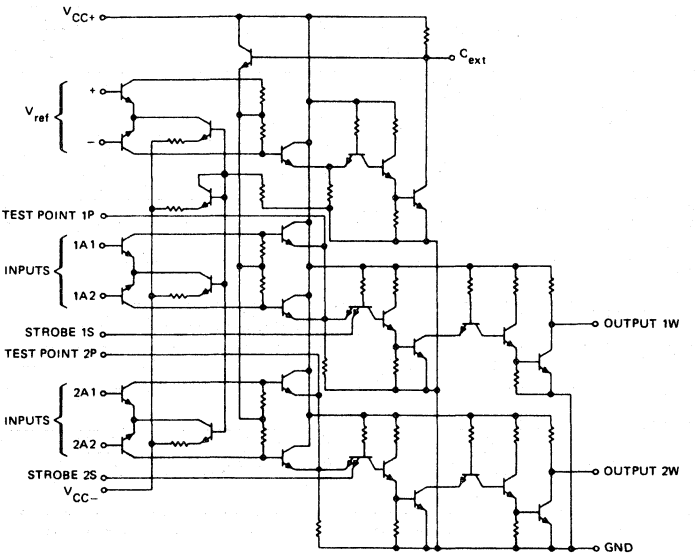
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	34	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		ns
$t_{PLH(S)}$	STROBE	W	34	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

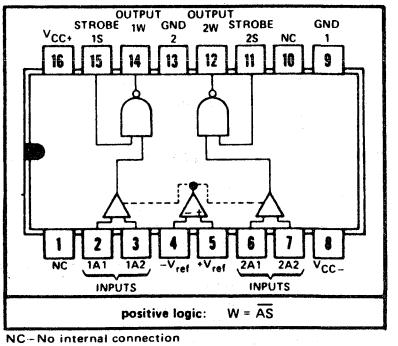
schematic



FUNCTION TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC – No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	20	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55232 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55232 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns				±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55232 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55232 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21				2			V
V_{IL}	Low-level input voltage (strobe inputs)	21						0.8	V
I_{OH}	High-level output current	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	V_{OH} = 5.25 V			250	μA
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

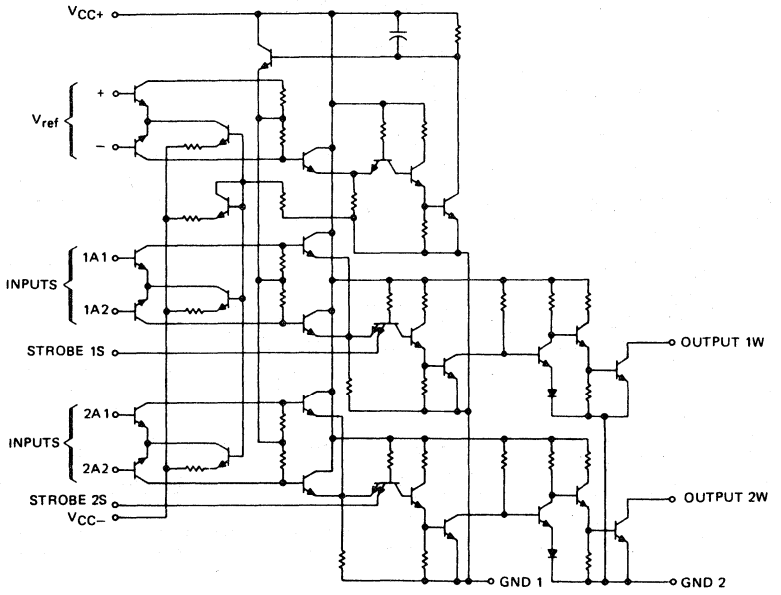
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode input overload signal prior to the strobe-enable signal.

6

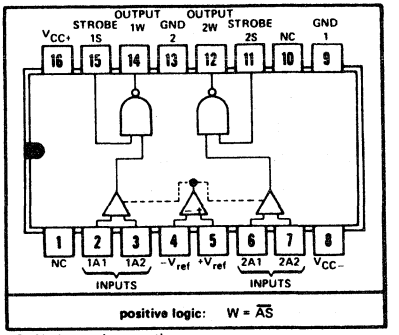
schematic



FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T}$ max	$V_{ID} \leq V_{T}$ min	Irrelevant
S	$V_{I} \geq V_{IH}$ min	$V_{I} \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	20	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55234 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55234 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} \triangleq V_{IH}$ *Common-mode input pulse:* $t_r \leq$ 15 ns,	$t_f \leq$ 15 ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55234 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55234 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21				2			V
V_{IL}	Low-level input voltage (strobe inputs)	21						0.8	V
V_{OH}	High-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	23	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

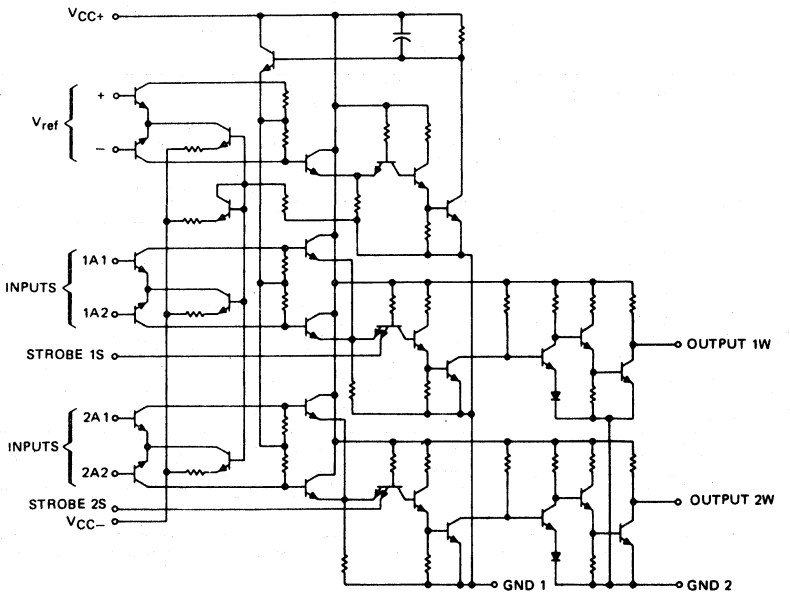
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

6

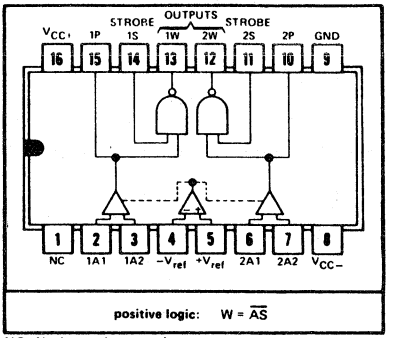
schematic



FUNCTION TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} > V_{T\ max}$	$V_{ID} < V_{T\ min}$	Irrelevant
S	$V_I > V_{IH\ min}$	$V_I < V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	24	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55238 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55238 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, *Common-mode input pulse:* $t_r \leq 15$ ns,	$V_{I(S)} = V_{IH}$ $t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55238 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55238 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	25				2			V
V_{IL}	Low-level input voltage (strobe inputs)	25						0.8	V
V_{OH}	High-level output voltage	25	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	25	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	26	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	26	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	27	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1–A2	W	36	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	ns
$t_{PLH(S)}$	STROBE	W	36	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	ns

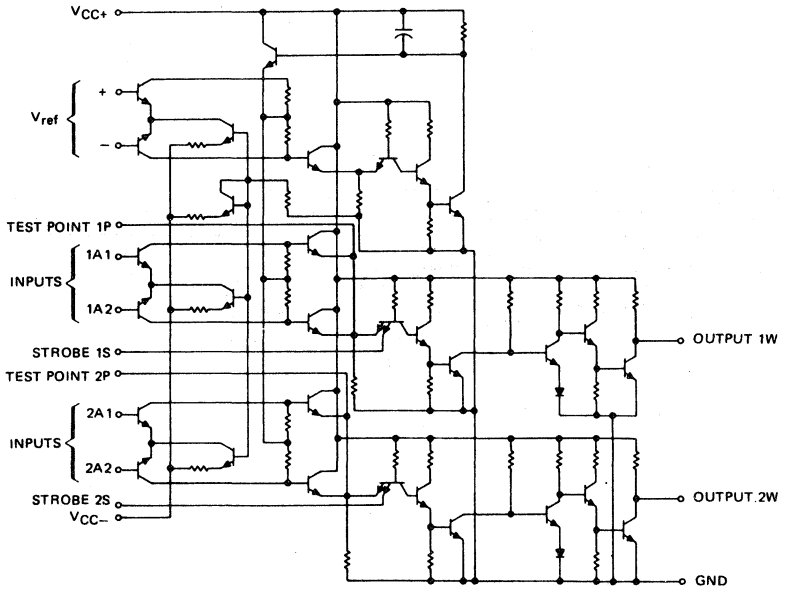
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

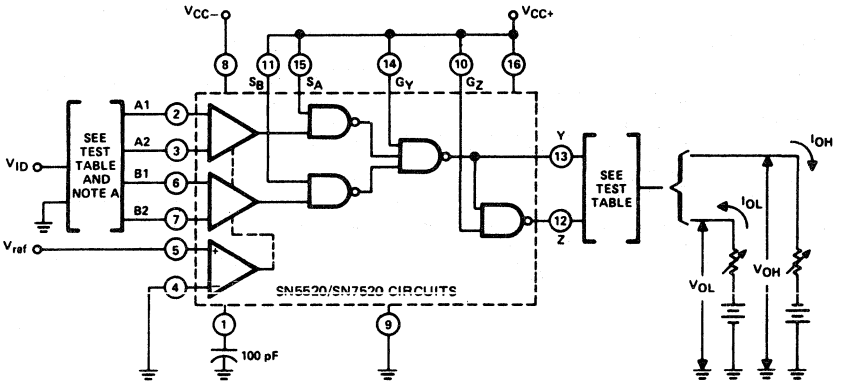
6

schematic



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN5520/ SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

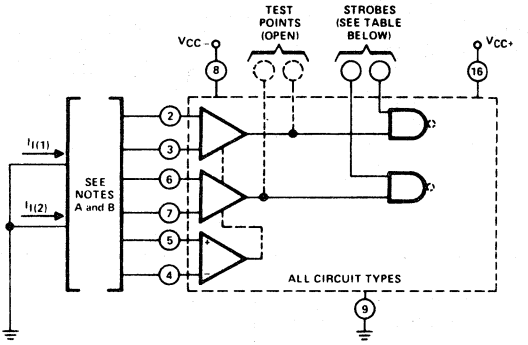
NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1–V_T

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN5520, SN7520	C_{ext} (1)	G_Y, G_Z (14) (10)	S_A, S_B (15) (11)	Y, Z (13) (12)	
SN5522, SN7522	C_{ext} (1)	G (14)	S_A, S_B, GND 2 (15) (11) (13)		R_L, Y (10) (12)
SN5524, SN7524	C_{ext} (1)		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN5528, SN7528	C_{ext} (1)		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	
SN55232, SN75232, SN55234, SN75234			1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN55238, SN75238			1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	

FIGURE 2–I_{IB}, I_{IO}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

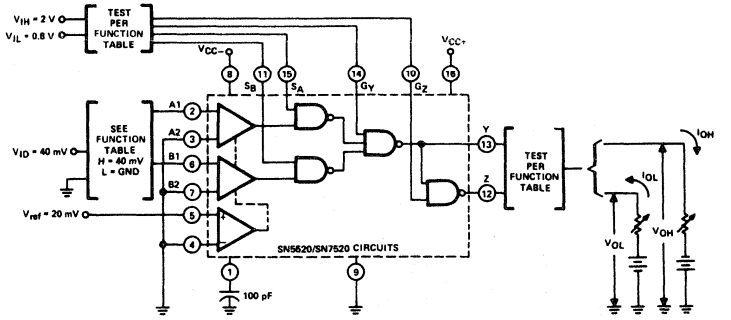
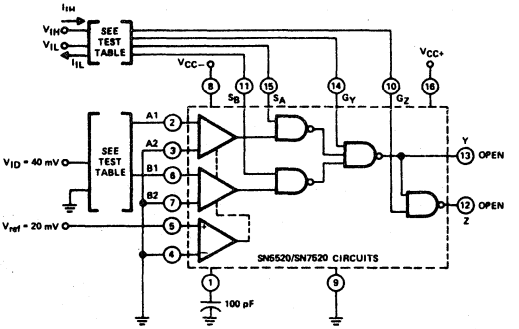


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}

6



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

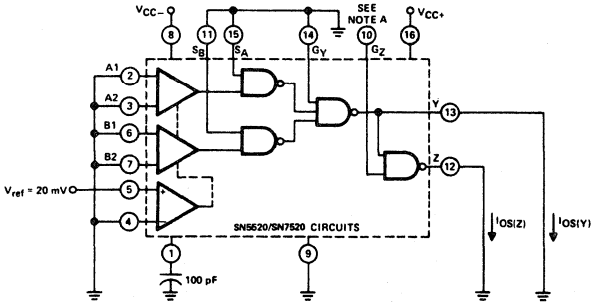
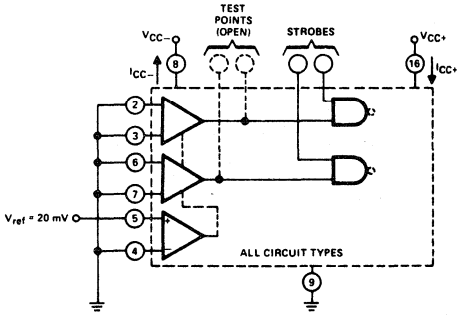


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

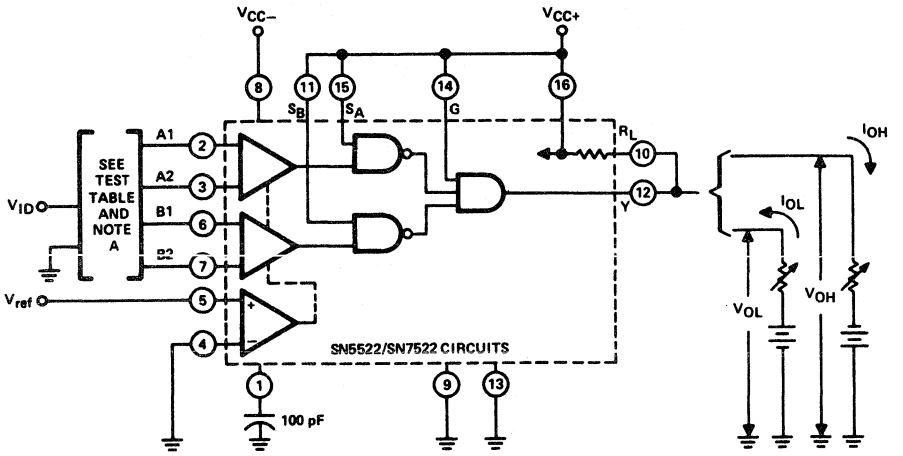
CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN5520, SN7520	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)	Y, Z (13) (12)
SN5522, SN7522	C_{ext} (1)	G, S_A, S_B, GND 2 (14) (15) (11) (13)	R_L, Y (10) (12)
SN5524, SN7524	C_{ext} (1)	1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN5528, SN7528	C_{ext} (1)	1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)
SN55232, SN75232, SN55234, SN75234		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN55238, SN75238		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)

FIGURE 6–I_{CC+}, I_{CC-}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



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TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5522/ SN7522	A1-A2 or B1-B2	15 mV	<11 mV	>2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	>19 mV	<0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	<36 mV	>2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	>44 mV	<0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

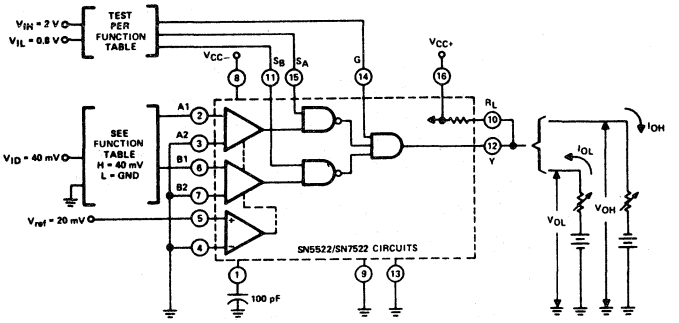
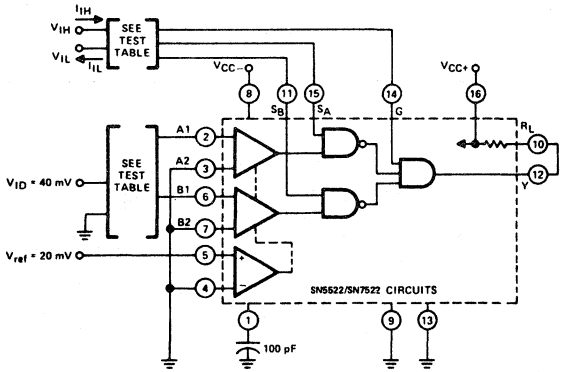


FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}

6



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

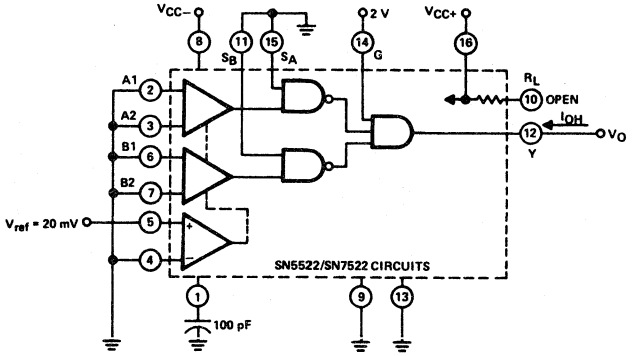


FIGURE 10–I_{OH}

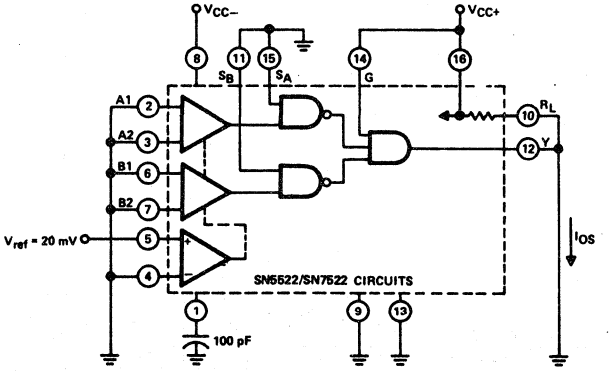
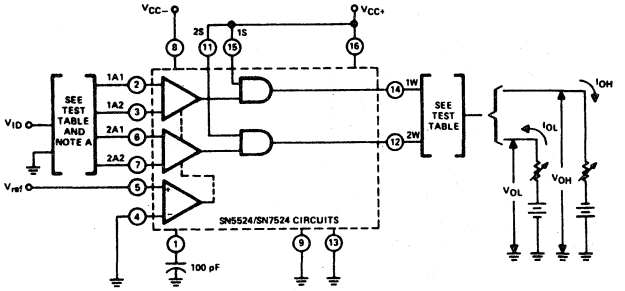


FIGURE 11–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5524/ SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

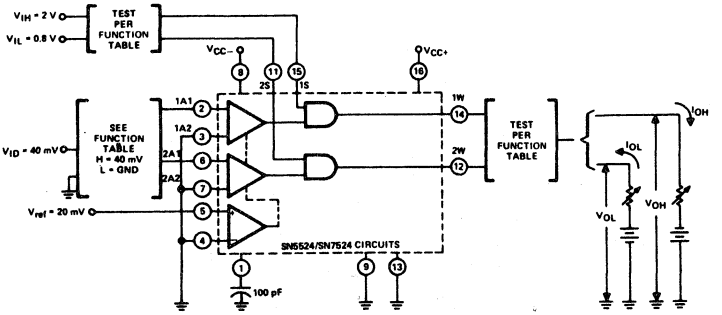
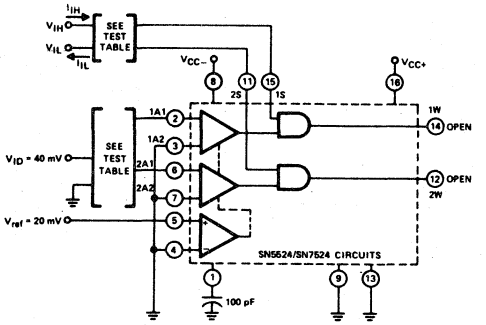


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

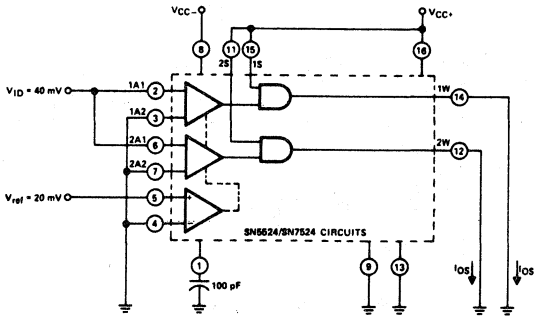
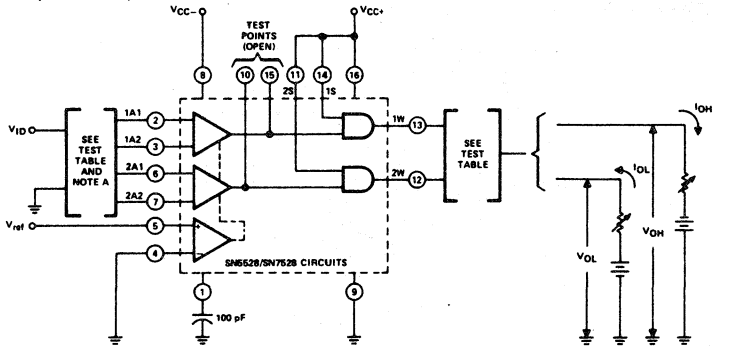


FIGURE 15–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5528/ SN7528	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 16 – V_T

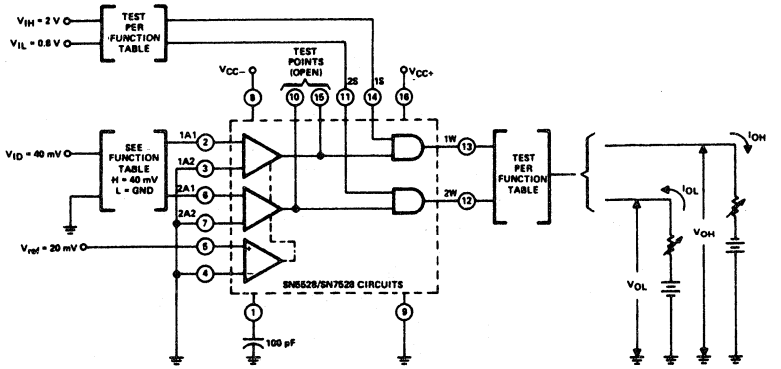
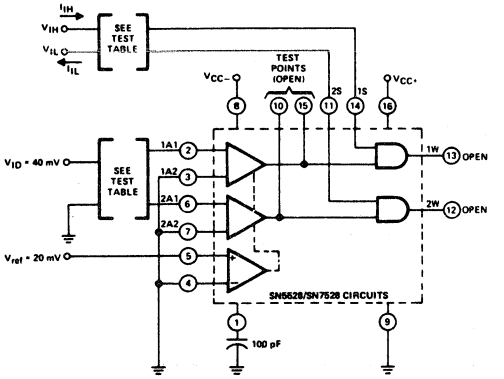


FIGURE 17 – V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 18 –I_{IH}, I_{IL}

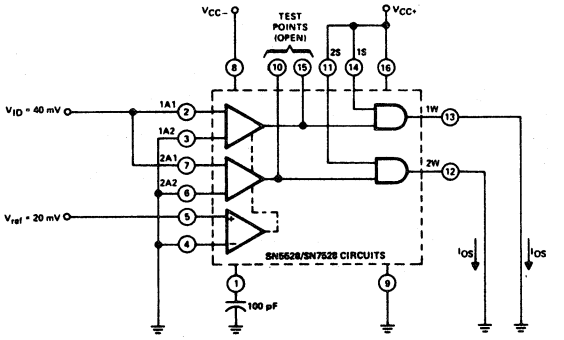
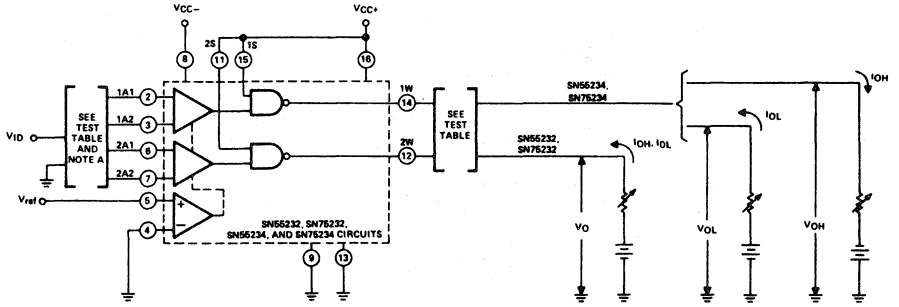


FIGURE 19–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS					
				SN55232, SN75232			SN55234, SN75234		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN55232, SN75232, SN55234, SN75234	A1-A2	15 mV	≤11 mV	5.25 V	≤250 μA		≥2.4 V	–400 μA	
	A1-A2	15 mV	≥19 mV	< 0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	5.25 V	≤250 μA		≥2.4 V	–400 μA	
	A1-A2	40 mV	≥44 mV	< 0.4 V		16 mA	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 20–V_T

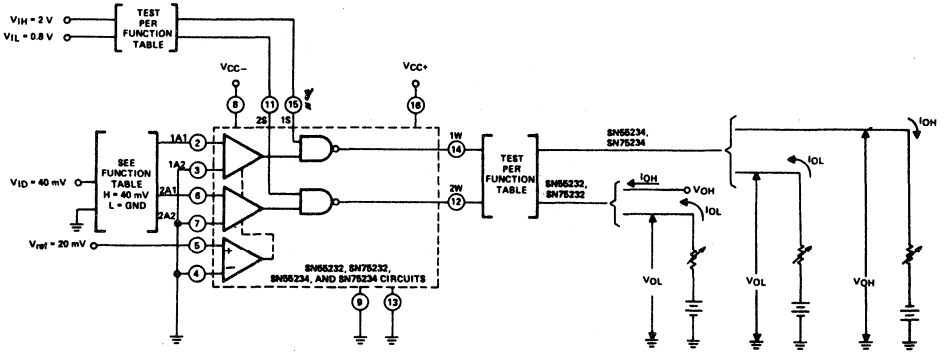
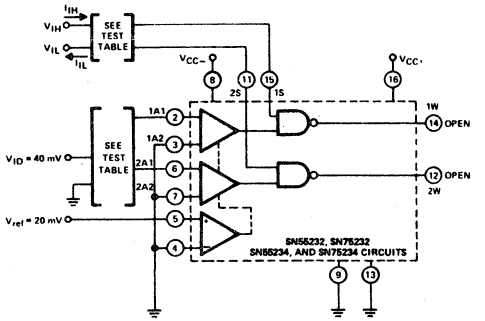


FIGURE 21–V_{IH}, V_{IL}, V_{OL}, V_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

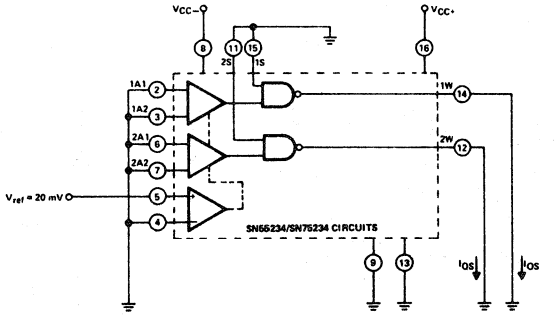
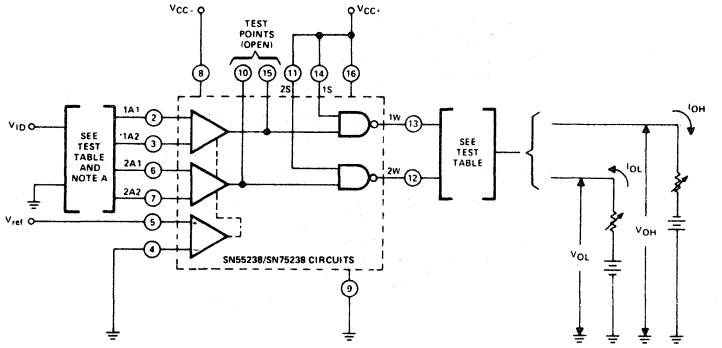


FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN55238/ SN75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 24–V_T

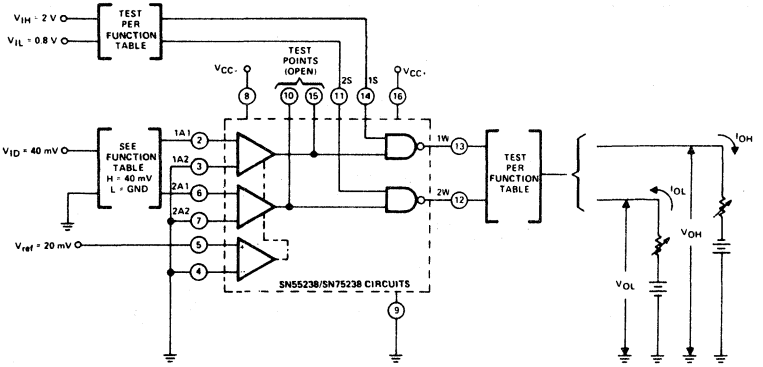
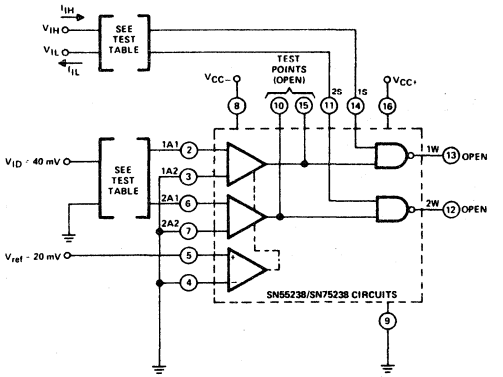


FIGURE 25–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

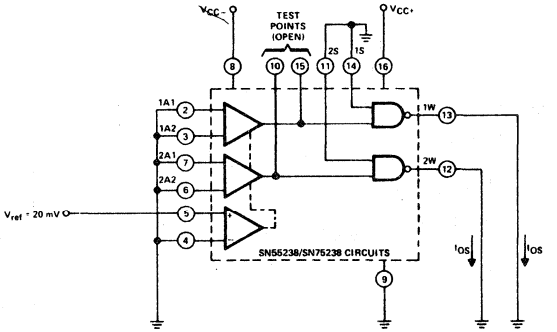
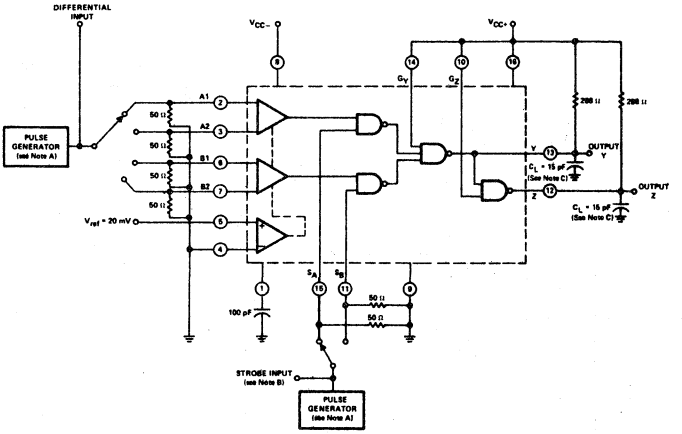


FIGURE 27–I_{OS}

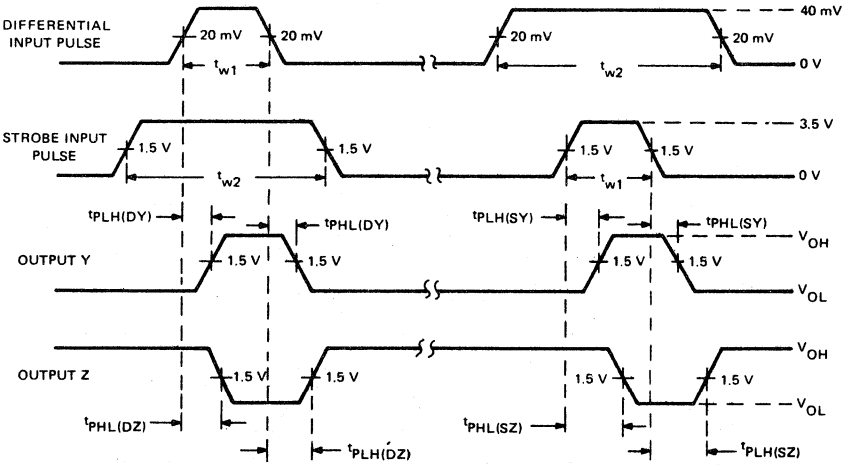
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

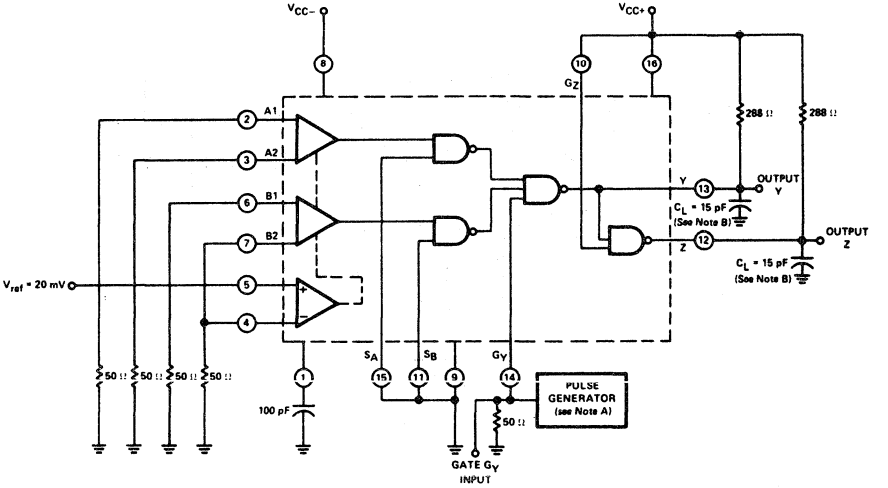
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

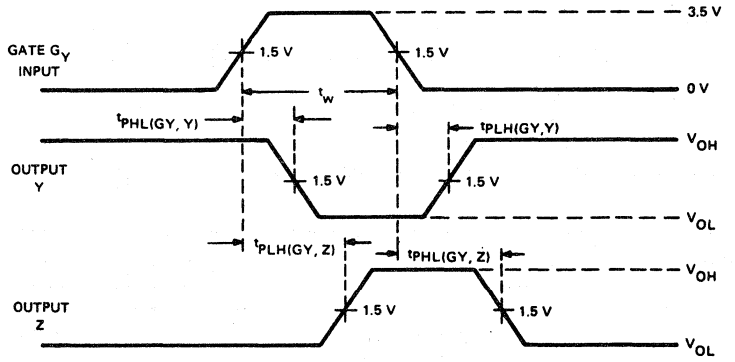
FIGURE 28–SN5520/SN7520 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



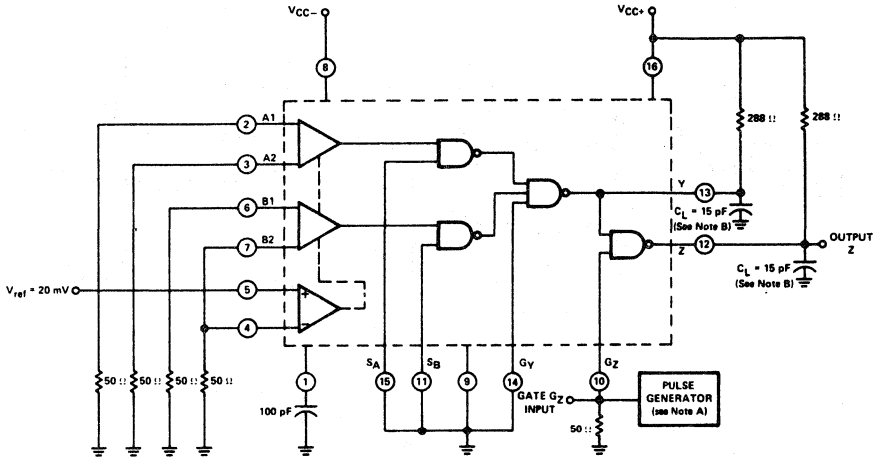
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

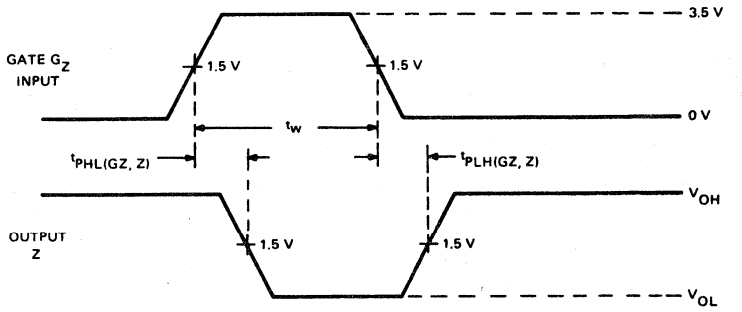
FIGURE 29–SN5520/SN7520 PROPAGATION DELAY TIMES FROM GATE G_Y

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



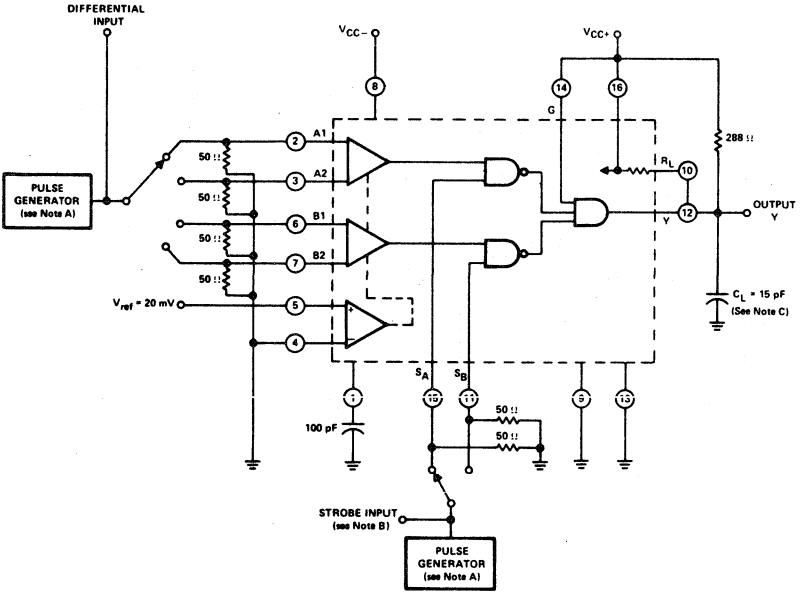
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

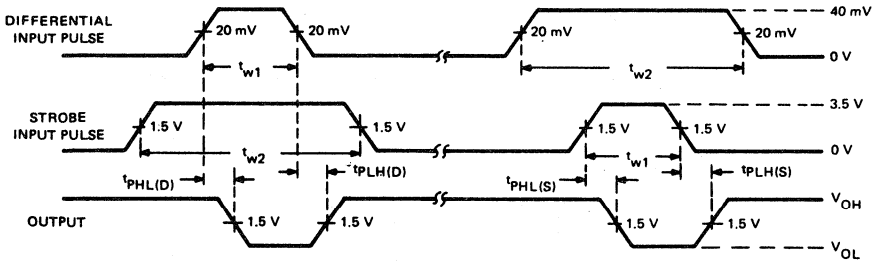
FIGURE 30–SN5520/SN7520 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

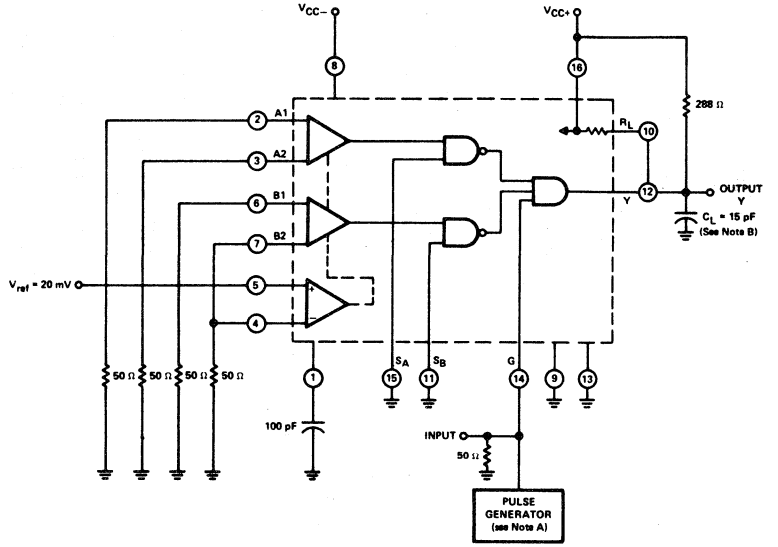


NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.
C. C_L includes probe and jig capacitance.

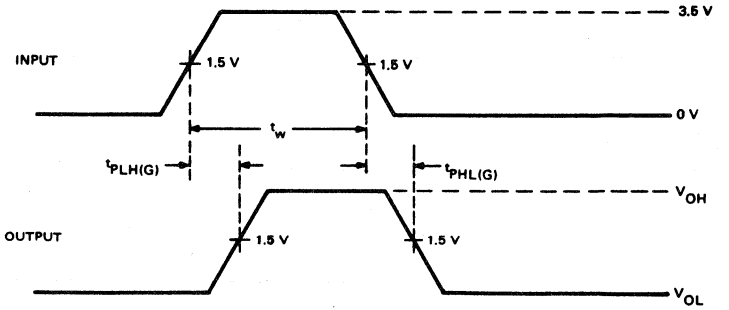
FIGURE 31–SN5522/SN7522 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



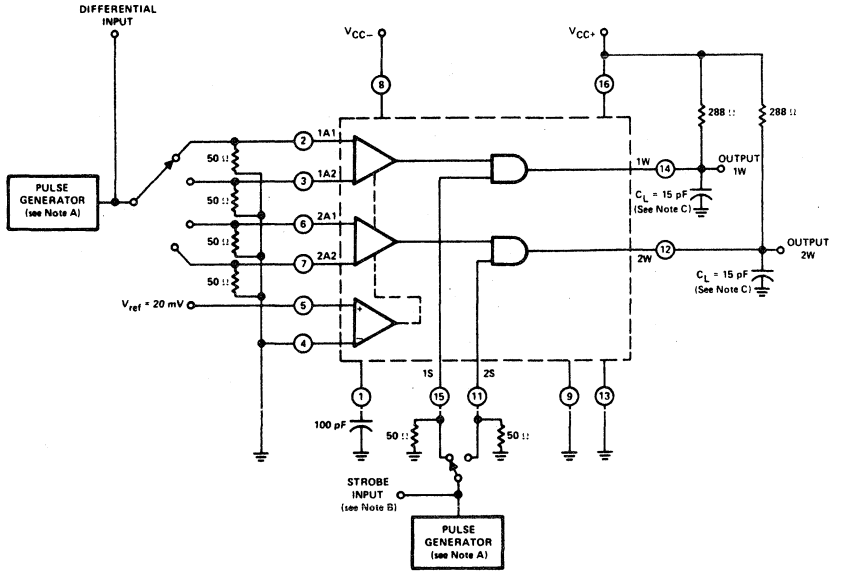
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

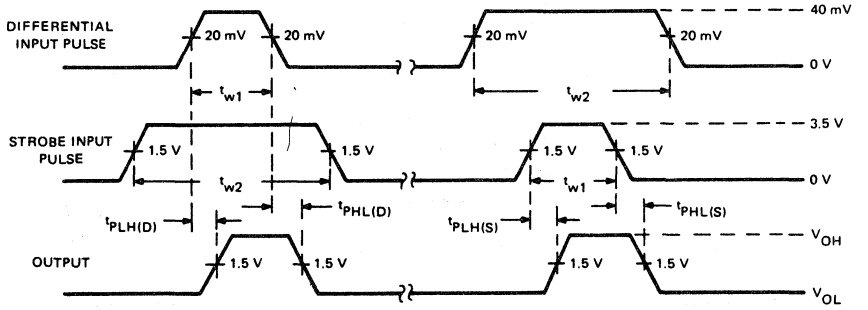
FIGURE 32–SN5522/SN7522 PROPAGATION DELAY TIMES FROM GATE INPUT

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



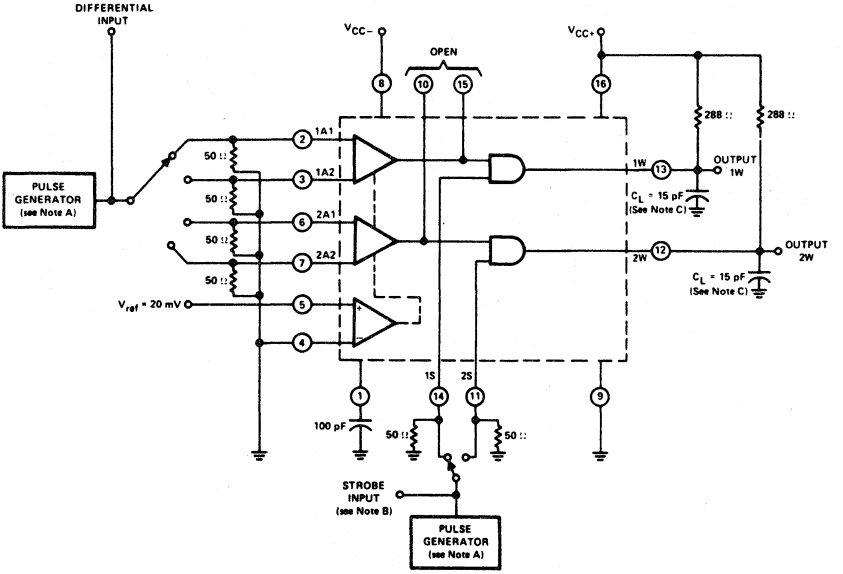
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

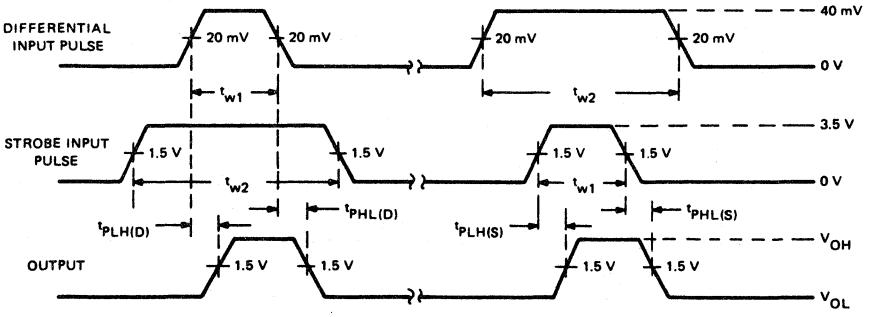
FIGURE 33–SN5524/SN7524 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

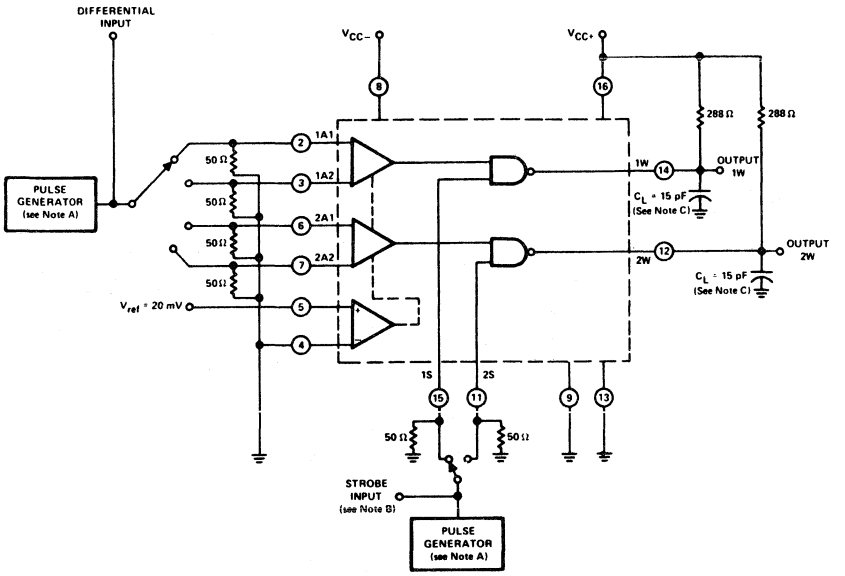
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

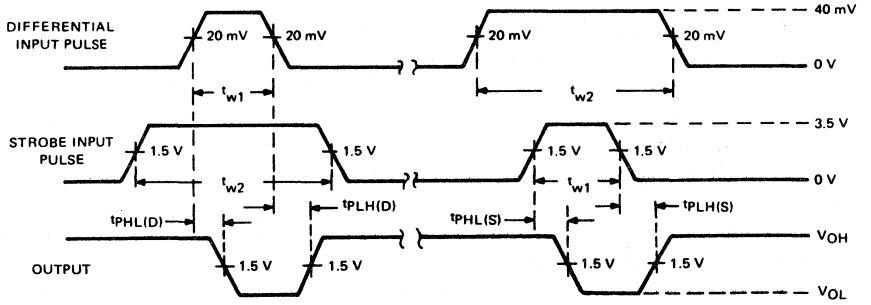
FIGURE 34–SN5528/SN7528 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



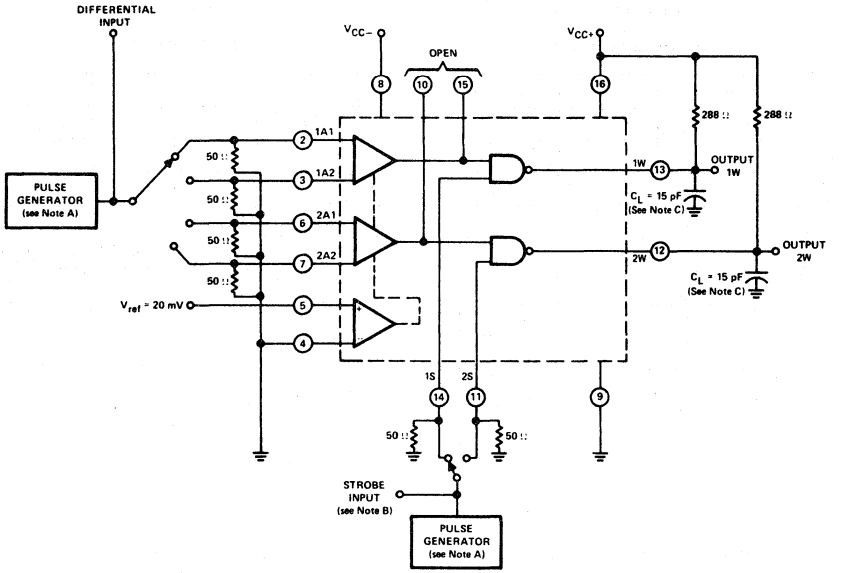
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

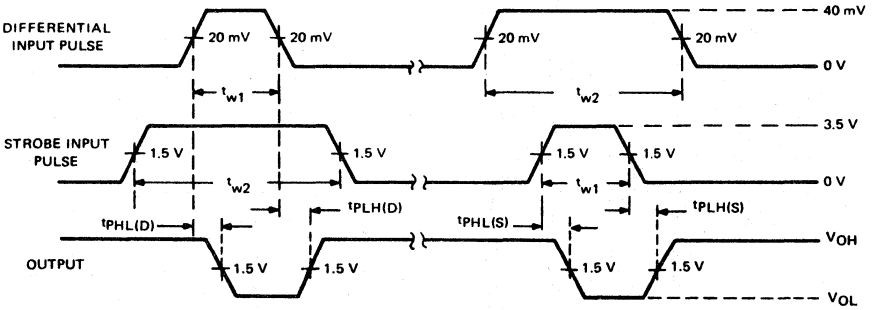
FIGURE 35–SN55232, SN75232, SN55234, and SN75234 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 36–SN55238/SN75238 PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

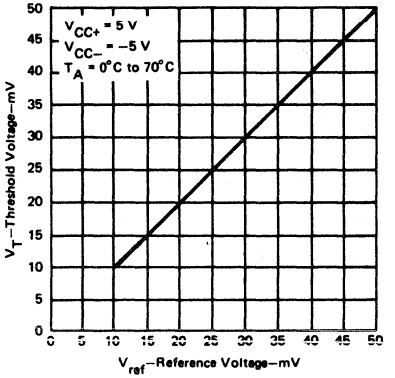


FIGURE 37

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

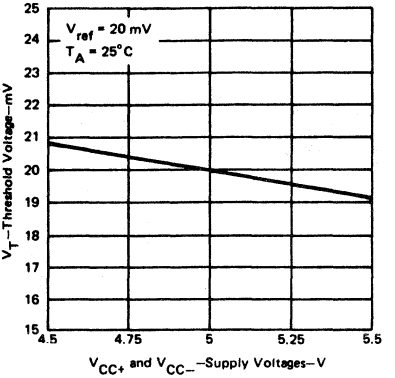


FIGURE 38

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

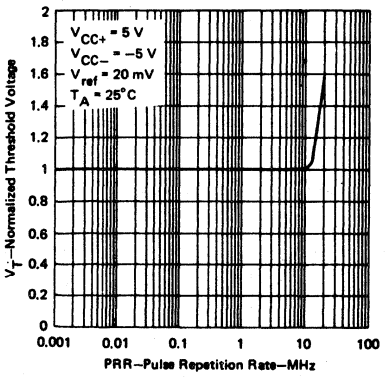


FIGURE 39

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

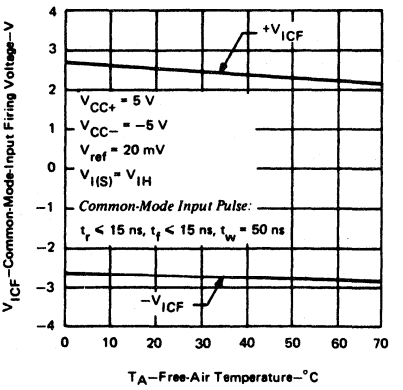


FIGURE 40

TYPICAL CHARACTERISTICS

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

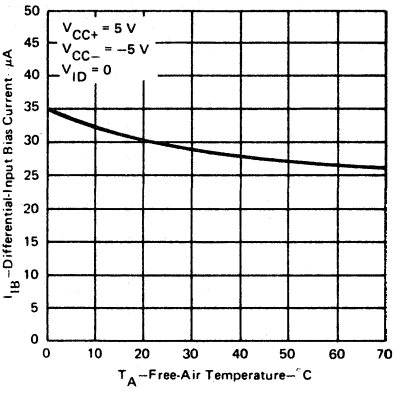


FIGURE 41

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

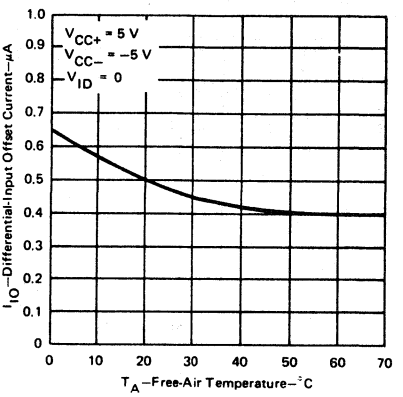


FIGURE 42

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

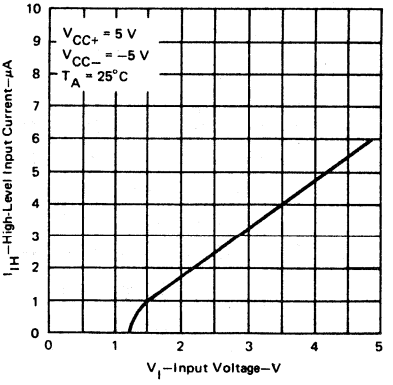


FIGURE 43

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

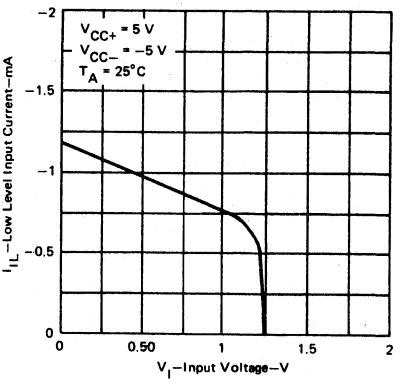


FIGURE 44

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

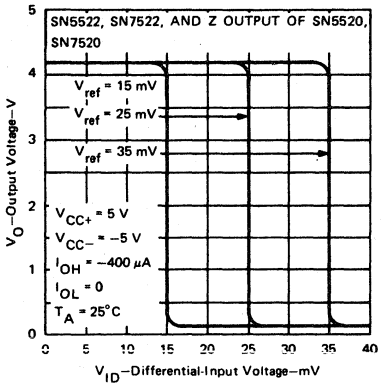


FIGURE 45

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

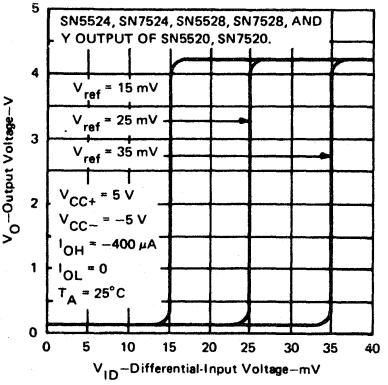


FIGURE 46

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

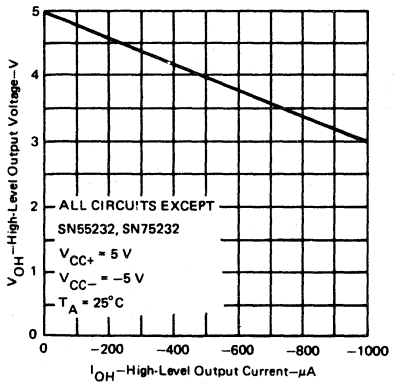


FIGURE 47

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

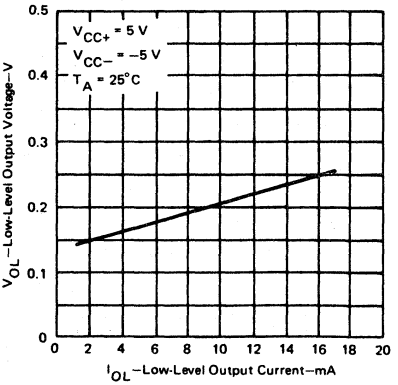


FIGURE 48

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure 49)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\,min}$$

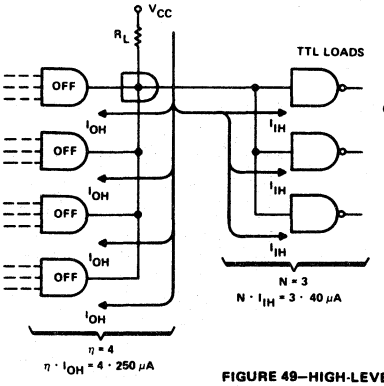
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\,min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\,min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\,\Omega = \frac{2.6}{0.00112}\,\Omega = 2321\,\Omega$$

FIGURE 49—HIGH-LEVEL CIRCUIT CONDITIONS

APPLICATION DATA

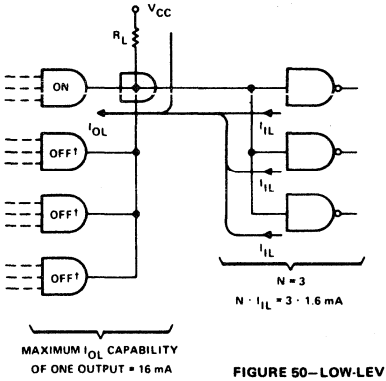
low-level (on-state) circuit calculations (see figure 50)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE 50—LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8995	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

‡—All values shown in the table are based on:
High-level conditions: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level conditions: V_{CC} = 5 V, $V_{OL\ max}$ = 0.4 V
X—Not recommended or not possible.
§—The theoretical value is ∞. See explanation in text.

TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN5524 or SN7524 sense amplifiers, see Figure 51. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

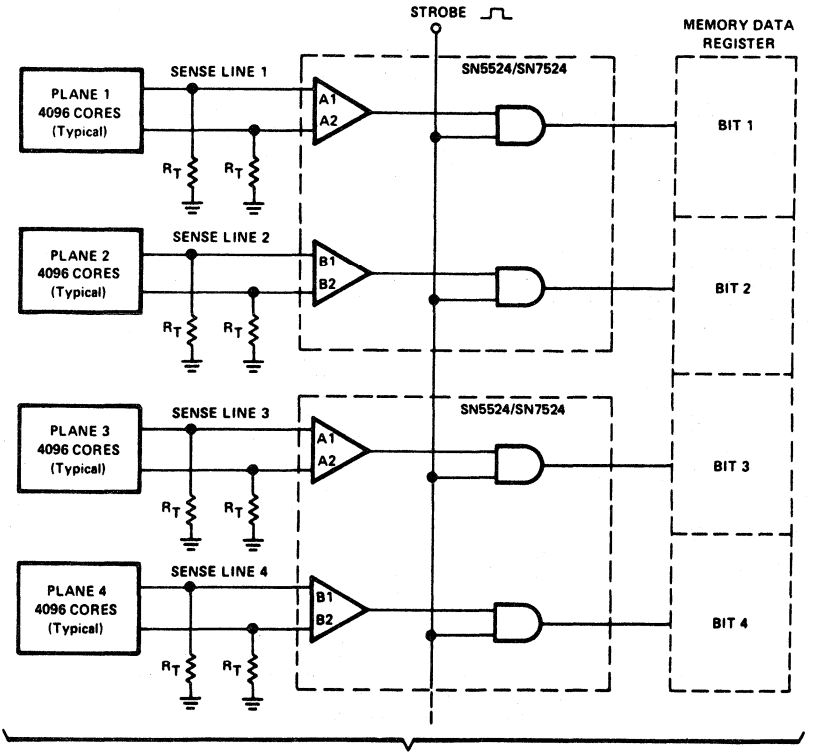


FIGURE 51–SENSING SMALL MEMORY SYSTEMS

TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal to noise ratio can be increased by sectioning the large core planes as illustrated in Figure 52. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN5520/SN7520 or SN5522/SN7522 sense amplifiers. The cascaded output gates of the SN5520/SN7520 circuits may be connected to serve as the memory data register (MDR). A number of SN5522/SN7522 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

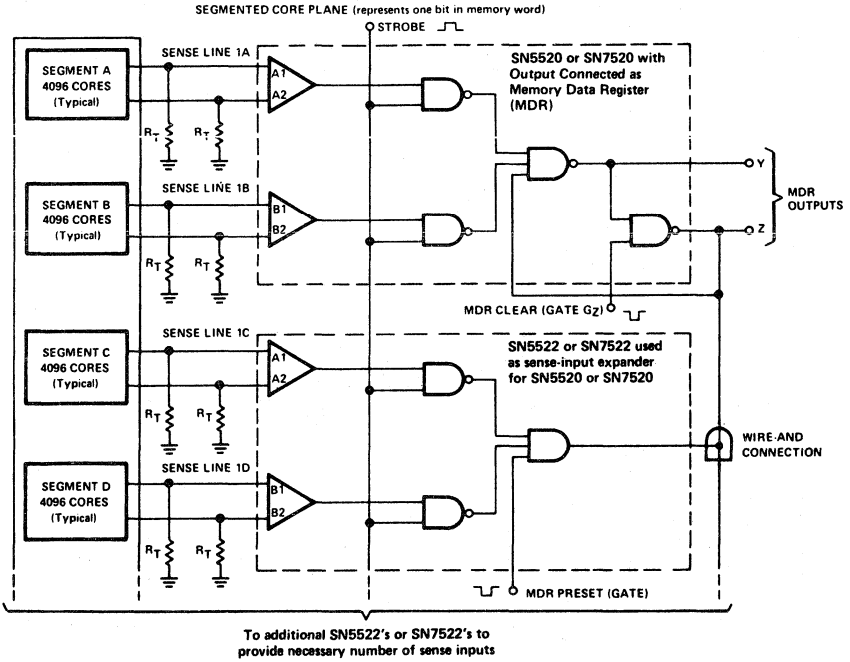


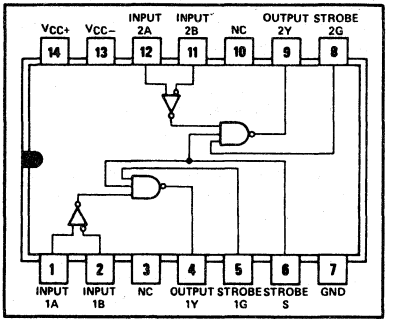
FIGURE 52–SENSING LARGE MEMORY SYSTEMS

TYPES SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

BULLETIN NO. DL-S 11793, JULY 1973—REVISED JANUARY 1977

- Plug-in Replacement for SN75107A, SN75107B, SN75108A, SN75108B with Improved Characteristics
- ±10 mV Guaranteed Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- '208 and '208B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

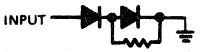
The SN75207, SN75207B, SN75208, and SN75208B are pin-for-pin replacements for the SN75107A, SN75107B, SN75108A, and SN75108B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output. The '208 and '208B each features an open-collector output that permits wired-AND logic connections with similar output configurations. These devices are designed for operation from 0°C to 70°C and are available in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

FUNCTION TABLE

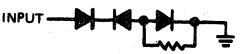
DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

The essential difference between the unsuffixed and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



UNSUFFIXED VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

design characteristics

The '207, '207B, '208, and '208B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

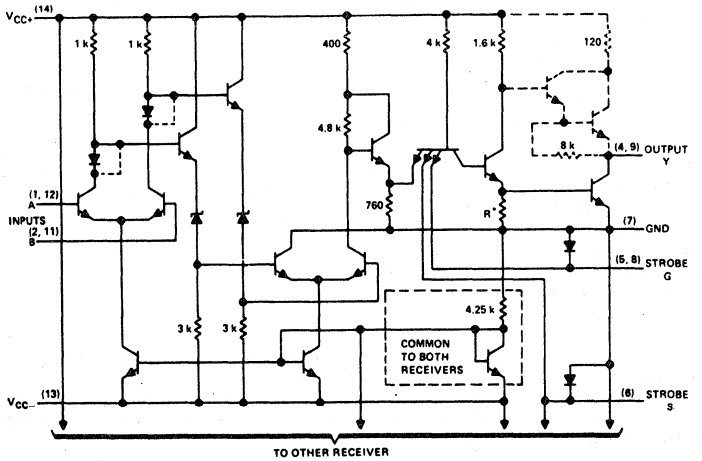
The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

6

schematic (each receiver)



*R = 1 kΩ for '207 and '207B, 750 Ω for '208 and '208B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '207 and '207B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '207 and '208.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions (see note 4)

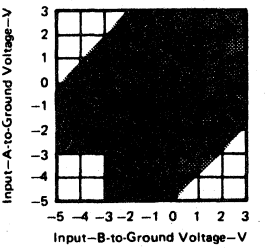
	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16	mA
Differential input voltage, V_{ID} (see Note 5)	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage range, any differential input to ground (see Note 5)	−5†		3	V
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

6

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
6. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS
OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.01	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.01	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

†The algebraic convention, where the more positive (less negative) limit is designated maximum, is used in this data sheet with logic input voltage levels only.

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

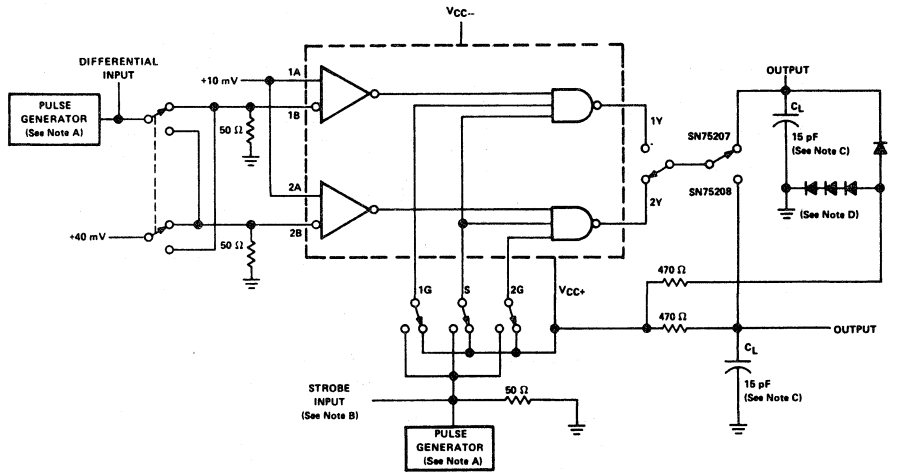
PARAMETER			TEST CONDITIONS‡		'207, '207B MIN	'207, '207B TYP§	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP§	'208, '208B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA,	V_{IDH} = 10 mV, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA,	V_{IDL} = −10 mV, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

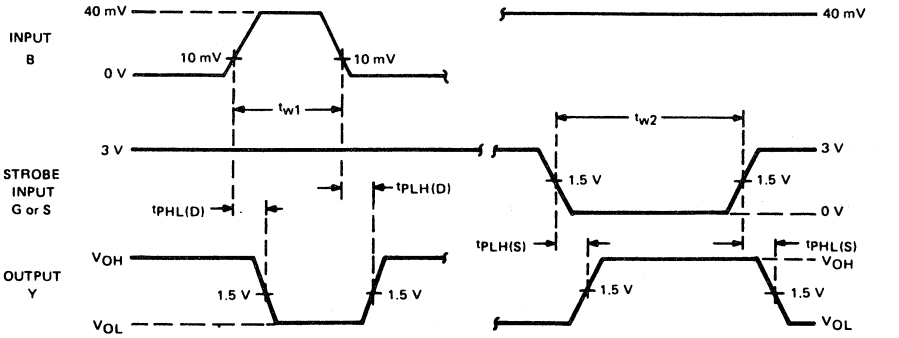
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'207, '207B MIN	'207, '207B TYP	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP	'208, '208B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 15 pF, See Figure 1			35			35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B				20			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S				17			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S				17			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

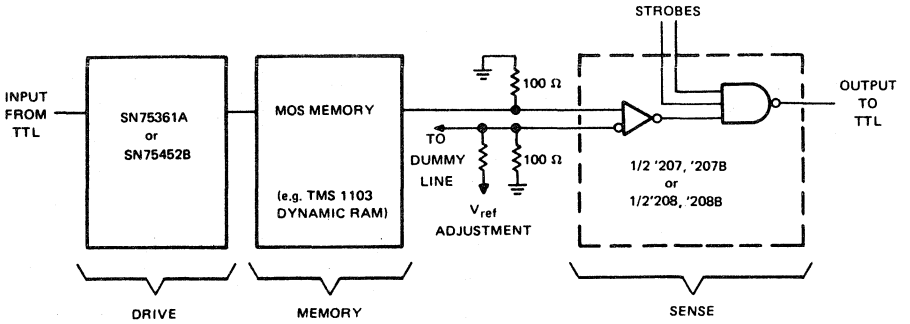
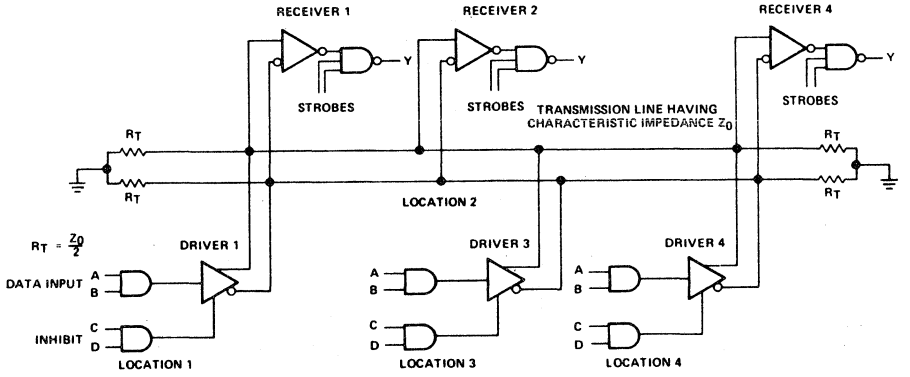


FIGURE 2–MOS MEMORY SENSE AMPLIFIER



Receivers are '207, '207B, '208, or '208B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3–DATA-BUS OR PARTY-LINE SYSTEM

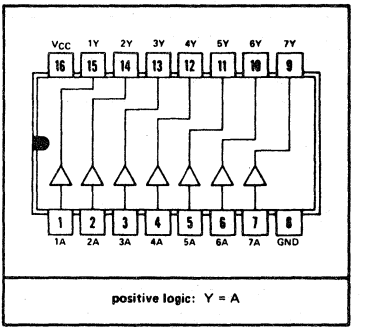
PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

TYPE SN75270
7-UNIT MOS-TO-TTL CONVERTER AND THERMAL PRINTHEAD DRIVER ARRAY

BULLETIN NO. DL-S 7712061, SEPTEMBER 1973—REVISED APRIL 1977

- 7 Single-Ended Noninverting Drivers Per Package
- Inputs Compatible with MOS
- TTL-Compatible Outputs
- Single 5-V Supply

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

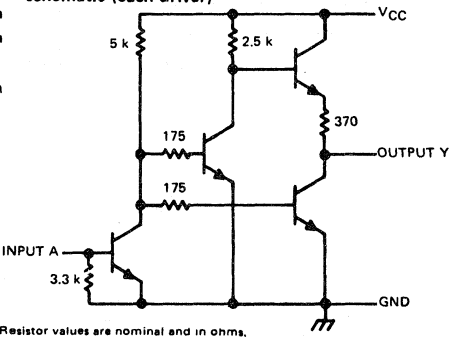


description

The SN75270 is a monolithic integrated circuit designed for use as a sense amplifier or thermal printhead driver. As a sense amplifier, the device can be used to convert from MOS to TTL levels. As a thermal printhead driver, this device is used with EPN3600-type thermal printheads.

The SN75270 is characterized for operation from 0°C to 70°C.

schematic (each driver)



Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input current	4 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input current, I_{IH}	0.5		2	mA
Low-level input current, I_{IL}	0		0.1	mA
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75270 chips are glass-mounted.

electrical characteristics over recommended operating free-air temperature range

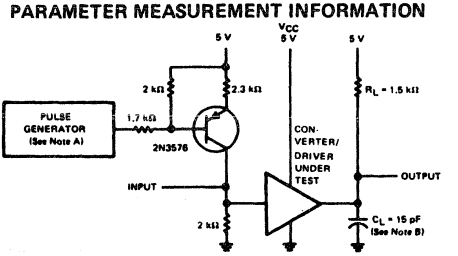
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	V_{CC} = 4.75 V, I_{IH} = 500 µA, I_{OH} = −80 µA	2.4			V
V_{OL} Low-level output voltage	V_{CC} = 4.75 V, I_{IL} = 100 µA, I_{OL} = 3.2 mA			0.4	V
I_{OH} High-level output current	V_{CC} = 4.75 V, I_{IH} = 500 µA, V_O = 1 V	−5			mA
	V_{CC} = 5.25 V, I_{IH} = 500 µA, V_O = 0.25 V			−15	mA
I_{CCL} Total supply current, all outputs low	V_{CC} = 5 V, I_{IL} = 100 µA, I_O = 0		20	35	mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	V_{CC} = 5 V, C_L = 15 pF,		30		ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 1.5 kΩ, See Figure 1		8		ns

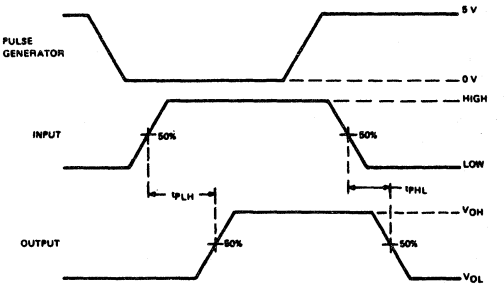
6

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

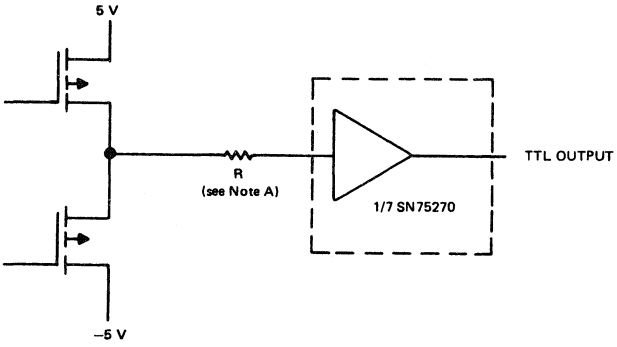
TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

TYPICAL APPLICATION DATA



Note A: $R = \dfrac{V_{OH} - V_{BE}}{I_{OH}}$

V_{OH} = High-level output voltage of MOS device
V_{BE} = Base-Emitter voltage of input transistor of SN75270
I_{OH} = High-level output current of MOS device

example: let $V_{OH} = 4$ V
$I_{OH} = 1$ mA
$V_{BE} = 0.7$ V

$$R = \frac{4 - 0.7}{1} = 3.3\ \text{k}\Omega$$

FIGURE 2–MOS TO SN75270 CONNECTION

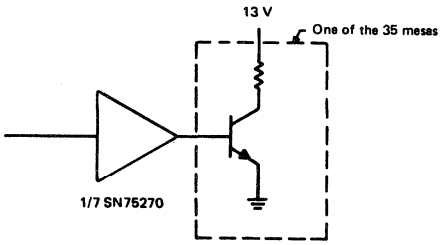


FIGURE 3–THERMAL PRINTHEAD DRIVER FOR THE EPN3600 THERMAL PRINTHEAD

MOS Drivers

7

MOS DRIVERS

INPUT COMPATIBILITY	POWER SUPPLIES (Nominal)	t_{PD}¶ TYPICAL	V_{OH} (MIN)	V_{OL} (MAX)	DEVICE TYPE	PACKAGE TYPE	DRIVERS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
ECL 10K	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_{EE} = −5.2 V	33 ns	V_{CC2} − 0.3 V	0.3 V	SN75368	J,N	2	• Compatible with many popular MOS RAMs including the TMS 1103, TMS 1103-1, TMS 4030, and 7001 • ECL to MOS/TTL driver	7–67
	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{EE} = −5.2 V, V_{BB} = −1.3 V	44 ns	V_{CC2} − 0.4 V	0.5 V	SN75320	J,N	2	• Compatible with the TMS 4030 4K RAM and other popular MOS RAMs • Fixed ECL input reference voltage (SN75321) • External reference voltage (SN75320) • Requires two external P-N-P transistors for operation	7–8
					SN75321	J,N			
TTL	V_{CC1} = 5 V, V_{CC2} = 12 V	20 ns	V_{CC2} − 1.6 V	0.5 V	SN75367	J,N	4	• CMOS applications • 3-state output • Separate address and enable/disable inputs for each driver	7–63
	V_{CC1} = 5 V, V_{CC2} = 12 V	25 ns	V_{CC2} − 1.6 V	1.3 V	SN75357	J,N	4	• CMOS applications • Very low transient current during switching • 3-state output • Separate address and enable/disable inputs for each driver	7–25
	V_{CC1} = 5 V, V_{CC2} = 20 V	31 ns	V_{CC2} − 0.3 V	0.3 V	SN75375	J,N	4	• Compatible with many popular MOS RAMs • Individual V_{CC2} supplies for each driver • Two drivers have single inputs; two have dual inputs	7–99
	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V	31 ns	V_{CC2} − 0.3 V	0.3 V	SN75365	J,N	4	• Compatible with many MOS RAMs including the TMS 1103, TMS 4062, and TMS 4070 16K RAM • V_{CC2} variable from 5 V to 24 V	7–48
	V_{CC1} = 5 V, V_{CC2} = 12 V	31 ns	V_{CC2} − 0.4 V	0.5 V	SN75322	J,N	2	• Compatible with most popular MOS RAMs • Separate driver address inputs with common strobe • Requires two external P-N-P transistors for operation • Low standby power	7–13

¶ t_{PD} = Propagation delay time

MOS DRIVERS (continued)

INPUT COMPATIBILITY	POWER SUPPLIES (Nominal)	t_{PD}¶ TYPICAL	V_{OH} (MIN)	V_{OL} (MAX)	DEVICE TYPE	PACKAGE TYPE	DRIVERS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
TTL	V_{CC1} = 5 V, V_{CC2} = 15 V	31 ns	V_{CC2} – 1 V	0.3 V	SN75350	JG,P	2	• Compatible with many popular MOS RAMs • Lower-voltage, high-speed version of the SN75361A • V_{CC2} variable from 5 V to 18 V	7–17
	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V	32 ns	V_{CC2} – 0.3 V	0.3 V	SN75355	J,N	4	• Compatible with many popular MOS RAMs • Low-voltage version of the SN75365 • V_{CC2} variable from 5 V to 18 V	7–21
	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V	33 ns	V_{CC2} – 0.3 V	0.3 V	SN75366	J,N	4	• Compatible with many popular MOS RAMs • Equivalent to the SN75365 with internal output damping resistor	7–57
	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V	33 ns	V_{CC2} – 0.3 V	0.5 V	SN75363	J,N	2	• Compatible with many MOS RAMs including the TMS 4030 4K RAM and TMS 4070 16K RAM • Separate driver address inputs with common strobe • V_{CC2} variable from 5 V to 15 V	7–39
	V_{CC1} = 24 V, V_{CC2} = 20 V	34 ns	V_{CC2} – 0.3 V	0.3 V	SN75364	JG,P	2	• Compatible with many popular MOS RAMs and shift registers • Single-ended inverting drivers	7–43
	V_{CC} = 20 V	35 ns	V_{CC} – 1 V	0.3 V	SN75369	JG,P	2	• Compatible with many popular MOS RAMs and MOS shift registers • Single-ended inverting drivers	7–75
	V_{CC1} = 5 V, V_{CC2} = 20 V	36 ns	V_{CC2} – 1 V	0.3 V	SN75361A	JG,P	2	• Compatible with many popular MOS RAMs including the TMS 1103, TMS 4062, and TMS 4070 16K RAM • V_{CC2} variable from 5 V to 24 V	7–30
	V_{SS} = 20 V, V_{REF} = 7 V	80 ns			SN75370	J,N	2	Dual read/write amplifier that is designed to interface with I/O terminals of the TMS 4062 and similar type MOS RAMs	7–81
	V_{CC1} = 5 V, See features for V_{CC2} and V_{CC3}	85 ns	V_{CC3} – 0.2 V	V_{CC2}+2 V	SN55180	J,W	2	• Compatible with all MOS devices • 31 V maximum output swing • V_{CC2} variable from –8 V to –25 V • V_{CC3} variable from –20 V to 25 V	7–5

¶ t_{PD} = Propagation delay time

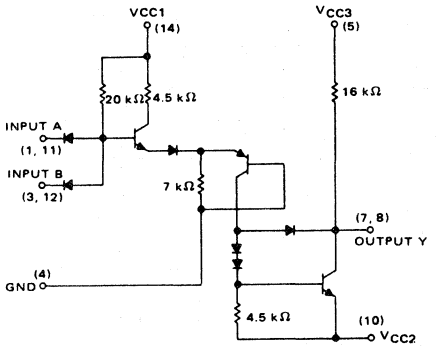
7

TYPE SN55180
DUAL NAND TTL-TO-MOS LEVEL CONVERTER

BULLETIN NO. DL-S 11765, AUGUST 1972 – REVISED APRIL 1981

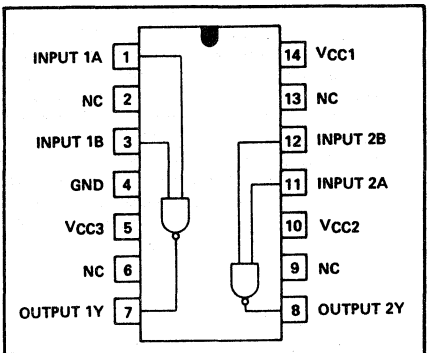
- Output Compatible with All MOS Devices
- Inputs Fully Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with National Semiconductor DS7800 and DS8800
- Standard 5 V Logic Supply Voltage
- Variable V_{CC2} and V_{CC3} Supply Voltages
- 31-Volt Maximum Output Swing
- 1 mW Dissipation with Output at High Level

schematic



Resistor values shown are nominal.

J OR W PACKAGE
(TOP VIEW)



NC – No internal connection

positive logic: $Y = \overline{AB}$

description

The SN55180 consists of two voltage-level converters designed for interfacing between TTL or DTL voltage levels and those levels associated with high-impedance junction or MOS FET-type devices. This device offers the system designer the flexibility of tailoring the output voltage swing to his application. This can be accomplished by varying the V_{CC2} and V_{CC3} supply voltage within the ranges shown in Figure 1. Typical applications include interfacing with MOS shift registers and analog gates.

The SN55180 is characterized for operation over the full military temperature range of –55°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC1} (see Note 1)	7 V
Supply voltage V_{CC2} (see Note 1)	–30 V
Supply voltage V_{CC3} (see Note 1)	30 V
V_{CC3} to V_{CC2} voltage differential	40 V
Input voltage (see Note 1)	5.5 V
Continuous total dissipation at (or below) 112°C free-air temperature (see Note 2)	300 mW
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds	300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 112°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package the chips are alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.5	5	5.5	V
Supply voltage, V_{CC2} (See Figure 1)	−8		−25	V
Supply voltage, V_{CC3} (See Figure 1)			+25 −20	V
Operating free-air temperature, T_A	−55		125	°C

Figure 1 shows the boundary conditions within which it is recommended that the SN55180 be operated for proper functioning of these converters. The range of operation for supply V_{CC2} is shown on the horizontal axis. V_{CC2} must be between −25 V and −8 V. The allowable range for V_{CC3} is governed by V_{CC2}. After a value for V_{CC2} has been chosen, V_{CC3} may be selected as any value along a vertical line passing through the V_{CC2} value and terminated by the boundaries of the recommended operation region. A voltage difference between supplies of at least 5 volts should be maintained for adequate output voltage swing.

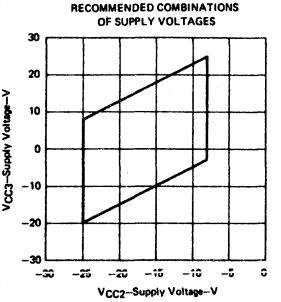


FIGURE 1

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see note 3)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC1} = MIN, V_I = 0.8 V, I_{OH} = 0	V_{CC3}−0.2			V
V_{OL}	Low-level output voltage	V_{CC1} = MIN, V_I = 2 V			V_{CC2}+2	V
$R_{pull-up}$	Output pull-up resistor (internal)	T_A = 25°C	11.5	16	20	kΩ
I_{IH}	High-level input current	V_{CC1} = MAX, V_I = 2.4 V			5	μA
I_I	Input current at maximum input voltage	V_{CC1} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current	V_{CC1} = MAX, V_I = 0.4 V		0.2	0.4	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, outputs high (both converters)	V_{CC1} = MAX, all inputs at 0 V, outputs open		440	820	μA
$I_{CC1(L)}$	Supply current from V_{CC1}, outputs low (both converters)	V_{CC1} = MAX, all inputs at 4.5 V, outputs open		1.7	3.2	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, outputs high (both converters)	V_{CC3} = MAX, all inputs at 0.8 V, outputs open			20	μA

NOTE 3: Minimum and maximum limits apply for all allowable values of V_{CC2} and V_{CC3}.

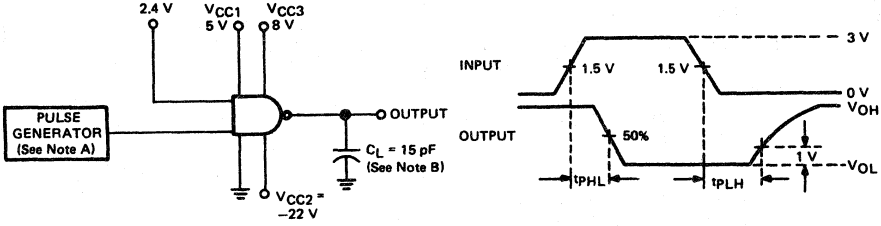
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	2	C_L = 15 pF, See Figure 2		85		ns
t_{PHL}	Propagation delay time, high-to-low-level output		C_L = 15 pF, See Figure 2		85		ns

‡All typical values are at V_{CC1} = 5 V, V_{CC2} = −22 V, V_{CC3} = 8 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 10 ns, t_f = 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS

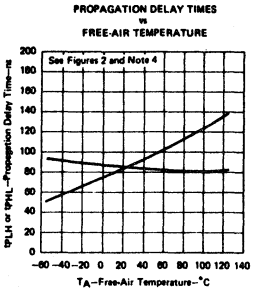


FIGURE 3

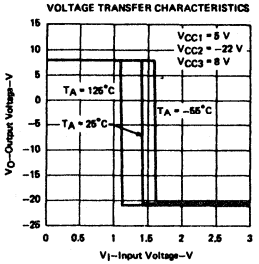


FIGURE 4

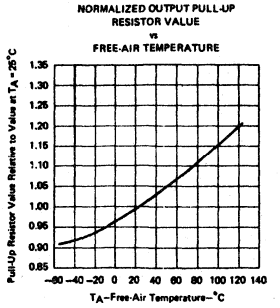


FIGURE 5

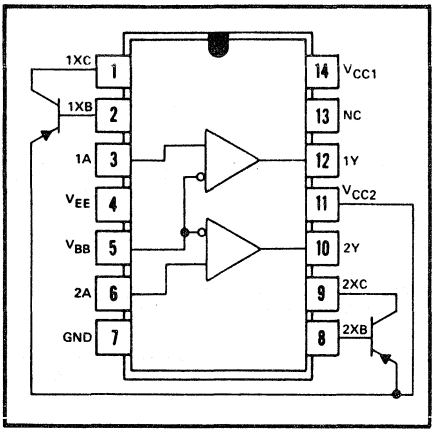
TYPES SN75320, SN75321 DUAL ECL-TO-MOS DRIVERS

BULLETIN NO. DL-S 7712473, APRIL 1977

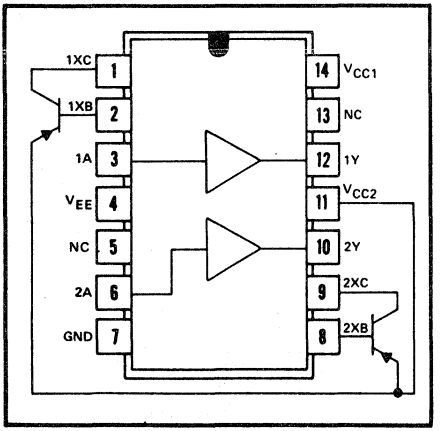
MOS MEMORY INTERFACE

- Dual ECL-to-MOS Drivers
- Versatile Interface Circuit for Use Between ECL and High-Current, High-Voltage Systems
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Inputs Compatible with Series 10000 ECL and Other Similar ECL Families
- Compatible with Many Popular MOS RAMs
- Negligible 12-V Supply Current and Low 5-V Supply Current when Output is at a Low Level
- Requires 2 External P-N-P Transistors per Package for Operation (Use of TIS149, A5T4260, or A5T4261 Recommended)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
SN75320



SN75321



Required external p-n-p transistors should be located as close as possible to the SN75320/SN75321.
NC—No internal connection

description

The SN75320 and SN75321 are monolithic dual ECL-to-MOS driver interface circuits. The devices accept standard input signals from Series 10000 ECL and other similar ECL families and provide high-current, high-voltage output levels suitable for driving MOS circuits. Due to the low power dissipation when the driver output is at a low level, these devices are ideal for driving N-channel RAMs such as the 4-k TMS 4030.

The SN75320 and SN75321 operate from a standard TTL V_{CC} supply (V_{CC1}), ECL V_{EE} supply (V_{EE}), and the MOS V_{SS} supply (V_{CC2}). These devices have been optimized for operation with a V_{CC2} supply voltage from 12 volts to 15 volts, but they are designed to be usable over a much wider range of V_{CC2}.

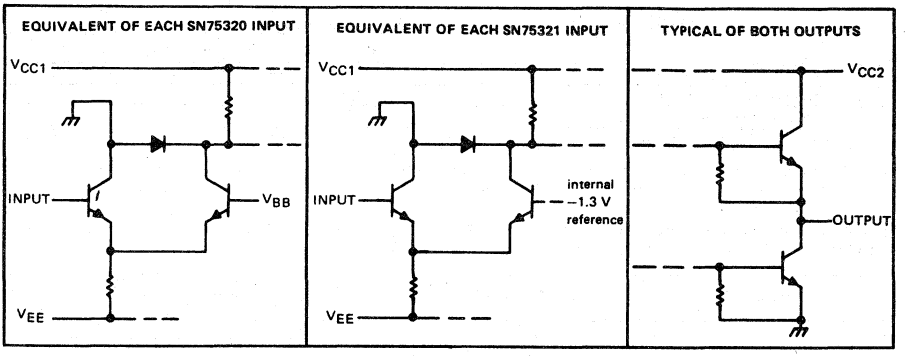
Both devices require two external p-n-p transistors per package. Suggested p-n-p transistors are TIS149, A5T4260, and A5T4261. The SN75320 requires an externally generated ECL input reference voltage, V_{BB}, while the SN75321 features an internally fixed ECL input reference voltage, V_{BB}, of -1.3 V ± 10%. The SN75320 can also be used with differential inputs. Both devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

H = high level, L = low level

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 15 V
Supply voltage range of V_{EE}	−8 V to 0.5 V
Negative voltage of V_{CC1} or V_{CC2} with respect to V_{EE}	−0.5 V
Input voltage range	−8 V to 0.5 V
Input voltage with respect to V_{BB} (SN75320)	5.5 V
Negative voltage at any input with respect to V_{EE}	−5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75320 and SN75321 chips are glass-mounted.

recommended operating conditions

	SN75320			SN75321			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	4.75	12	15	V
Supply voltage, V_{EE}	−4.68	−5.2	−5.72	−4.68	−5.2	−5.72	V
Supply voltage, V_{BB}	−1.23	−1.3	−1.37				V
Operating free-air temperature, T_A	0		70	0		70	°C
Load capacitance, C_L	200			200			pF

definition of input logic levels (see Note 3)

PARAMETER		SN75320 B (LEAST POSITIVE)	SN75320 A (MOST POSITIVE)	SN75321 B (LEAST POSITIVE)	SN75321 A (MOST POSITIVE)	UNIT
V_{IH}	High-level input voltage at input A	−1.15	−0.7	−0.9	−0.7	V
V_{IL}	Low-level input voltage at input A	V_{EE}	−1.45	V_{EE}	−1.6	V
	High-level differential input voltage	150				mV
	Low-level differential input voltage		−150			mV

NOTE 3: This data sheet uses the algebraic limit system that has been adopted by the International Electrotechnical Commission for logic voltage levels. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{EE}, and operating free-air temperature (unless otherwise noted) with V_{BB} = −1.3 V for SN75320.

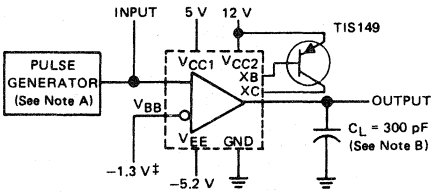
PARAMETER		TEST CONDITIONS		SN75320 MIN	SN75320 TYP†	SN75320 MAX	SN75321 MIN	SN75321 TYP†	SN75321 MAX	UNIT
V_{OH}	High-level output voltage	$V_{IH} = V_{IHB}$	I_{OH} = −10 mA	V_{CC2} −1.1	V_{CC2} −0.7		V_{CC2} −1.1	V_{CC2} −0.7		V
			I_{OH} = −400 μA	V_{CC2} −0.5	V_{CC2} −0.3		V_{CC2} −0.5	V_{CC2} −0.3		
			I_{OH} = −200 μA	V_{CC2} −0.4	V_{CC2} −0.2		V_{CC2} −0.4	V_{CC2} −0.2		
V_{OL}	Low-level output voltage	V_{CC2} = 11.4 V, $V_{IL} = V_{ILA}$, I_{OL} = 10 mA			0.12	0.5		0.12	0.5	V
I_{IH}	High-level input current	V_{EE} = −5.72 V, V_I = −0.7 V			80	800		80	800	μA
I_{IL}	Low-level input current	V_{EE} = −5.72 V, V_I = −2 V				−10			−10	μA
		V_{EE} = −5.72 V, V_I = −5.72 V				−100			−100	
I_{CC1} (H)	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{EE} = −5.72 V, No load			18	26		18	26	mA
I_{CC2} (H)	Supply current from V_{CC2}, both outputs high				9	13		9	13	
I_{EE} (H)	Supply current from V_{EE}, both outputs high				−8	−12		−10	−15	
I_{BB} (H)	Supply current from V_{BB}, both outputs high					−10				μA
I_{CC1} (L)	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{EE} = −5.72 V, No load			18	25		18	25	mA
I_{CC2} (L)	Supply current from V_{CC2}, both outputs low					0.5			0.5	
I_{EE} (L)	Supply current from V_{EE}, both outputs low				−12	−17		−14	−20	
I_{BB} (L)	Supply current from V_{BB}, both outputs low				80	800				μA

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, V_{EE} = −5.2 V, V_{BB} = −1.3 V (SN75320), and T_A = 25°C.

switching characteristics, V_{CC1} = 5V, V_{CC2} = 12 V, V_{EE} = −5.2V, T_A = 25°C

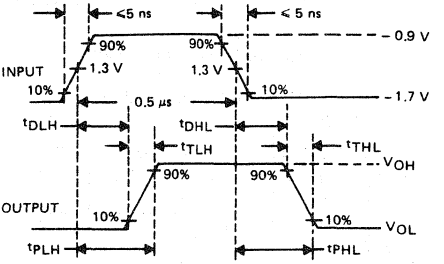
PARAMETER		TEST CONDITIONS	BOTH TYPES MIN	BOTH TYPES TYP	BOTH TYPES MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1		16	24	ns
t_{DHL}	Delay time, high-to-low-level output			30	43	
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			14	20	
t_{PLH}	Propagation delay time, low-to-high-level output			26	44	ns
t_{PHL}	Propagation delay time, high-to-low-level output			44	62	

PARAMETER MEASUREMENT INFORMATION



‡V_{BB} is internally generated on SN75321

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

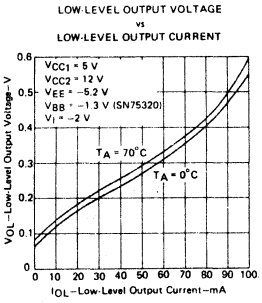


FIGURE 2

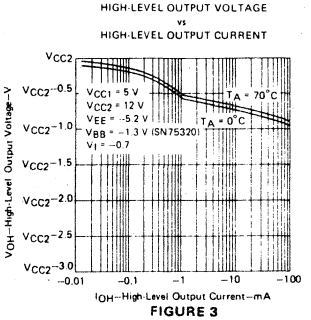


FIGURE 3

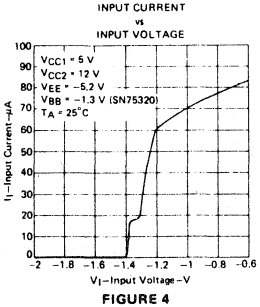


FIGURE 4

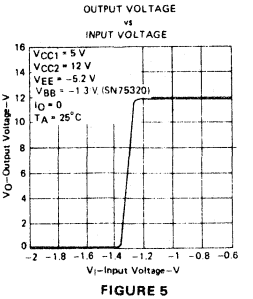


FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

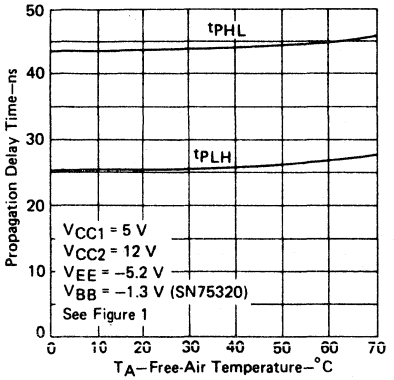


FIGURE 6

DELAY TIMES
vs
FREE-AIR TEMPERATURE

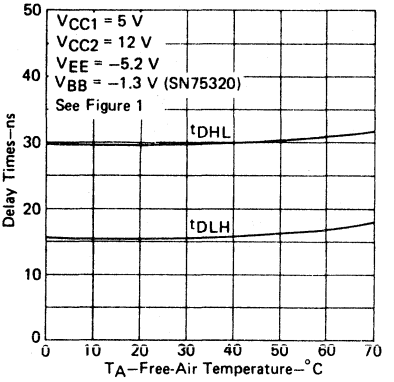


FIGURE 7

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE V_{CC2}

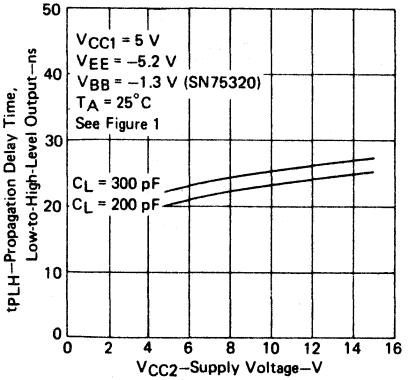


FIGURE 8

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE V_{CC2}

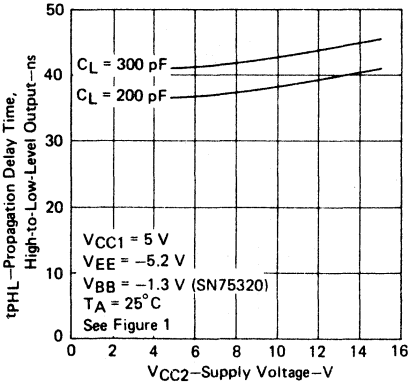


FIGURE 9

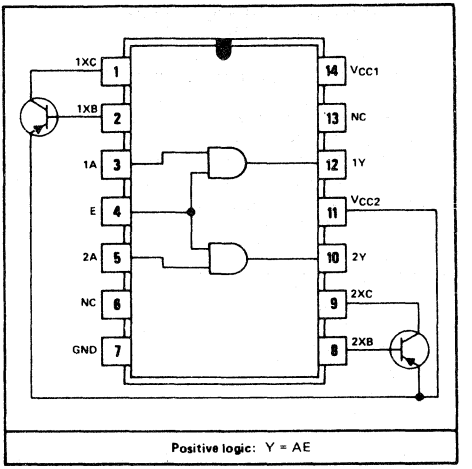
TYPE SN75322
DUAL POSITIVE-AND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712336, MAY 1976–REVISED APRIL 1977

MOS MEMORY INTERFACE

- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{OH} and V_{OL} Compatible with TMS4030 4K RAM and Other Popular MOS RAMs
- Negligible 12-V Supply Current and Low 5-V Supply Current when Output is at a Low Level
- Output in High-Impedance State if 5-V Supply is Lost
- Requires 2 External P-N-P Transistors per Package for Operation (Use of TIS149, A5T4260, or A5T4261 is Recommended)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



Positive logic: Y = AE

Required external p-n-p transistors should be located as close as possible to the SN75322.

description

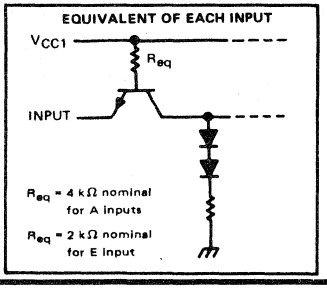
The SN75322 is a monolithic dual TTL-to-MOS driver and interface circuit. The device has separate driver address inputs with common strobe. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. The SN75322 is designed for driving N-Channel RAMs where low power dissipation is desirable when the driver output is at a low level. Specifically, it may be used to drive the chip-enable input of the TMS4030 MOS RAM.

The SN75322 requires two external P-N-P transistors per package. Suggested P-N-P transistors are TIS149, A5T4260, or A5T4261.

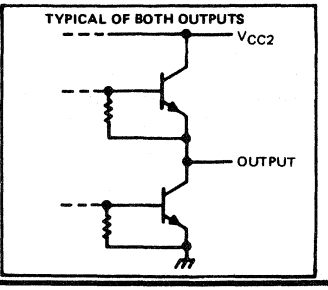
The SN75322 operates from the TTL 5-volt supply and the MOS V_{DD} supply. With the use of an external pull-down resistor, the driver output of the SN75322 will be forced to the low level if the 5-volt supply is lost. The SN75322 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . –0.5 V to 15 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75322 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Operating free-air temperature, T_A	0		70	°C
Load capacitance, C_L	200			pF

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

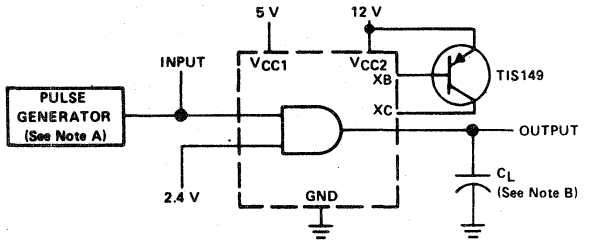
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage		V_{IH} = 2 V, I_{OH} = –10 mA	V_{CC2}–1.1	V_{CC2}–0.9		V
			V_{IH} = 2 V, I_{OH} = –400 µA	V_{CC2}–0.5	V_{CC2}–0.25		
			V_{IH} = 2 V, I_{OH} = –200 µA	V_{CC2}–0.4	V_{CC2}–0.2		
V_{OL}	Low-level output voltage		V_{CC2} = 11.4 V, V_I = 0.8 V, I_{OL} = 10 mA		0.23	0.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A inputs	V_I = 2.4 V			40	µA
		E input				80	
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V		–1	–1.6	mA
		E input			–2	–3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 0 V, No load		15	20	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 0 V, No load		0.01	0.5	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 5 V, No load		24	34	mA
$I_{CC2(H)}$	Supply current from V_{CC2} both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 5 V, No load		9.5	14	mA

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, and T_A = 25°C.

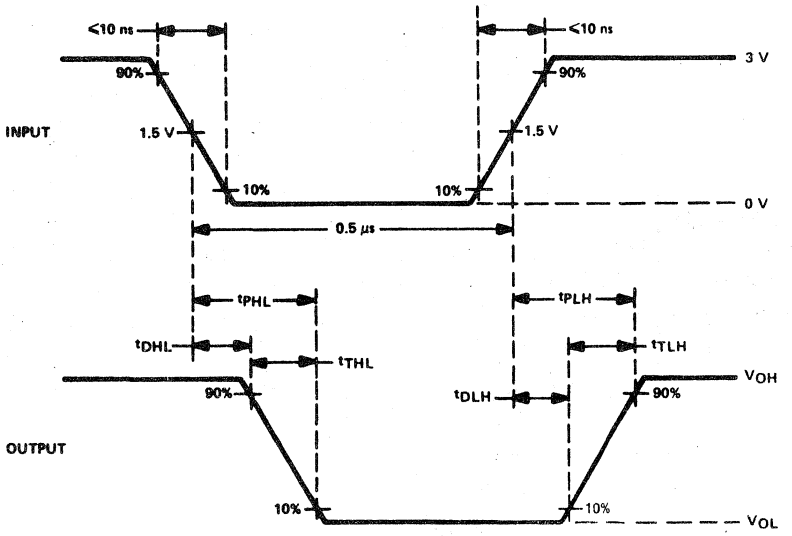
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1		16	21	ns
t_{DHL}	Delay time, high-to-low-level output			18	24	ns
t_{TLH}	Transition time, low-to-high-level output			11	17	ns
t_{THL}	Transition time, high-to-low-level output			13	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		12	27	38	ns
t_{PHL}	Propagation delay time, high-to-low-level output		14	31	44	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

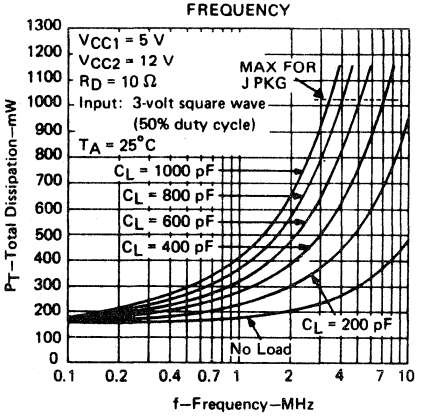
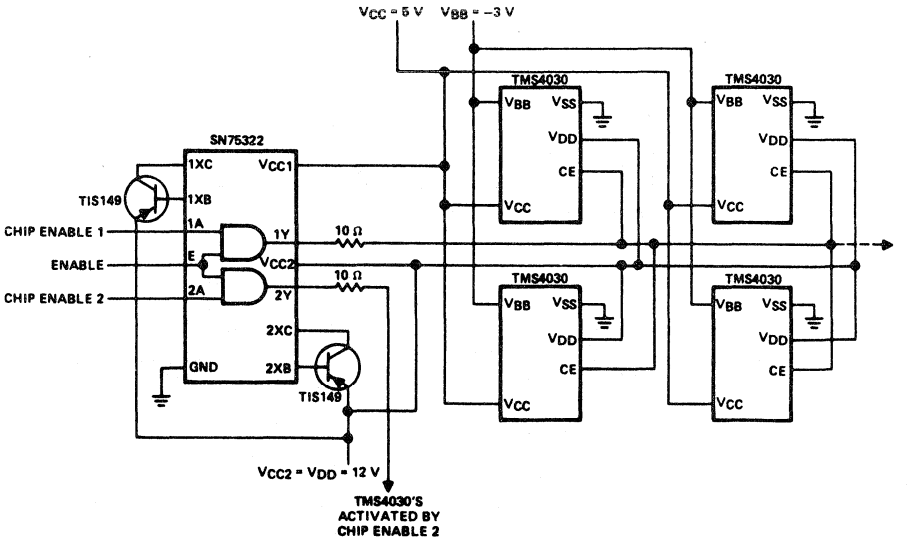


FIGURE 2

TYPICAL APPLICATION DATA



NOTE: The external P-N-P transistors should be located as close as possible to the SN75322.

FIGURE 3—SN75322 DRIVING TMS4030 MEMORIES

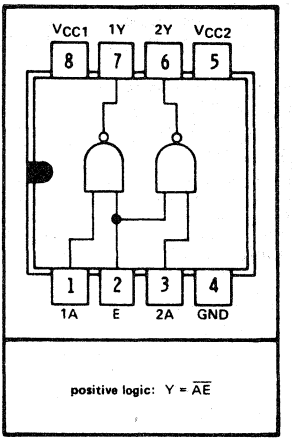
TYPE SN75350
DUAL NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712370, MAY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Lower-Voltage, High-Speed Version of SN75361A
- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible With Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range . . . 5 V to 18 V
- TTL- and DTL-Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Low Standby Power Dissipation
- Special Application . . . 7001 MOS RAM Drivers

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75350 is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs.

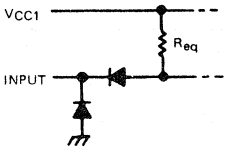
The SN75350 operates from the TTL 5-volt supply and the MOS V_{SS} supply in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 18 volts; however, it is designed so as to be useable over a much wider range of V_{CC2}.

The SN75350 has speed advantages over the SN75361A when driving heavy loads with reduced V_{CC2}.

The SN75350 is characterized for operation from 0°C to 70°C.

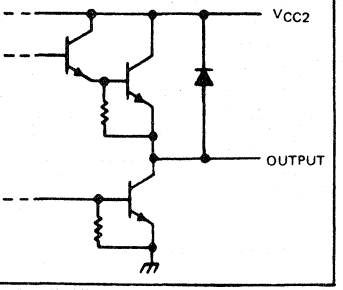
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



R_{eq} = 4 kΩ nominal for A inputs
R_{eq} = 2 kΩ nominal for E input

TYPICAL OF BOTH OUTPUTS



TYPE SN75350
DUAL NAND TTL-TO-MOS DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 20 V
Input voltage . . . . . 5.5 V
Inter-input voltage (see Note 2) . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) : JG package . . . . . 825 mW
: P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75350 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	15	18	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

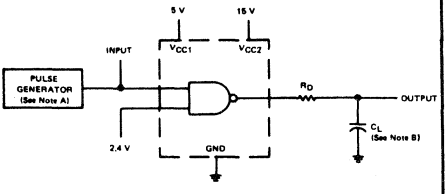
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
		V_{CC2} = 12 V to 18 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E input			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E input		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V,	V_{CC2} = 18 V,		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	All inputs at 0 V,	No load			0.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V,	V_{CC2} = 18 V,		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	All inputs at 5 V,	No load		12	17	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, All inputs at 5 V,	V_{CC2} = 18 V, No load			0.5	mA

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 15 V, and T_A = 25°C.

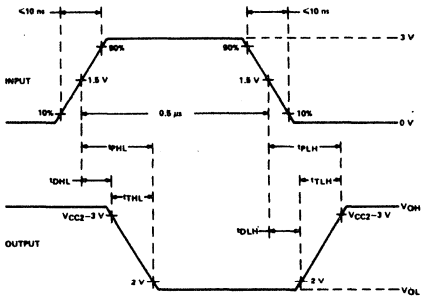
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 15 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		16	24	ns
t_{DHL}	Delay time, high-to-low-level output			15	23	ns
t_{TLH}	Transition time, low-to-high-level output			14	22	ns
t_{THL}	Transition time, high-to-low-level output			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level output			30	46	ns
t_{PHL}	Propagation delay time, high-to-low-level output			31	47	ns

PARAMETER MEASURMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1—SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

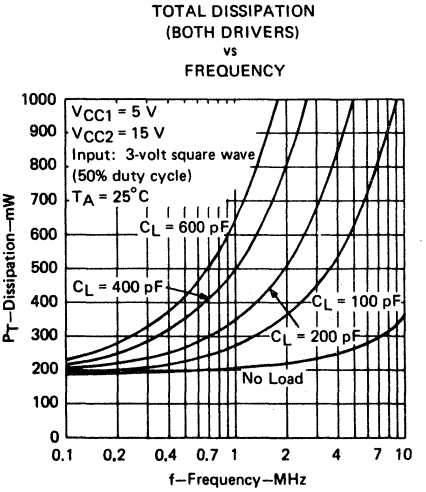


FIGURE 2

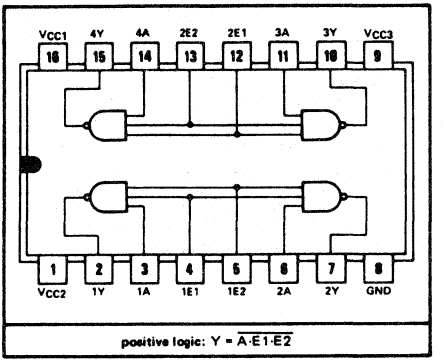
TYPE SN75355
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712371, MAY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range to 18 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL- and DTL-Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Low Standby Power Dissipation
- High-Speed SN75365-Type Device with Lower V_{CC2} Voltage Requirement

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

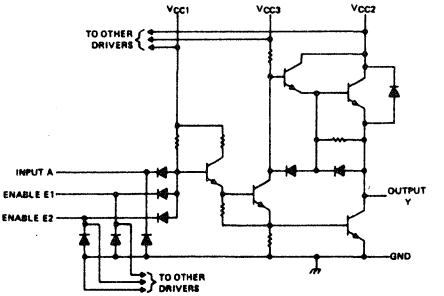
The SN75355 is a monolithic quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs or microprocessor multiphase clock inputs.

The SN75355 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 18 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75355 has speed advantages over the SN75365 when driving highly capacitive loads with V_{CC2} reduced to within the range of 12 to 15 volts.

The SN75355 is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . –0.5 V to 19 V
Supply voltage range of V_{CC3} . . . . . –0.5 V to 19 V
Input voltage . . . . . 5.5 V
Inter-input voltage (see Note 2) . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J package . . . . 1025 mW
N package . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75365 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	15	18	V
Supply voltage, V_{CC3}	V_{CC2}	18	18	V
Voltage difference between supply voltages: V_{CC3}–V_{CC2}	0	3	4	V
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

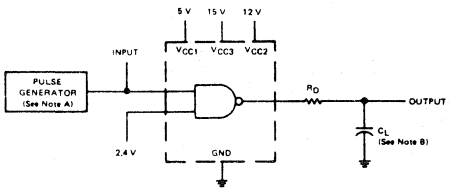
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		V_{CC2}−0.3	V_{CC2}−0.1		V
		V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−1.2	V_{CC2}−0.9		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −50 μA		V_{CC2}−1	V_{CC2}−0.7		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC3} = 12 to 18 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 0 V, No load			4.5	6.5	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−3	−4.5	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				3	5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 5 V, No load			33	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				19	31	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, and T_A = 25°C, except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

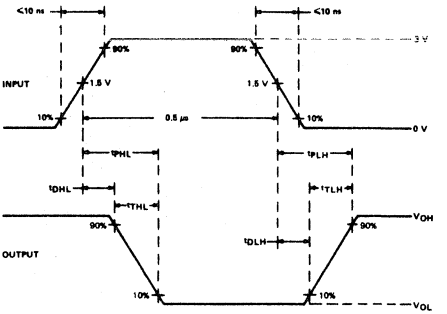
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		18	28	ns
t_{DHL}	Delay time, high-to-low-level output			11	17	ns
t_{TLH}	Transition time, low-to-high-level output			14	21	ns
t_{THL}	Transition time, high-to-low-level output			13	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output			32	49	ns
t_{PHL}	Propagation delay time, high-to-low-level output			24	37	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1—SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(ALL FOUR DRIVERS)
vs
FREQUENCY

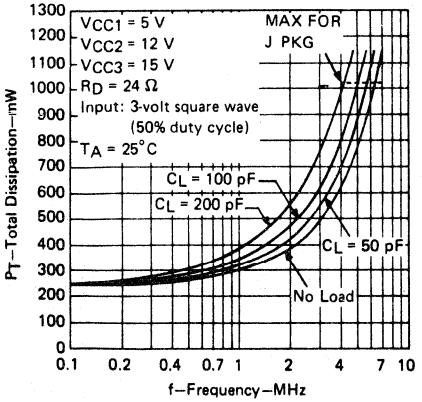


FIGURE 2

TOTAL DISSIPATION
(ALL FOUR DRIVERS)
vs
FREQUENCY

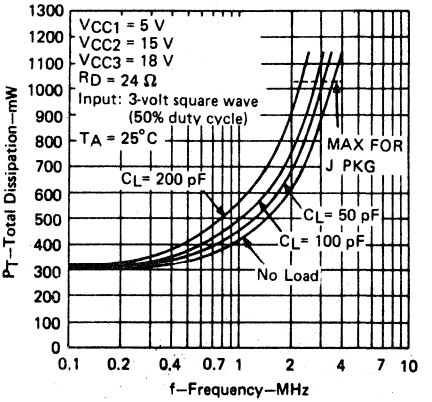


FIGURE 3

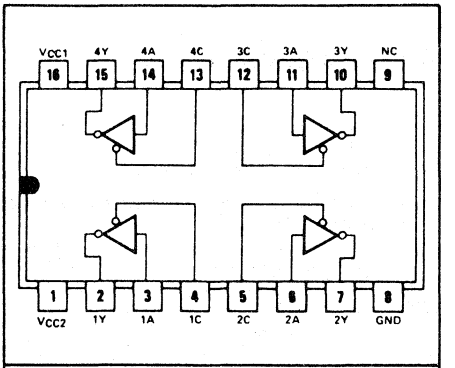
TYPE SN75357
QUADRUPLE TTL-TO-MOS DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7712563, JULY 1977

MOS MEMORY INTERFACE

- Quadruple Inverting TTL-to-MOS Drivers
- 3-State Outputs
- CMOS Applications
- High-Speed Switching
- Very Low Transient Current During Switching
- Separate Address and Enable/Disable Inputs for Each Driver
- V_{CC2} Variable Over Wide Range . . . 5 V to 13.2 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$

Output is off (disabled) when C is high

NC—No internal connection

description

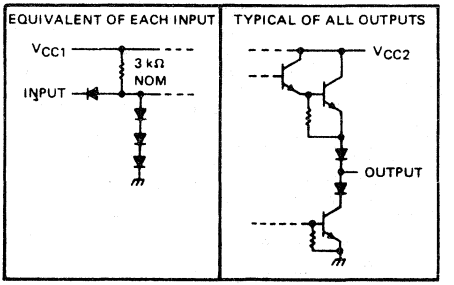
The SN75357 is a monolithic quadruple TTL-to-MOS driver and interface circuit with three-state outputs. The device accepts standard TTL and DTL input signals and creates output levels suitable for driving MOS devices.

Each driver output may be disabled to the high-impedance state by taking the C input high to allow multiple drivers to be connected to the same bus line for selective enable operation. The SN75357 is designed such that the output disable times are shorter than the output enable times to minimize the possibility that two outputs will attempt to take a common bus line to opposite logic levels.

The device has very low transient supply current during switching. It also features a minimum high-level output voltage of V_{CC2} –1.6 volts, and a maximum low-level output voltage of 1.3 volts.

The SN75357 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	–0.5 V to 7 V
Supply voltage range of V_{CC2}	–0.5 V to 15 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75257 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	13.2	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_{OH}	High-level output voltage		V_{CC1} = 4.75 V, A inputs at 0.8 V,	V_{CC2} = 10.8 V, C inputs at 0.8 V,	I_O = −50 μA	V_{CC2}−1.6	V_{CC2}−1.2		V
					I_O = −10 mA	V_{CC2}−2.7	V_{CC2}−2.4		
V_{OL}	Low-level output voltage		V_{CC1} = 4.75 V, C inputs = 0.8 V,	V_{CC2} = 10.8 V, I_O = 10 mA	A inputs at 2 V,		1.0	1.3	V
I_I	Input current at maximum input voltage		V_I = 5.5 V					1	mA
I_{IH}	High-level input current		V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V				−1.5	−2.2	mA
		C inputs						−1.6	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC1} = 5 V, A inputs at 0 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 12 V			−250	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC1} = 5 V, A inputs at 2.4 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 0 V			250	μA
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 13.2 V, No load			11	16	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high							0.6	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 13.2 V, C inputs at 0 V,	No load		17	22	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low						21	30	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off		V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 13.2 V, C inputs at 5 V,	No load		27	36	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off		V_{CC1} = 5.25 V, A input at 0 V,	V_{CC2} = 13.2 V, C inputs at 5 V,	No load		27	36	mA
$I_{CC2(Z)}$	Supply current from V_{CC2}, all outputs off		V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 13.2 V, C inputs at 5 V,	No load		26	34	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, and T_A = 25°C except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 250 pF, See Figures 1 thru 4	10	21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	20	32	ns
t_{TLH}	Transition time, low-to-high level output		5	14	25	ns
t_{THL}	Transition time, high-to-low level output		10	20	32	ns
t_{PZH}	Output enable time to high level		10	22	32	ns
t_{PZL}	Output enable time to low level		12	26	36	ns
t_{PHZ}	Output disable time from high level		1	6	12	ns
t_{PLZ}	Output disable time from low level		10	18	30	ns
$I_{cc2m(LH)}$	Peak transient supply current, low-to-high level output	See Figure 5		20		mA
$I_{cc2m(HL)}$	Peak transient supply current, high-to-low level output			15		mA

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PARAMETER MEASUREMENT INFORMATION

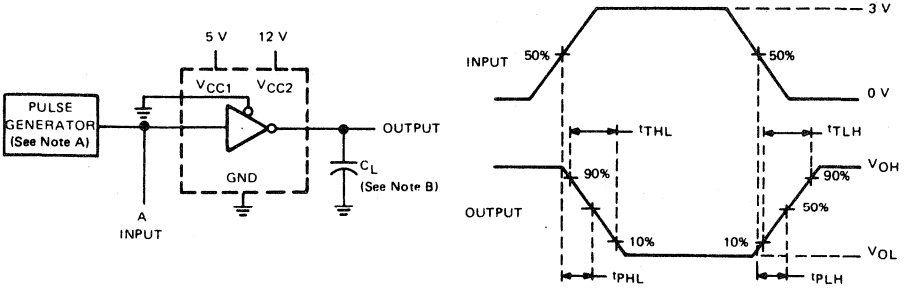
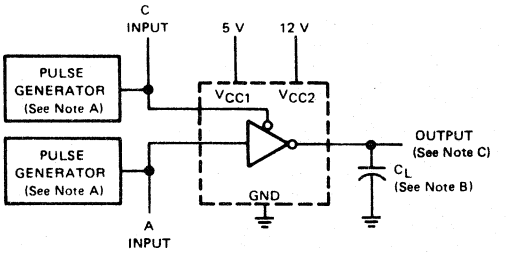


FIGURE 1–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



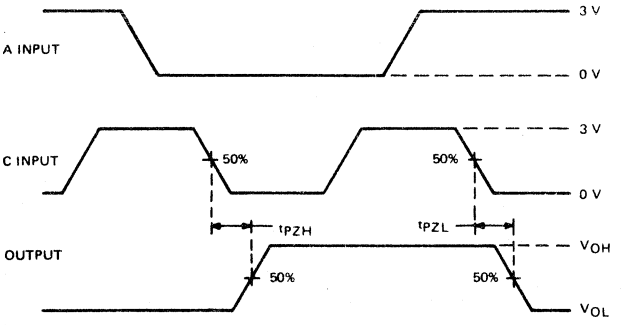


FIGURE 2–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PZH} AND t_{PZL}

NOTES: A. The pulse generators have the following characteristics: PRR = 1 MHz for A input, 2 MHz for C input, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ ns, $R_{in} \geq 1$ MΩ.

PARAMETER MEASUREMENT INFORMATION

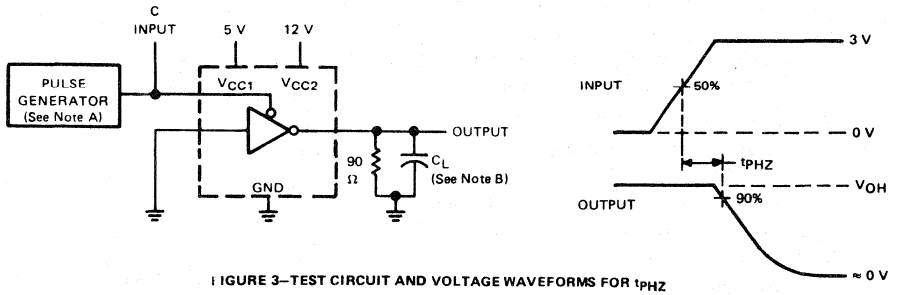


FIGURE 3—TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PHZ}

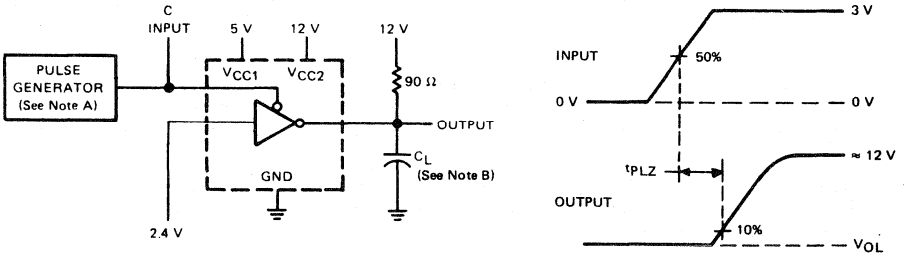


FIGURE 4—TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLZ}

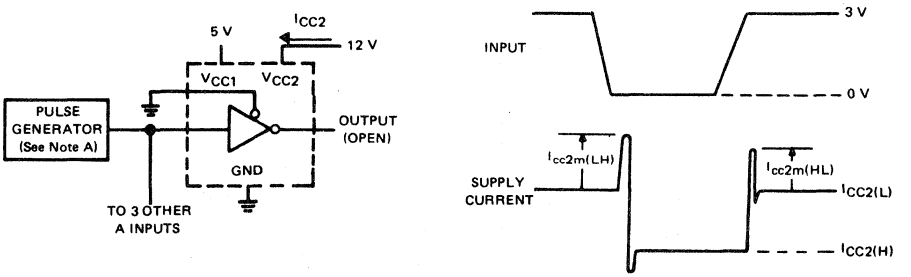


FIGURE 5—TEST CIRCUIT AND WAVEFORMS FOR TRANSIENT SUPPLY CURRENT, ALL 4 DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

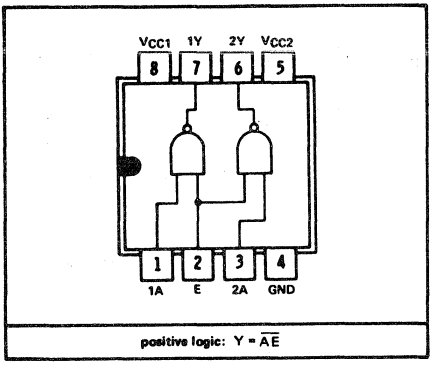
TYPE SN75361A
DUAL NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712054, SEPTEMBER 1973—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



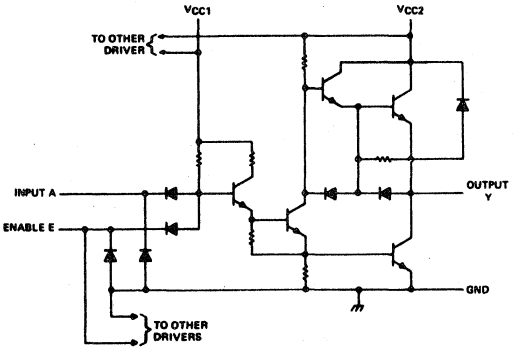
description

The SN75361A is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS 1103 and TMS 4062.

The SN75361A operates from the TTL 5-volt supply and the MOS V_{SS} supply in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts; however, it is designed so as to be useable over a much wider range of V_{CC2}.

The SN75361A is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 25 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75361A chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

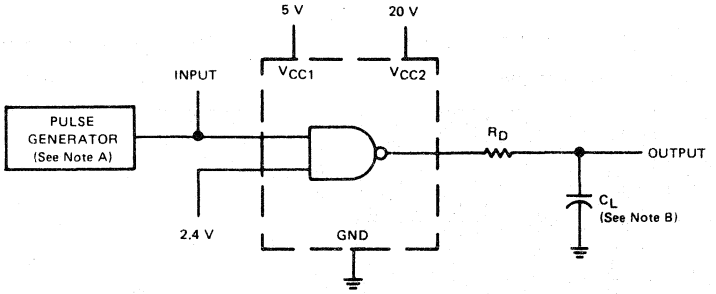
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
		V_{CC2} = 15 V to 24 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	V
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E input			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E input		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V,	V_{CC2} = 24 V,		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	All inputs at 0 V,	No load			0.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V,	V_{CC2} = 24 V,		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	All inputs at 5 V,	No load		7	13	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

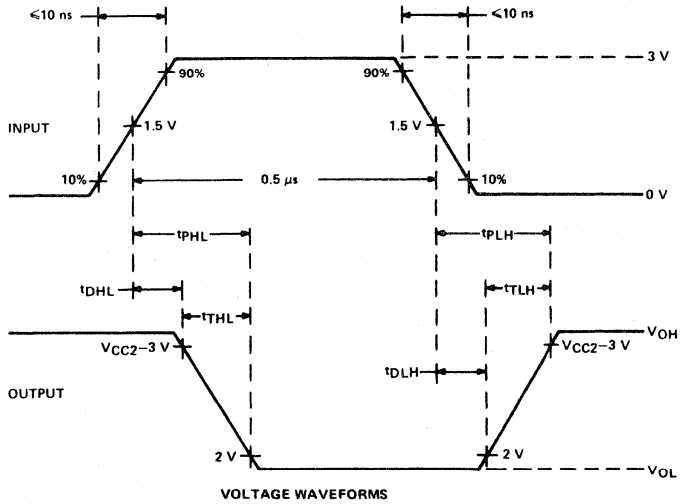
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		11	24	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			25	40	ns
t_{THL}	Transition time, high-to-low-level output			21	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	36	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	31	47	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

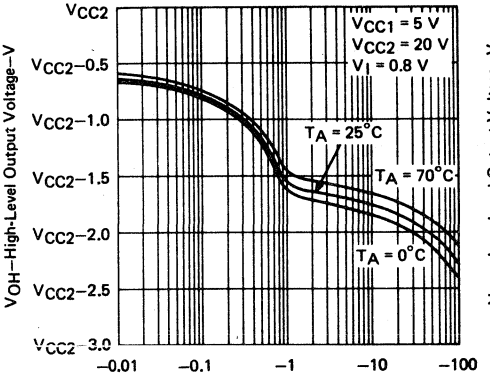


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

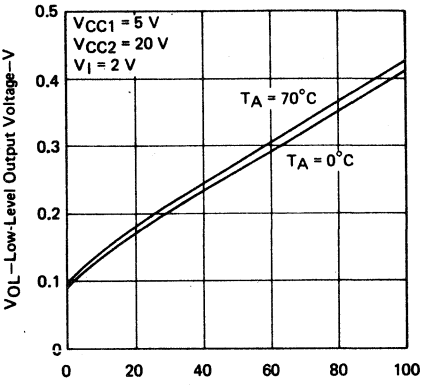


FIGURE 3

7

VOLTAGE TRANSFER CHARACTERISTICS

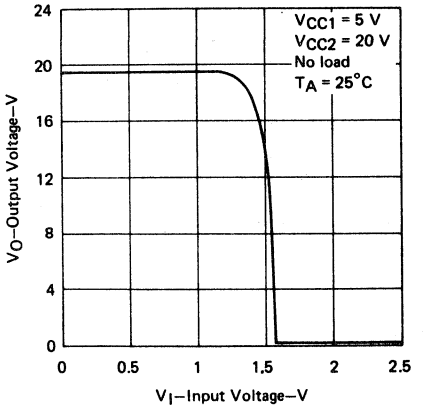


FIGURE 4

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

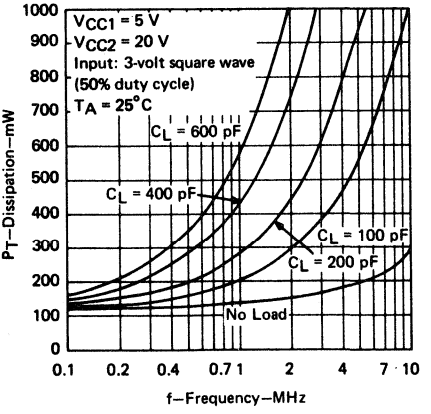


FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

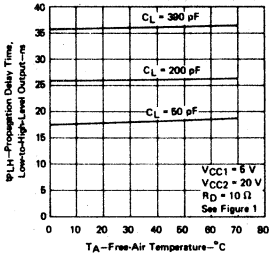


FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

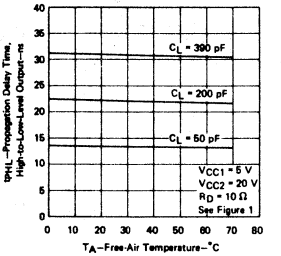


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

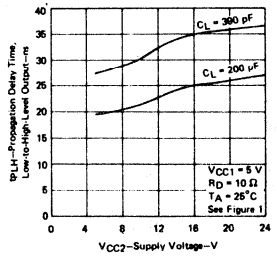


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

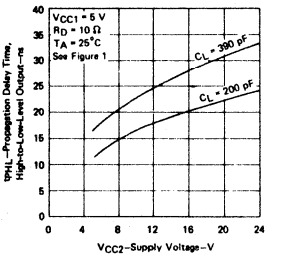


FIGURE 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

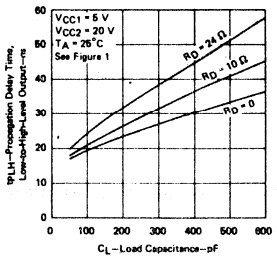


FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

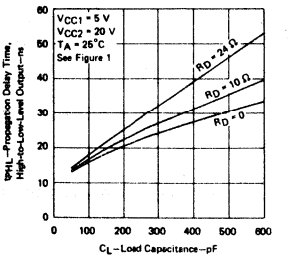


FIGURE 11

TYPICAL APPLICATION DATA

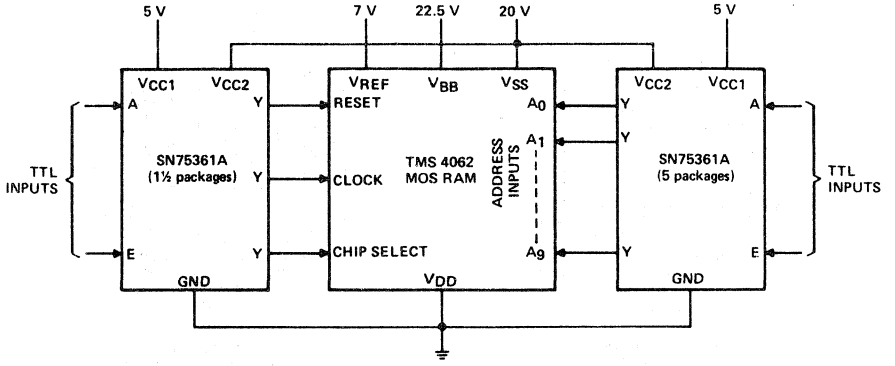


FIGURE 12–INTERCONNECTION OF SN75361A DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

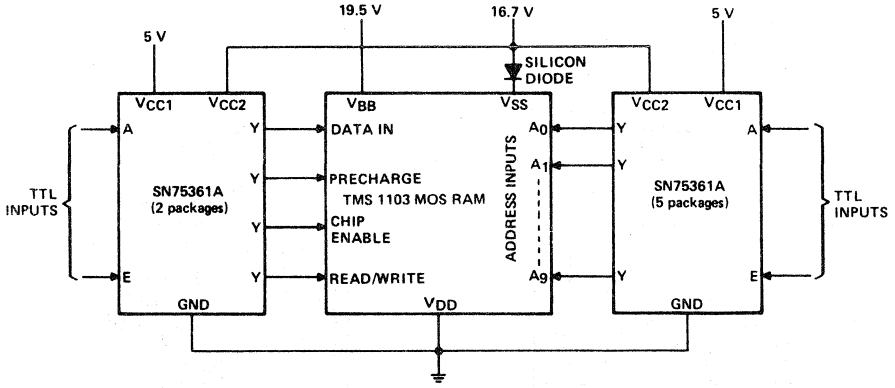


FIGURE 13–INTERCONNECTION OF SN75361A DEVICES WITH '1103-TYPE SILICON-GATE MOS RAM

TYPICAL APPLICATION DATA

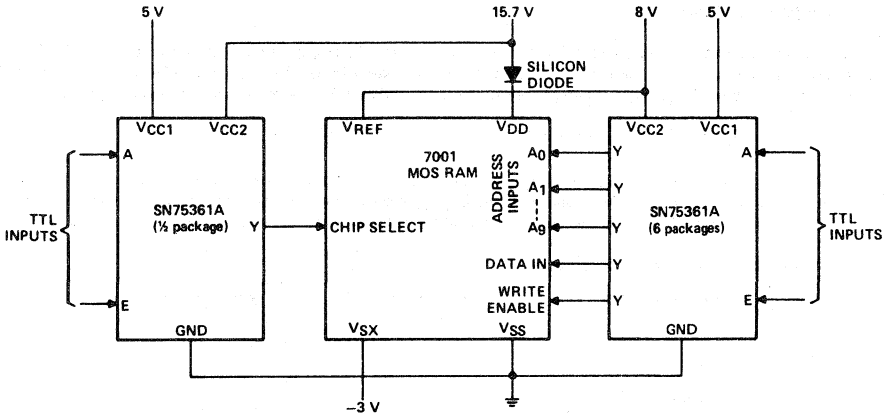


FIGURE 14–INTERCONNECTION OF SN75361A DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM

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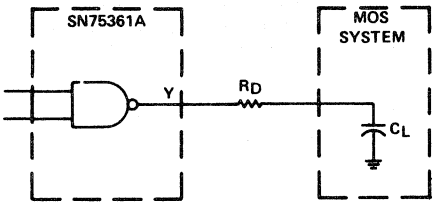


NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional).

FIGURE 15–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75361A APPLICATIONS

Applications using SN75361A as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figures 12, 13, and 14. A silicon diode is used in Figures 13 and 14 to increase the SN75361A high-level output voltage to obtain the desired high-level input voltage required by these MOS RAMs. An extra power supply could be used in place of the diode.

Figures 12, 13, and 14 show the use of the SN75361A over a wide range of V_{CC2} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} to 5 volts.

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between $10\ \Omega$ and $30\ \Omega$. See Figure 15.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75361A driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75361A as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 16.

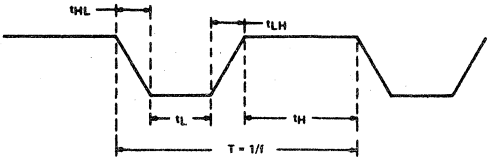


FIGURE 16–OUTPUT VOLTAGE WAVEFORM

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The SN75361A is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H >> t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 5 for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5 V, V_{CC2} = 20 V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3 V, V_{OL} = 0.1 V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V}\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx (200\text{ pF})\ (19.2\text{ V})^2\ (2\text{ MHz})$

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.

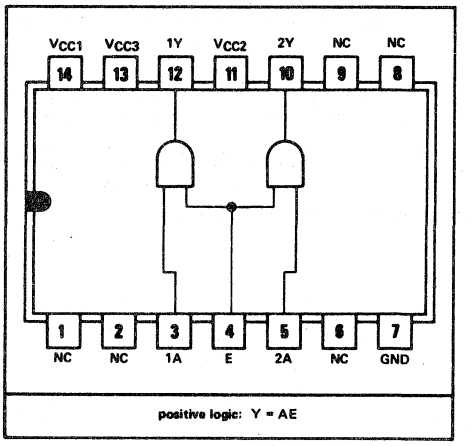
TYPE SN75363
DUAL POSITIVE-AND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712359, FEBRUARY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{CC2} Supply Voltage Variable Over Wide Range
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin can be Connected to V_{CC2} Pin in Some Applications
- Damping Resistor Eliminates Undesired Output Transient Overshoot
- Transient Overdrive Improves Fall Time

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection.

7

description

The SN75363 is a monolithic dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive the chip-enable clock input of the TMS4030 MOS RAM and the address, control, and timing inputs for several other types of MOS RAMs.

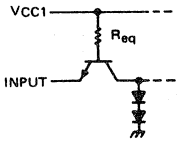
The SN75363 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{DD} supplies. This device has been optimized for operation with V_{CC2} supply voltage from 11 volts to 15 volts, and with nominal V_{CC3} supply voltage from 3 to 4 volts higher than V_{CC2}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

A small series damping resistor has been included in the design to eliminate undesired output transient overshoot due to load or wiring inductance.

The SN75363 is characterized for operation from 0°C to 70°C.

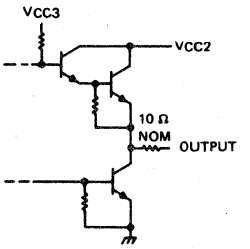
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



R_{eq} = 4 kΩ nominal for A inputs
R_{eq} = 2 kΩ nominal for E input

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 16 V
Supply voltage range of V_{CC3} . . . . . −0.5 V to 19 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75363 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Supply voltage, V_{CC3}	V_{CC2}	15	18	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	3	4	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

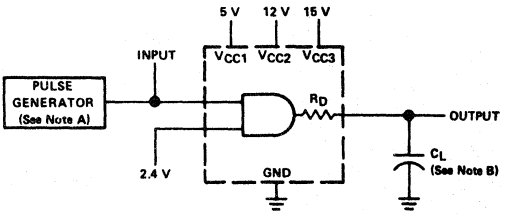
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage		V_{CC2}+3 V = V_{CC3}, V_{IH} = 2 V, I_{OH} = −10 mA	V_{CC2}−1.2	V_{CC2}−1.0		V
			V_{CC2}+3 V = V_{CC3}, V_{IH} = 2 V, I_{OH} = −100 μA	V_{CC2}−0.3	V_{CC2}−0.15		
			V_{CC2} = V_{CC3}, V_{IH} = 2 V, I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		
V_{OL}	Low-level output voltage		V_{CC2} = 10.8 V, V_{CC3} = 10.8 V, V_{IL} = 0.8 V, I_{OL} = 10 mA		0.3	0.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A inputs	V_I = 2.4 V			40	μA
		E input				80	
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V		−1	−1.6	mA
		E input			−2	−3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 12 V, V_{CC3} = 12 V, All inputs at 0 V, No load		7	11	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low		V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 0 V, No load		0.8	1.2	
$I_{CC3(L)}$	Supply current from V_{CC3}, both outputs low				5	9	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 12 V, V_{CC3} = 12 V, All inputs at 5 V, No load		17	25	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high		V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 5 V, No load		−0.8	−1.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, both outputs high				0.8	1.2	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

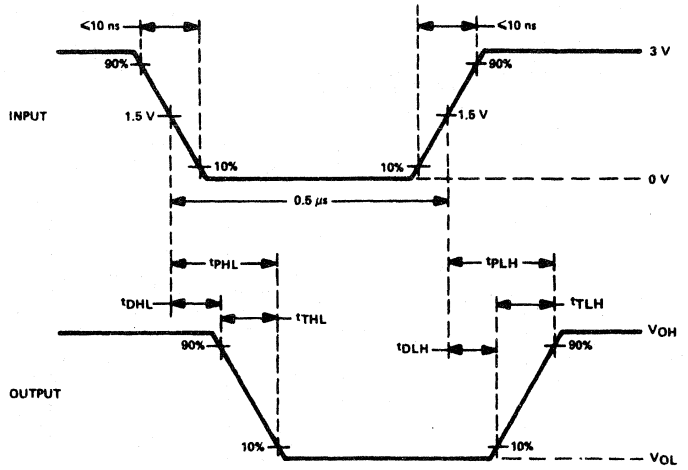
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1	7	12	17	ns
t_{DHL}	Delay time, high-to-low-level output		10	17	24	ns
t_{TLH}	Transition time, low-to-high-level output		10	16	22	ns
t_{THL}	Transition time, high-to-low-level output		10	16	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output		17	28	39	ns
t_{PHL}	Propagation delay time, high-to-low-level output		20	33	46	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

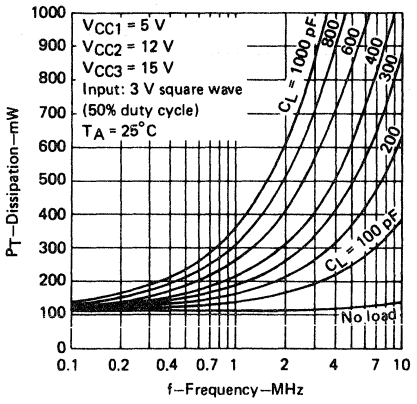


FIGURE 2

SWITCHING TIME
vs
LOAD CAPACITANCE

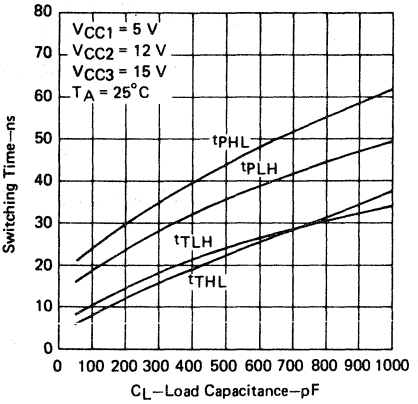


FIGURE 3

TYPICAL APPLICATION DATA

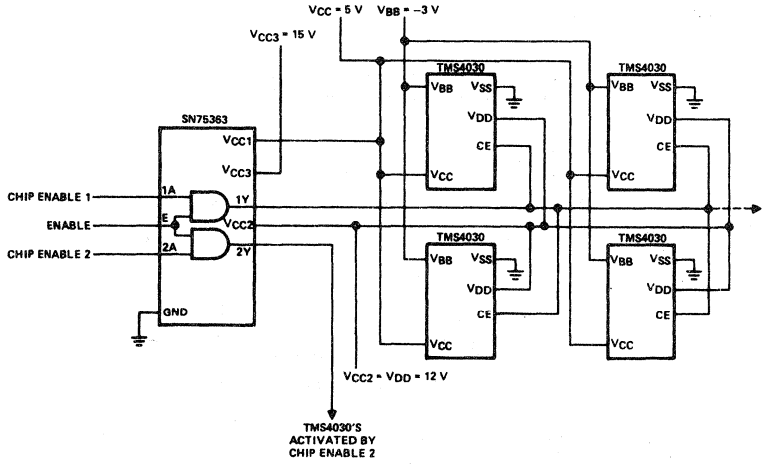


FIGURE 4—SN75363 DRIVING TMS4030 MEMORIES

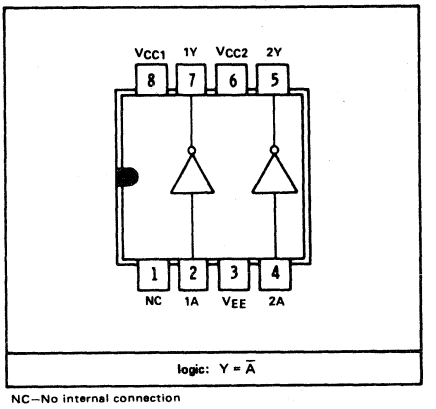
TYPE SN75364
DUAL MOS DRIVER

BULLETIN NO. DL-S 7712373, APRIL 1976—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Inverting MOS Driver
- Versatile Interface Circuit for Use Between TTL Levels and Level-Shifted High-Current, High-Voltage Systems
- Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs and MOS Shift Registers
- V_{CC2} Supply Voltage Variable over Wide Range to 22 Volts Maximum with Respect to V_{EE}
- V_{CC1} Pull-up Supply Voltage Pin Available
- V_{CC1} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- Operates from Standard Bipolar and/or MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

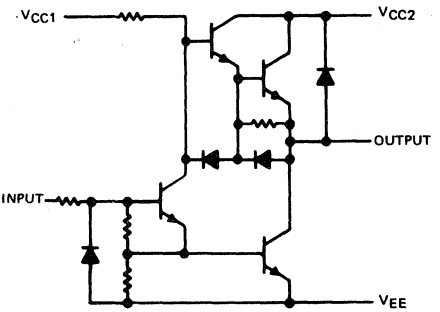
The SN75364 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The SN75364 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 20 volts positive with respect to V_{EE}, and with nominal V_{CC1} supply voltage from 3 volts to 4 volts more positive than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC1} power supply can be eliminated by connecting the V_{CC1} pin to the V_{CC2} pin.

Inputs of the SN75364 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12 volts to −15 volts with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

The SN75364 is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 30 V
Supply voltage range of V_{CC2}	−0.5 V to 22 V
Input voltage	20 V
Positive voltage at any input with respect to V_{CC1}	0.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75364 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	V_{CC2}	24	28	V
Supply voltage, V_{CC2}	4.75	20	22	V
Voltage difference between supply voltages: $V_{CC1}-V_{CC2}$	0	4	10	V
Input voltage			10	V
Operating free-air temperature, T_A	0		70	°C

7

definition of input logic levels

PARAMETER		MIN	MAX	UNIT
V_{IH}	High-level input voltage	5	10	V
V_{IL}	Low-level input voltage		1	V
I_{IH}	High-level input current	8	15	mA
I_{IL}	Low-level input current		0.7	mA

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC1} = V_{CC2} + 3$ V,	$V_{IL} = 1$ V,	$I_{OH} = -100\ \mu A$	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC1} = V_{CC2} + 3$ V,	$I_{IL} = 0.7$ mA,	$I_{OH} = -100\ \mu A$				
		$V_{CC1} = V_{CC2} + 3$ V,	$V_{IL} = 1$ V,	$I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		
		$V_{CC1} = V_{CC2} + 3$ V,	$I_{IL} = 0.7$ mA,	$I_{OH} = -10$ mA				
		$V_{CC1} = V_{CC2}$,	$V_{IL} = 1$ V,	$I_{OH} = -50\ \mu A$	$V_{CC2}-1$	$V_{CC2}-0.7$		
		$V_{CC1} = V_{CC2}$,	$I_{IL} = 0.7$ mA,	$I_{OH} = -50\ \mu A$				
		$V_{CC1} = V_{CC2}$,	$V_{IL} = 1$ V,	$I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		
		$V_{CC1} = V_{CC2}$,	$I_{IL} = 0.7$ mA,	$I_{OH} = -10$ mA				
V_{OL}	Low-level output voltage	$V_{IH} = 5$ V,	$I_{OL} = 10$ mA			0.15	0.3	V
		$I_{IH} = 8$ mA,	$I_{OL} = 10$ mA					
		$V_{CC1} = 15$ V to 28 V,	$V_{IH} = 5$ V,	$I_{OL} = 40$ mA		0.25	0.5	
		$V_{CC1} = 15$ V to 28 V,	$I_{IH} = 8$ mA,	$I_{OL} = 40$ mA				
V_{OK}	Output clamp voltage	$V_I = 0$ V,	$I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
V_I	Input voltage	$V_{CC1} = 13.5$ V to 28 V,	$I_I = 15$ mA			9	13.5	V
		$I_I = 8$ mA				5.5	8	
		$I_I = 0.7$ mA				0.7	1	
I_I	Input current	$V_{CC1} = 10$ V to 28 V,	$V_I = 10$ V			17	26	mA
		$V_I = 5$ V				7	11	
		$V_I = 1$ V				1.1	1.6	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	$V_{CC1} = 26$ V,	$V_{CC2} = 22$ V,			1.0	2	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	Both inputs at 0 V,	No load			−1.0	+0.25 −1.6	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	$V_{CC1} = 28$ V,	$V_{CC2} = 22$ V,			7	14	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	Both inputs at 7 V,	No load			0.5	1	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	$V_{CC1} = 22$ V,	$V_{CC2} = 22$ V,				0.5	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	Both inputs at 0 V,	No load				0.25	

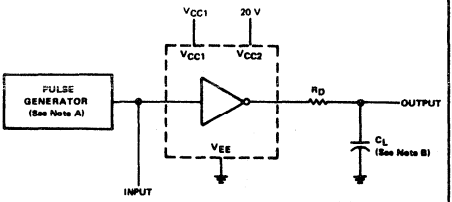
†All typical values are at $V_{CC1} = 24$ V, $V_{CC2} = 20$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

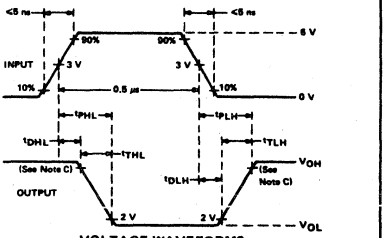
switching characteristics, $V_{CC2} = 20$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC1} = 24$ V			$V_{CC1} = 20$V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10\ \Omega$, See Figure 1	2	13	23	3	14	24	ns
t_{DHL}	Delay time, high-to-low-level output		1	9	18	1	10	18	ns
t_{TLH}	Transition time, low-to-high-level output		8	21	24	8	21	34	ns
t_{THL}	Transition time, high-to-low-level output		6	19	30	5	18	29	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	34	57	11	35	58	ns
t_{PHL}	Propagation delay time, high-to-low-level output		8	28	47	8	28	47	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The high-level reference point is 17 V when $V_{CC1} = V_{CC2} = 20$ V and is 18 V when $V_{CC1} = V_{CC2} + 4$ V = 24 V.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

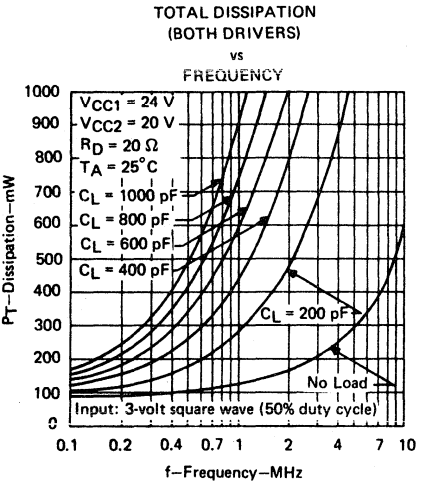
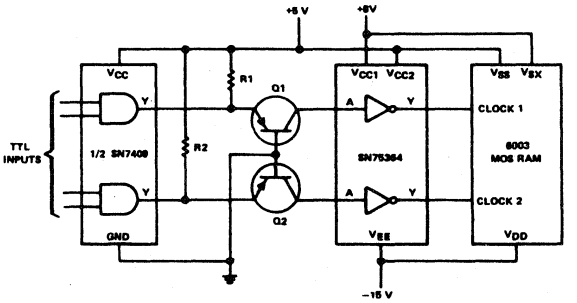


FIGURE 2

TYPICAL APPLICATION DATA



NOTES: R1 and R2 ≈ 350 Ω to 500 Ω.
Q1 and Q2 are 2N3829 or similar p-n-p transistors.

FIGURE 3–MOS RAM CLOCK DRIVER SYSTEM WITH P-N-P TRANSITOR CURRENT SOURCE USED TO LEVEL-SHIFT TO INPUTS OF SN75364

TYPICAL APPLICATION DATA

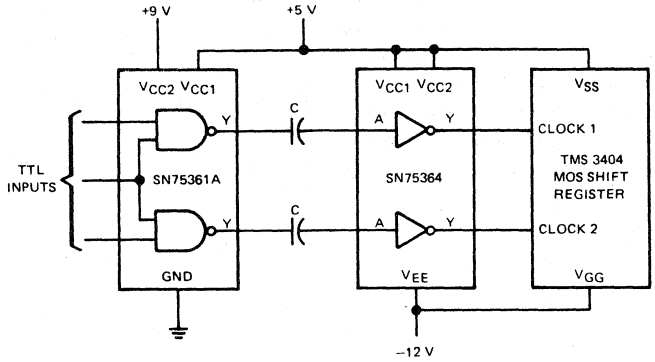
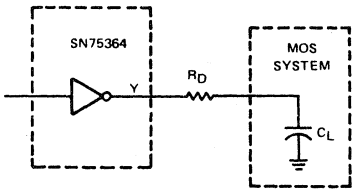


FIGURE 4—MOS SHIFT REGISTER CLOCK DRIVER SYSTEM WITH CAPACITIVE COUPLING USED TO LEVEL-SHIFT TO INPUTS OF SN75364



NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional)

FIGURE 5—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75364 APPLICATIONS

Applications of the SN75364 used as an interface device in systems converting TTL signals to negative polarity MOS clock signals are shown in Figures 3 and 4. In both applications the SN75364 V_{EE} pin is connected to a negative MOS supply voltage. The V_{CC1} supply pin may be connected to the V_{CC2} pin as shown in Figure 4 or connected to a separate voltage more positive than V_{CC2}, as shown in Figure 3. The SN75364 may be used over a wide range of V_{CC1} and V_{CC2} supply voltage. However, for proper operation, the voltage at the inputs of the SN75364 should not be more positive than the voltage at V_{CC1}.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the SN75364, which are referenced to the V_{EE} terminal. A p-n-p transistor current source is used to level shift in Figure 3. Resistor R sets the current and an open-collector TTL gate is used to switch the p-n-p transistor. Figure 4 shows capacitive coupling being used to level shift with the SN75361A TTL-to-MOS driver used as a low-impedance voltage-source driver. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

The fast switching speeds of the SN75364 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 5.

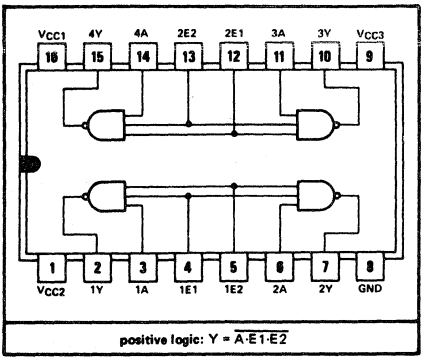
TYPE SN75365
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712058, SEPTEMBER 1973—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Designed to be Interchangeable with Intel 3207
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot E1 \cdot E2}$

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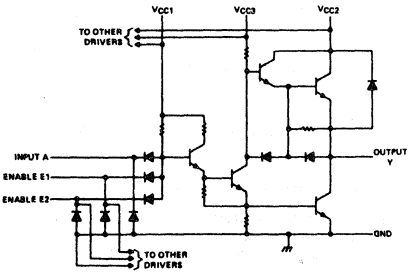
description

The SN75365 is a monolithic integrated quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103 and TMS4062.

The SN75365 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75365 is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 25 V
Supply voltage range of V_{CC3}	−0.5 V to 30 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75365 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	4	10	V
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

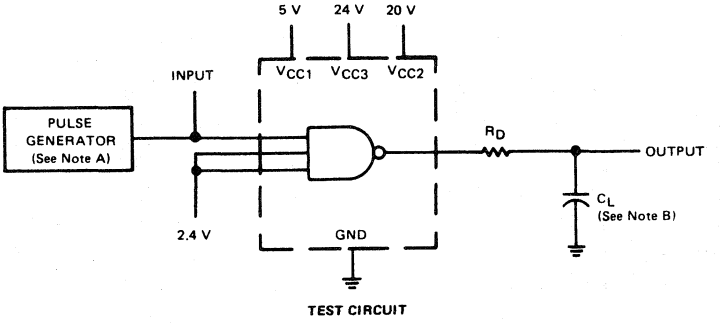
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{CC3} = V_{CC2} + 3$ V, $V_{IL} = 0.8$ V, $I_{OH} = -100$ μA		$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2} + 3$ V, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA		$V_{CC2}-1.2$	$V_{CC2}-0.9$		
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -50$ μA		$V_{CC2}-1$	$V_{CC2}-0.7$		
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA		$V_{CC2}-2.3$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15$ V to 28 V, $V_{IH} = 2$ V, $I_{OL} = 40$ mA			0.25	0.5	
V_{OK}	Output clamp voltage	$V_I = 0$ V, $I_{OH} = 20$ mA				$V_{CC2}+1.5$	V
I_I	Input current at maximum input voltage	$V_I = 5.5$ V				1	mA
I_{IH}	High-level input current	$V_I = 2.4$ V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	$V_I = 0.4$ V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V, All inputs at 0 V, No load			4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−2.2	+0.25 −3.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V, All inputs at 5 V, No load			31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	$V_{CC1} = 0$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

†All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

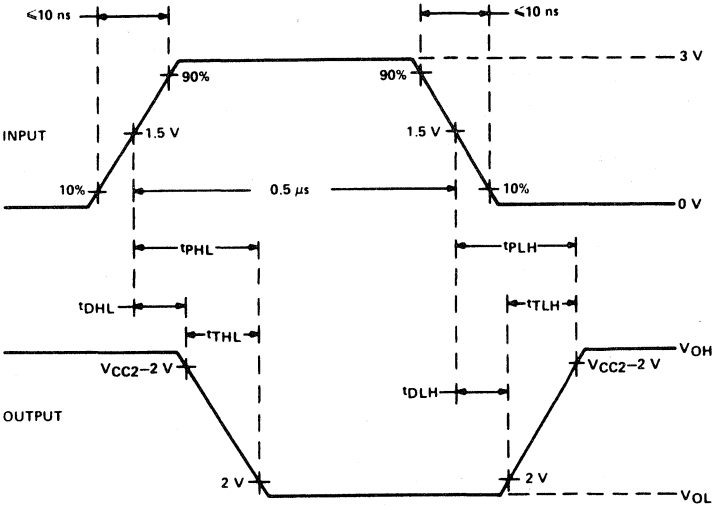
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	$C_L = 200$ pF, $R_D = 24\ \Omega$, See Figure 1		11	20	ns
t_{DHL}	Delay time, high-to-low-level output			10	18	ns
t_{TLH}	Transition time, low-to-high-level output			20	33	ns
t_{THL}	Transition time, high-to-low-level output			20	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	31	48	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	46	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

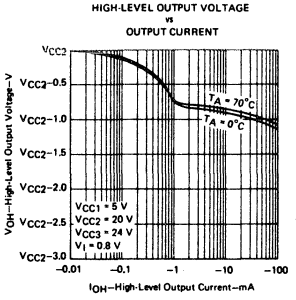


FIGURE 2

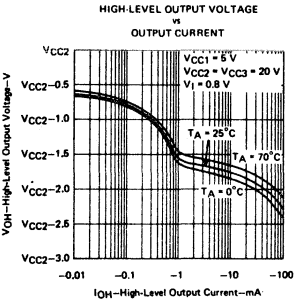


FIGURE 3

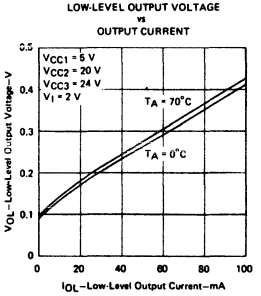


FIGURE 4

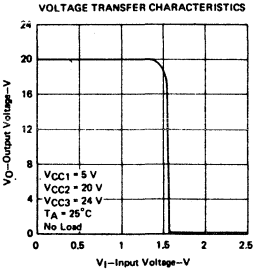


FIGURE 5

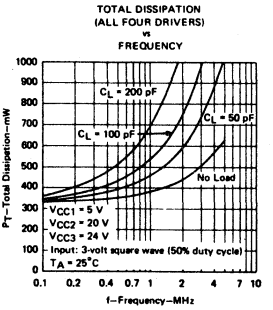


FIGURE 6

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

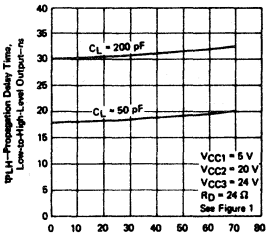


FIGURE 7

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

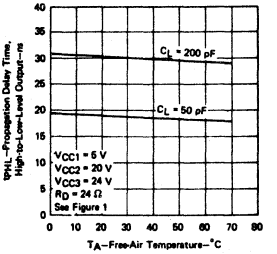


FIGURE 8

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs V_{CC2} SUPPLY VOLTAGE

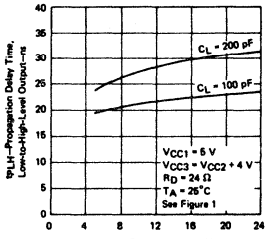


FIGURE 9

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs V_{CC2} SUPPLY VOLTAGE

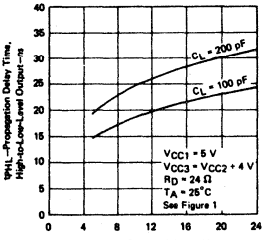


FIGURE 10

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs LOAD CAPACITANCE

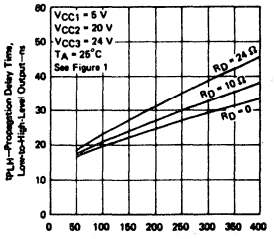


FIGURE 11

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs LOAD CAPACITANCE

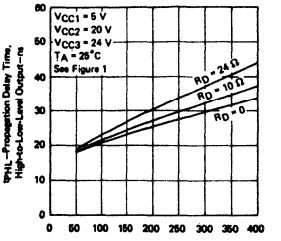


FIGURE 12

TYPICAL APPLICATION DATA

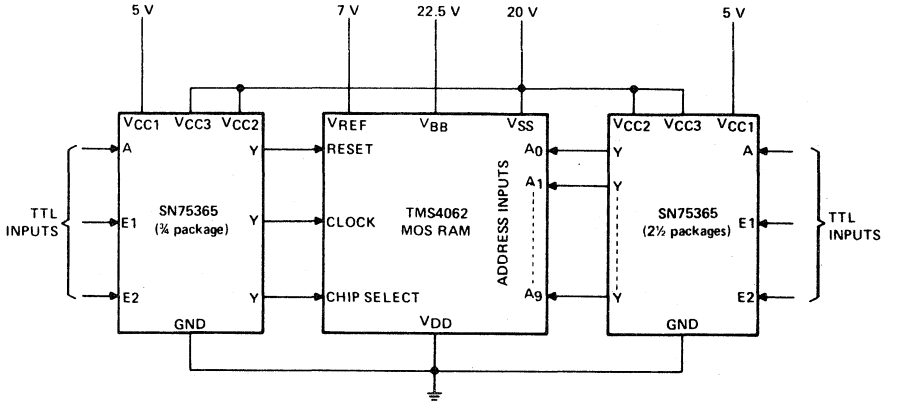


FIGURE 13—INTERCONNECTION OF SN75365 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

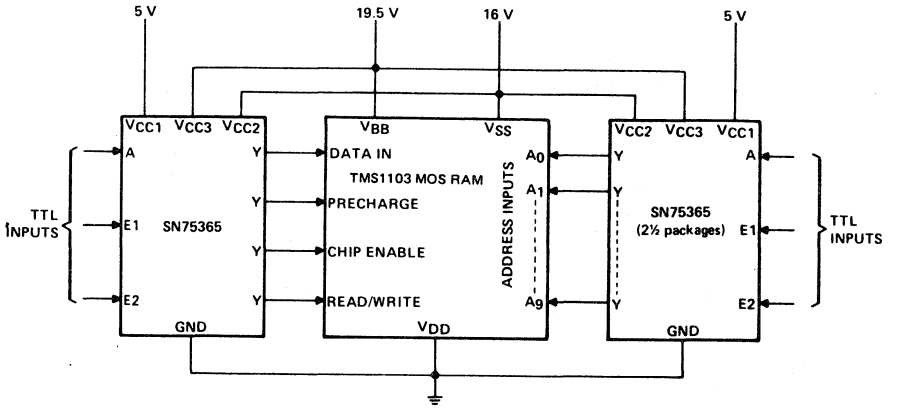


FIGURE 14—INTERCONNECTION OF SN75365 DEVICES WITH TMS1103-TYPE SILICON-GATE MOS RAM

TYPICAL APPLICATION DATA

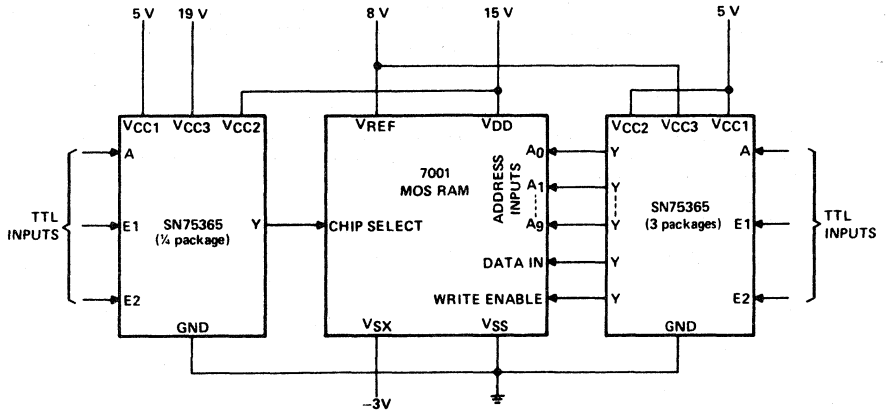


FIGURE 15—INTERCONNECTION OF SN75365 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM

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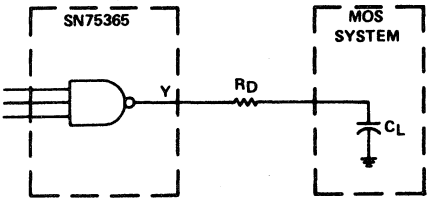


NOTE: $R_D \approx 10\ \Omega$ TO $30\ \Omega$ (optional).

FIGURE 16—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75365 APPLICATIONS

Applications using SN75365 as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figures 13, 14, and 15. The V_{CC3} supply pin of the SN75365 may be connected to the V_{CC2} pin as shown in Figure 13 or connected to a separate voltage higher than V_{CC2} as shown in Figures 14 and 15.

Figures 13, 14, and 15 show the use of the SN75365 over a wide range of V_{CC2} and V_{CC3} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} and V_{CC3} to 5 volts.

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between $10\ \Omega$ and $30\ \Omega$. See Figure 16.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75365 driver when charging and discharging high capacitance loads over a wide voltage range at high-frequencies. Figure 6 shows the power dissipated in a typical SN75365 as a function of frequency and load capacitance. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 17.

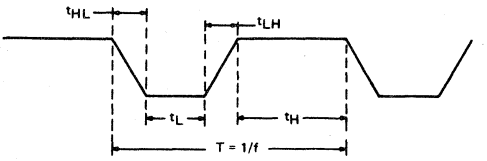


FIGURE 17—OUTPUT VOLTAGE WAVEFORM

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The SN75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H >> t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 6 for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20 V, V_{OL} = 0.1 V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) +$$

$$\left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})(19.9\text{ V})^2(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \approx 4(58 + 79)$

$P_{T(AV)} \approx 548$ mW typical for total package.

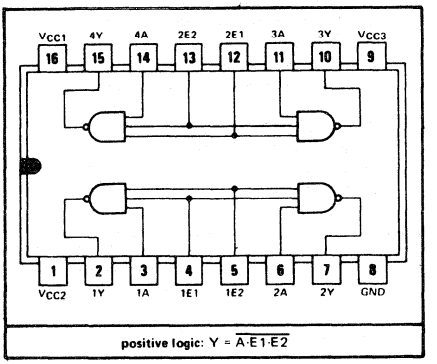
TYPE SN75366
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712159, APRIL 1975—REVISED APRIL 1977

MOS MEMORY INTERFACE

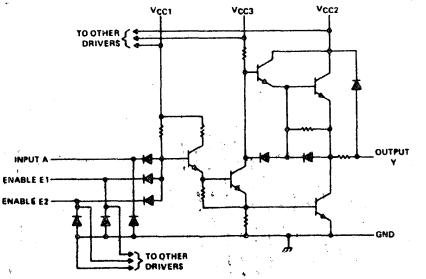
- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Equivalent to SN75365 with Internal Output Damping Resistors
- No External Damping Resistors Needed in Most Applications
- Designed to be Interchangeable with Intel 3207
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot E1 \cdot E2}$

schematic (each driver)



description

The SN75366 is a monolithic integrated quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103 and TMS4062.

The SN75366 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75366 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)		−0.5 V to 7 V
Supply voltage range of V_{CC2}		−0.5 V to 25 V
Supply voltage range of V_{CC3}		−0.5 V to 30 V
Input voltage		5.5 V
Inter-input voltage (see Note 2)		5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	J package	1025 mW
	N package	1150 mW
Operating free-air temperature range		0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the drivers.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75366 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	4	10	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

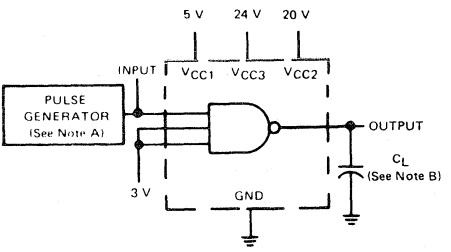
	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC3} = V_{CC2}+3 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		V_{CC2}−0.3	V_{CC2}−0.1		V
		V_{CC3} = V_{CC2}+3 V, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−1.7	V_{CC2}−1.2		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −50 μA		V_{CC2}−1	V_{CC2}−0.7		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−2.8	V_{CC2}−2.1		
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 1 mA			0.15	0.3	V
		V_{CC3} = 10 V to 28 V, V_{IH} = 2 V, I_{OL} = 30 mA			1.2	1.9	
V_{OK}	Output clamp voltage	V_I = 0 V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 0 V, No load			4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−2.2	+0.25 −3.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 5 V, No load			31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low				0.9	2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V (unless otherwise noted), and T_A = 25°C.

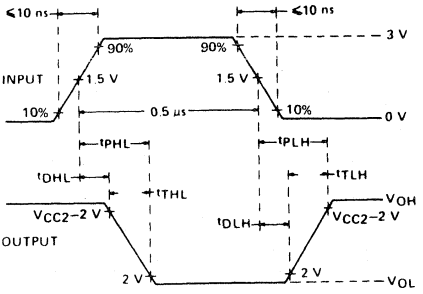
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, See Figure 1		15	22	ns
t_{DHL}	Delay time, high-to-low-level output			14	21	ns
t_{TLH}	Transition time, low-to-high-level output		5	18	33	ns
t_{THL}	Transition time, high-to-low-level output		5	18	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	33	48	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	32	48	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

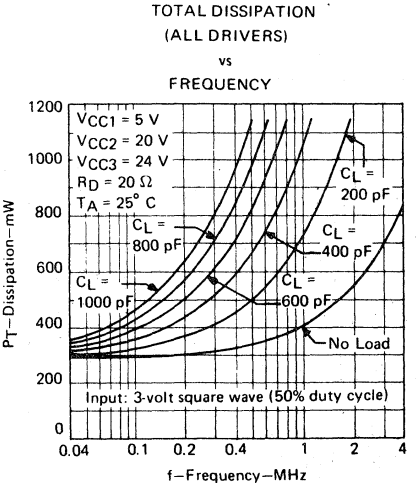


FIGURE 2

TYPICAL APPLICATION DATA

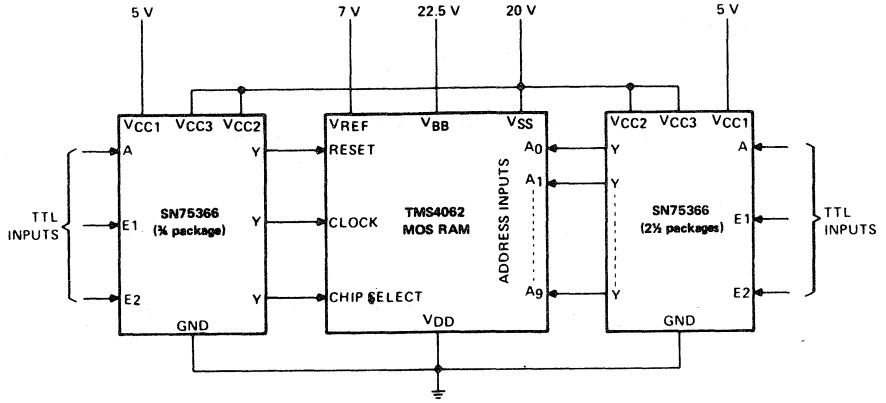


FIGURE 3—INTERCONNECTION OF SN75366 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

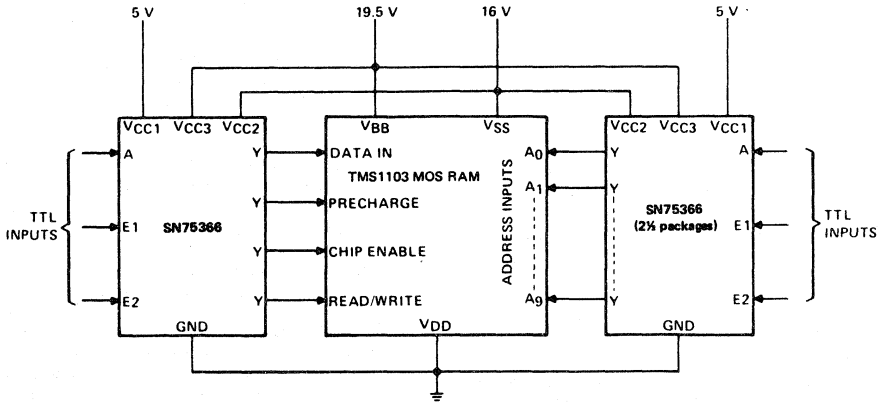


FIGURE 4—INTERCONNECTION OF SN75366 DEVICES WITH TMS1103-TYPE SILICON-GATE MOS RAM

TYPICAL APPLICATION DATA

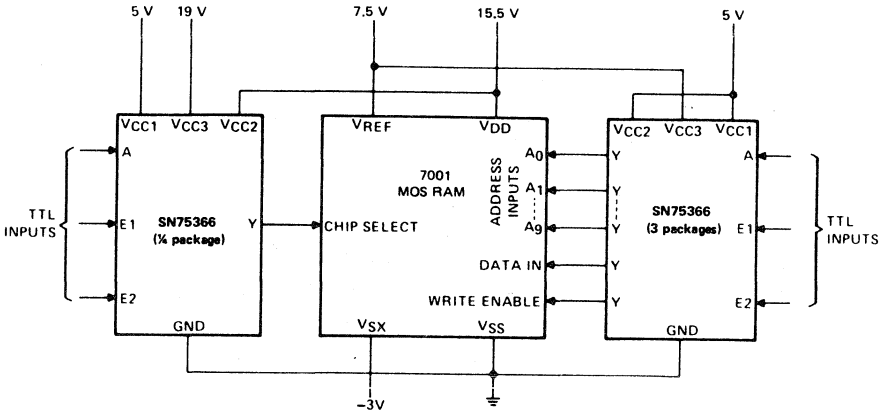
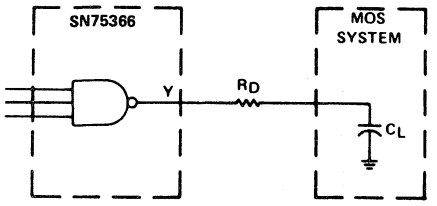


FIGURE 5—INTERCONNECTION OF SN75366 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM

7



NOTE: $R_D \approx 5$ to 20 Ω (optional).

FIGURE 6—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75366 APPLICATIONS

Applications using SN75366 devices interface between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figure 3, 4, and 5. The V_{CC3} supply pin of the SN75366 may be connected to the V_{CC2} pin as shown in Figure 3 or connected to a separate voltage higher than V_{CC2} as shown in Figures 4 and 5.

Figures 3, 4, and 5 show the use of the SN75366 over a wide range of V_{CC2} and V_{CC3} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} and V_{CC3} to 5 volts.

The fast switching speeds of many MOS drivers produce undesirable output transient overshoot because of load or wiring inductance. Often a small external series damping resistor is used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed.

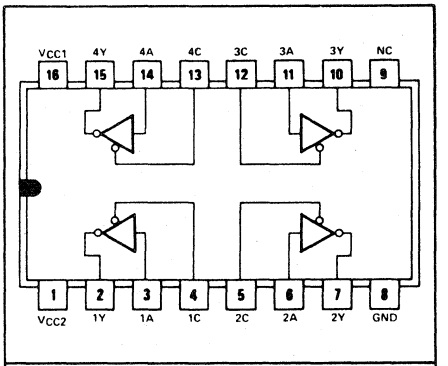
In most applications the internal damping resistor in the SN75366 eliminates the need for an external damping resistor. However, an external damping resistor may still be desired in some applications. See Figure 6.

TYPE SN75367
QUADRUPLE TTL-TO-MOS DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7712374, MAY 1976–REVISED APRIL 1977

- Quad Inverting TTL-to-MOS Drivers
- Three-State Outputs
- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- CMOS Applications
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Address and Enable/Disable Inputs for Each Driver
- V_{CC2} Variable Over Wide Range . . . V_{CC1} to 15 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$
Output is off (disabled) when C is high

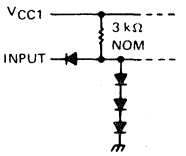
NC–No internal connection

description

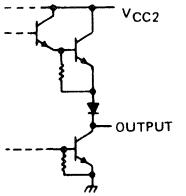
The SN75367 is a monolithic quadruple TTL-to-MOS driver and interface circuit with three-state outputs. Each driver output may be disabled to the high-impedance state by taking the C input high to allow multiple drivers to be connected to the same bus line for selective enable operation. The SN75367 is designed such that the output disable times are shorter than the output enable times to minimize the possibility that two outputs will attempt to take a common bus line to opposite logic levels. The SN75367 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 16 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75367 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC1} = 4.75 V, A inputs at 0.8 V,	V_{CC2} = 10.8 V, C inputs at 0.8 V,	I_O = −50 μA	V_{CC2}−1.6	V_{CC2}−1.2		V
				I_O = −10 mA	V_{CC2}−2.7	V_{CC2}−2.4		
V_{OL}	Low-level output voltage	V_{CC1} = 4.75 V, C inputs = 0.8 V,	V_{CC2} = 10.8 V, I_O = 10 mA	A inputs at 2 V,		0.3	0.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_I = 2.4 V					40	μA
I_{IL}	Low-level input current, A inputs	V_I = 0.4 V					−1.5	mA
	Low-level input current, C inputs						−2.2	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC1} = 5 V, A inputs at 0 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 12 V			−1.6	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC1} = 5 V, A inputs at 2.4 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 0 V			250	μA
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 15 V, No load			11	16	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high						0.6	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 0 V,	No load		17	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					24	37	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		23	32	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off	V_{CC1} = 5.25 V, A input at 0 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		22	32	mA
$I_{CC2(Z)}$	Supply current from V_{CC2}, all outputs off	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		26	39	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, and T_A = 25°C except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 250 pF, See Figures 1 thru 4	4	16	26	ns
t_{PHL}	Propagation delay time, high-to-low-level output		8	20	32	ns
t_{TLH}	Transition time, low-to-high-level output		3	15	23	ns
t_{THL}	Transition time, high-to-low-level output		6	21	32	ns
t_{PZH}	Output enable time to high level		9	21	31	ns
t_{PZL}	Output enable time to low level		10	30	42	ns
t_{PHZ}	Output disable time from high level		1	8	15	ns
t_{PLZ}	Output disable time from low level		6	15	27	ns

PARAMETER MEASUREMENT INFORMATION

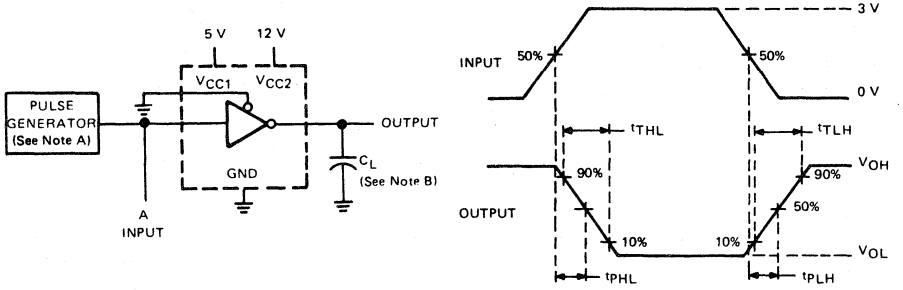


FIGURE 1–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}

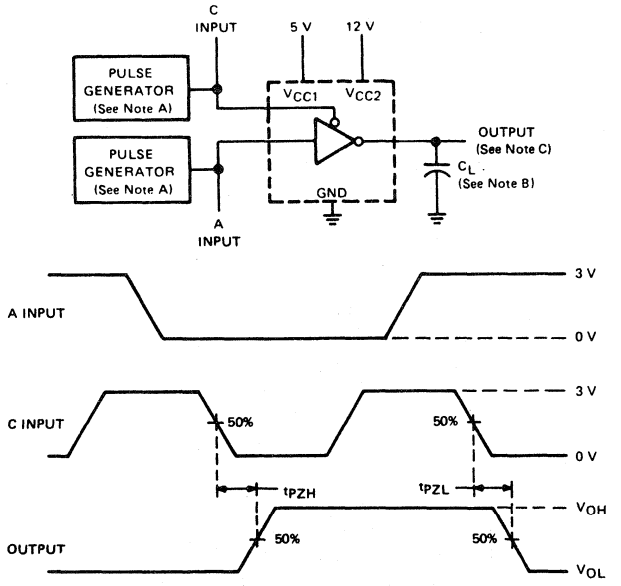


FIGURE 2–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PZH} AND t_{PZL}

NOTES: A. The pulse generators have the following characteristics: PRR = 1 MHz, (2 MHz for C input in Figure 2), $Z_{out} = 50\,\Omega$.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ ns, $R_{in} \geq 1\,M\Omega$.

PARAMETER MEASUREMENT INFORMATION

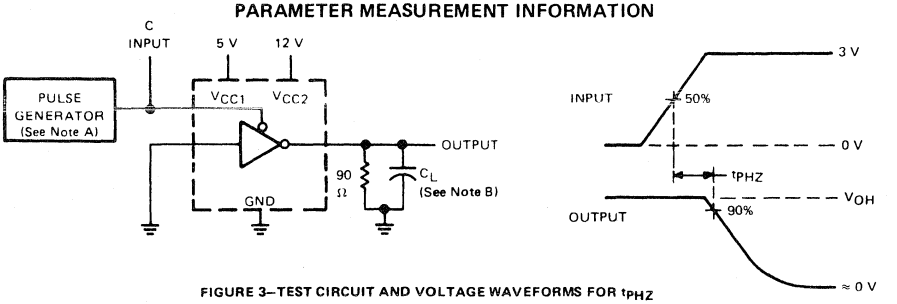


FIGURE 3–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PHZ}

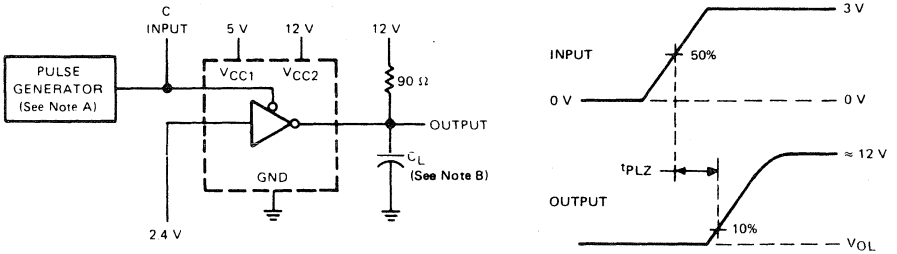


FIGURE 4–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLZ}

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

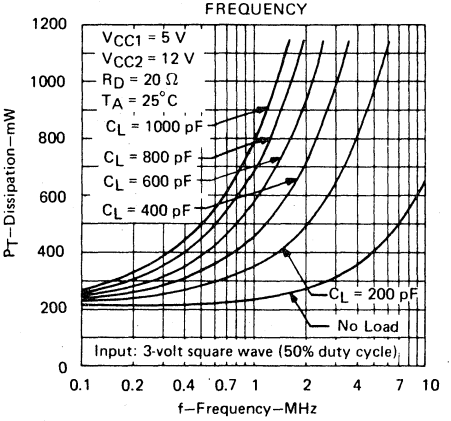


FIGURE 5

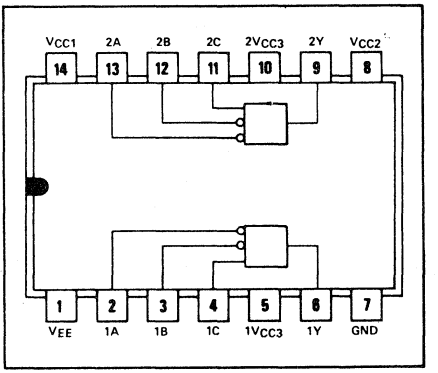
TYPE SN75368
DUAL ECL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712377, APRIL 1976–REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual ECL-to-MOS Drivers
- Dual ECL-to-TTL Drivers
- Versatile Interface Circuits for Use Between ECL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Inputs are Compatible with Series 10000 ECL and Other Similar ECL Families
- Single In-Phase and Dual Out-of-Phase Inputs per Driver
- Operates from Standard Bipolar and MOS Supply Voltages
- V_{CC2} Supply Voltage Variable over Wide Range . . . 4.75 V to 22 V
- Two Independent V_{CC3} Supply Voltage Pins Available
- V_{CC3} Pins Can Be Connected to V_{CC2} Pin in Some Applications
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



7

description

The SN75368 is a monolithic dual ECL-to-MOS driver and interface circuit. The device accepts standard input signals from Series SN10000 ECL and other similar ECL families and provides high-current and high-voltage output levels suitable for driving MOS and TTL circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103, TMS1103-1, TMS4030, TMS4062, and 7001.

FUNCTION TABLE

INPUTS				OUTPUT
DIFFERENTIAL	LOGIC LEVEL			Y
(More positive of A or B)–C	A	B	C	
H ($V_{ID} \geq 150$ mV)	L	H	L	L
	H	L	L	
	H	H	L	
? (-150 mV $< V_{ID} <$ 150 mV)	X	X	X	INDETERMINATE
L ($V_{ID} \leq -150$ mV)	L	L	H	H

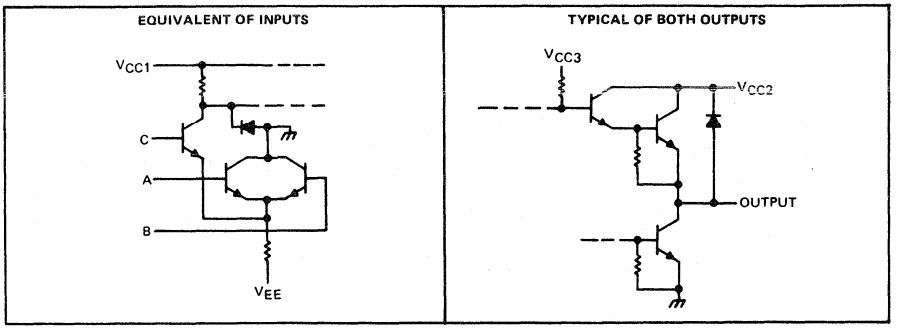
H = high level, L = low level, X = irrelevant
See additional function tables in Figure 6.

The SN75368 operates from the TTL V_{CC} supply, the ECL V_{EE} supply, and standard MOS supplies in most applications. This device has been optimized for operation with a V_{CC2} supply voltage from 12 volts to 20 volts with nominal V_{CC3} supply voltages from 3 to 4 volts higher than V_{CC2}. However, the SN75368 was designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the two V_{CC3} pins to the V_{CC2} pin. By connecting the V_{CC2} pin to the TTL 5-volt supply, the device can be used as an ECL-to-TTL converter.

The device has one in-phase and two out-of-phase ECL-compatible inputs per driver. By proper connections of the inputs, the SN75368 may be used three ways: positive-NOR gate, differential ECL line receiver, or noninverting gate. Some applications require one input per gate to be connected to an externally generated ECL reference voltage, V_{BB}.

The SN75368 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 to 22 V
Supply voltage range of $1V_{CC3}$ and $2V_{CC3}$ . . . . . −0.5 to 30 V
Supply voltage range of V_{EE} . . . . . −8 to 0.5 V
Negative voltage at V_{CC1}, V_{CC2}, $1V_{CC3}$, or $2V_{CC3}$ with respect to V_{EE} . . . . . −0.5 V
Input voltage range . . . . . −7V to 0.5 V
Negative voltage at any input with respect to V_{EE} . . . . . −1 V
Differential input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65° to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75368 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	22	V
Supply voltage, $1V_{CC3}$ and $2V_{CC3}$	V_{CC2}	24	28	V
Voltage difference between supply voltages: $1V_{CC3}-V_{CC2}$ and $2V_{CC3}-V_{CC2}$	0	4	10	V
Supply voltage, V_{EE}	−4.68	−5.2	−5.72	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels (see Note 3)

PARAMETER		B (Least Positive)	A (Most Positive)	UNIT
V_{IH}	High-level input voltage at any input	−1.5	−0.7	V
V_{IL}	Low-level input voltage at any input	V_{EE}	$V_{IH}-150$ mV	
V_{IDH}	High-level differential input voltage (see Note 3)	150		mV
V_{IDL}	Low-level differential input voltage (see Note 3)		−150	mV

NOTE 3: Differential input voltage is the voltage at the more-positive inverting input (A or B) with respect to the noninverting input (C) of the same gate.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, V_{EE}, and operating free-air temperature (unless otherwise noted)

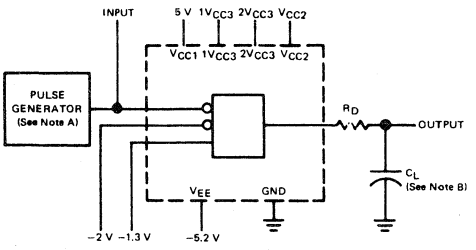
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC3} = V_{CC2} + 3$ V, $V_{IDL} = -150$ mV, $I_{OH} = -100$ μA	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2} + 3$ V, $V_{IDL} = -150$ mV, $I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		
		$V_{CC3} = V_{CC2}$, $V_{IDL} = -150$ mV, $I_{OH} = -50$ μA	$V_{CC2}-1$	$V_{CC2}-0.7$		
		$V_{CC3} = V_{CC2}$, $V_{IDL} = -150$ mV, $I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage	$V_{IDH} = 150$ mV, $I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC3} = 10$ V to 28 V, $V_{IDH} = 150$ mV, $I_{OL} = 30$ mA		0.2	0.4	
V_{OK}	Output clamp voltage	$V_{ID} = -500$ mV, $I_{OH} = 20$ mA			$V_{CC2}+1.5$	V
I_{IH}	High-level input current	$V_{EE} = -5.72$ V, $V_I = -0.7$ V All other inputs at -5.72 V		300	800	μA
I_{IL}	Low-level input current	$V_I = -2$ V, All other inputs at -0.7 V			-10	μA
		$V_{EE} = -5.72$ V, $V_I = -5.72$ V, All other inputs at -0.7 V			-100	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V $V_{CC3} = 28$ V, $V_{EE} = -5.72$ V, All A and B inputs at -2 V, Both C inputs at -0.7 V, No load		21	38	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high			-2	+0.25 -3.6	
$I_{CC3(H)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs high			1	1.8	
$I_{EE(H)}$	Supply current from V_{EE}, all outputs high			-21	-38	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V, $V_{CC3} = 28$ V, $V_{EE} = -5.72$ V, All A and B inputs at -0.7 V, Both C inputs at -2 V, No load		13	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low			0.5	1	
$I_{CC3(L)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs low			4	8	
$I_{EE(L)}$	Supply current from V_{EE}, all outputs low			-21	-38	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V, $V_{CC3} = 22$ V, $V_{EE} = -5.72$ V, All A and B inputs at -2 V, Both C inputs at -0.7 V, No load			0.25	mA
$I_{CC3(H)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs high				0.25	
$I_{CC2(S)}$	Supply current from V_{CC2}, stand-by condition	$V_{CC1} = 0$ V, $V_{CC2} = 22$ V, $V_{CC3} = 22$ V, $V_{EE} = 0$ V, All A and B inputs at -0.7 V, Both C inputs at -2 V, No load			0.25	mA
$I_{CC3(S)}$	Supply current from $1V_{CC3}$/ $2V_{CC3}$, stand-by condition				0.25	

†All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $V_{EE} = -5.2$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

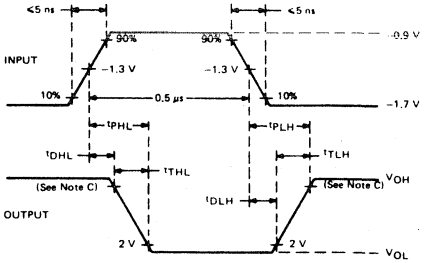
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{EE} = -5.2$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC3} = 24$ V			$V_{CC3} = 20$ V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10\ \Omega$, See Figure 1	4	12	22	5	13	23	ns
t_{DHL}	Delay time, high-to-low-level output		5	13	23	5	15	24	ns
t_{TLH}	Transition time, low-to-high-level output		7	19	32	8	20	33	ns
t_{THL}	Transition time, high-to-low-level output		8	20	33	6	18	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		11	31	54	13	33	56	ns
t_{PHL}	Propagation delay time, high-to-low-level output		13	33	56	11	33	57	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The high-level reference point is 17 V when $V_{CC3} = V_{CC2} = 20$ V, and is 18 V when $V_{CC3} = V_{CC2} + 4$ V = 24 V.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

7

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

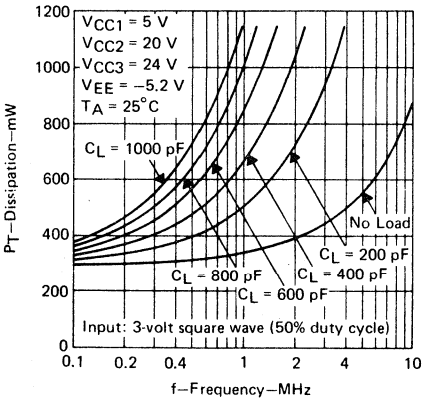


FIGURE 2

TYPICAL APPLICATION DATA

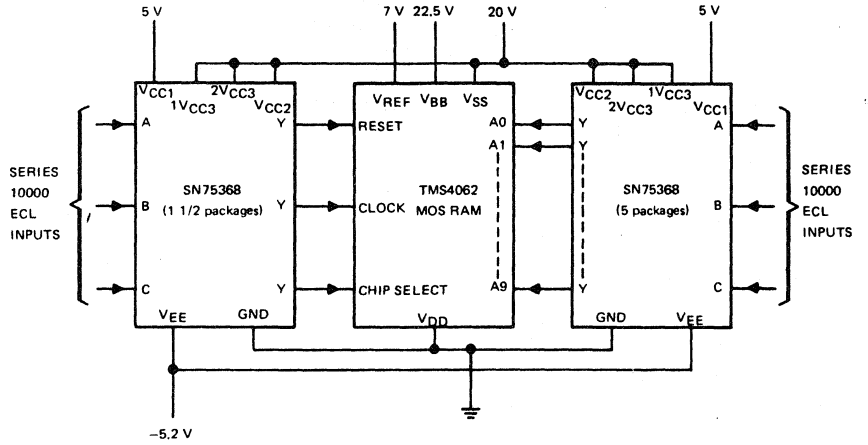


FIGURE 3—INTERCONNECTION OF SN75368 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

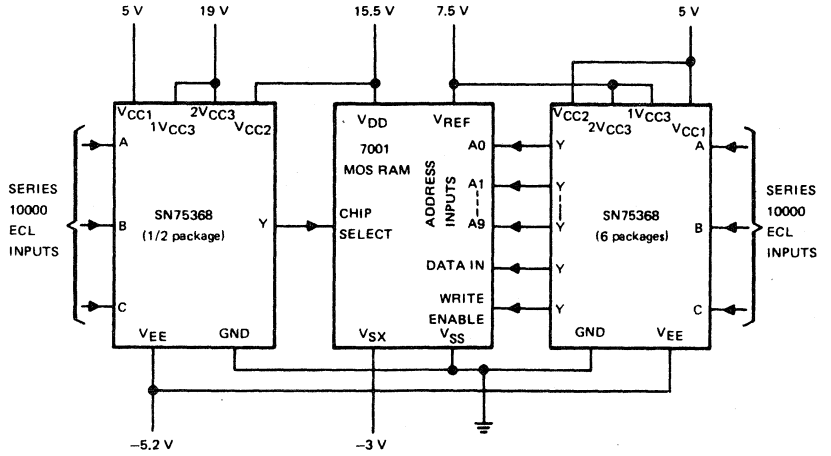
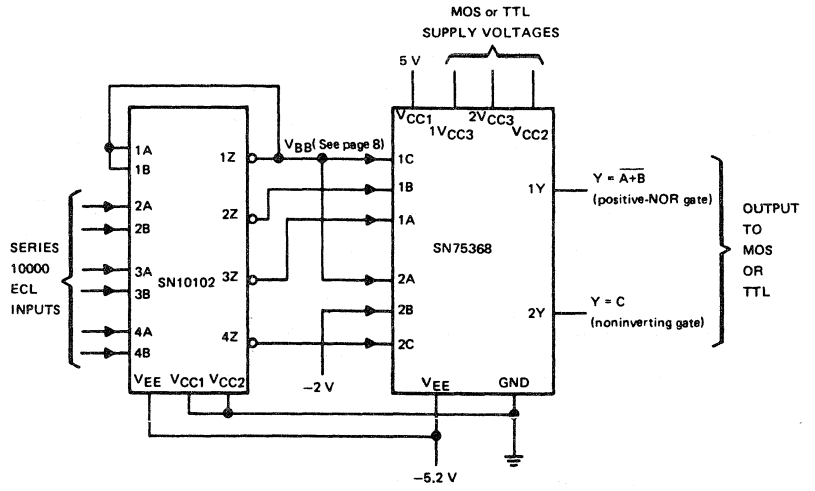
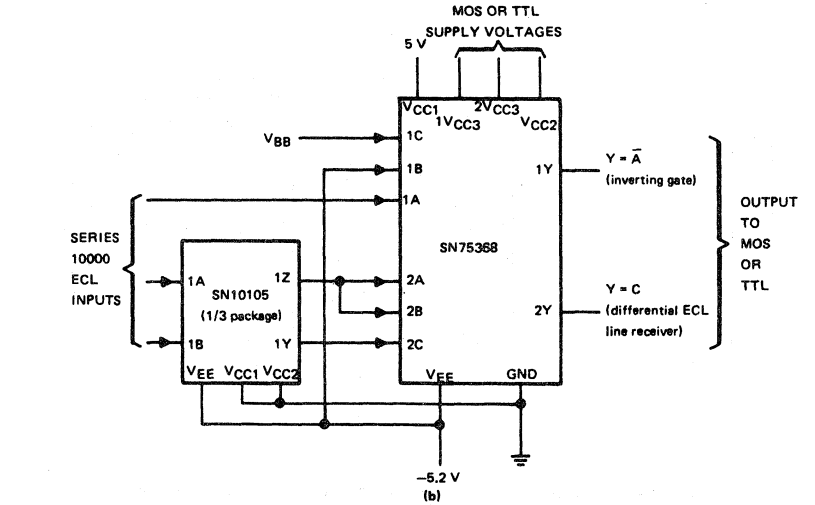


FIGURE 4—INTERCONNECTION OF SN75368 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM

TYPICAL APPLICATION DATA



(a)



(b)

FIGURE 5–REPRESENTATIVE METHODS OF INTERCONNECTING SN75368 DEVICES WITH SN10000 SERIES ECL

TYPICAL APPLICATION DATA

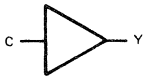
positive-NOR gate

$Y = \overline{A+B}$

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

noninverting gate

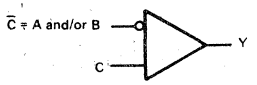


Y = C

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

differential ECL line receiver



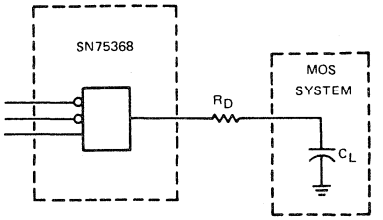
Y = C

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

H = high level, L = low level, X = irrelavant
V_{BB} = Reference Supply voltage for SN10000 Series ECL.

FIGURE 6–FUNCTIONS



NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional).

FIGURE 7–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75368 APPLICATIONS

Applications using the SN75368 as an interface device between series SN10000 ECL inputs and the address, control, and timing inputs for two types of MOS RAMS are shown in Figures 3 and 4. The $1V_{CC3}$ and $2V_{CC3}$ supply pins of the SN75368 may be connected to the V_{CC2} pin as shown in Figure 3 or connected to a separate voltage higher than V_{CC2} as shown in Figure 4. If desired, the $1V_{CC3}$ pin may be connected to a voltage different from the $2V_{CC3}$ pin.

Figures 3 and 4 show the use of the SN75368 over a wide range of V_{CC2}, $1V_{CC3}$, and $2V_{CC3}$ supply voltages. This device may even be used as ECL-to-TTL-level converters, if desired, by connecting V_{CC2}, $1V_{CC3}$, and $2V_{CC3}$ to 5 volts.

The one in-phase (C) and two out-of phase (A and B) inputs per driver permit much flexibility when using the SN75368. By connecting the correct input to an externally generated V_{BB} (ECL reference supply voltage) positive-NOR gate, inverting gate, or noninverting gate functions may be obtained as shown in Figure 5. By driving the correct inputs differentially as in Figure 5 (b), these devices may be used as differential ECL line receivers and no V_{BB} reference voltage is required. The V_{BB} reference voltage may be generated as in Figure 5 (a) by connecting the output of an ECL gate to its out-of-phase input, by using the V_{BB} pin of certain ECL devices such as SN10115, or by other methods. An unused out-of-phase input may be connected low or connected to the other out-of-phase input of the same gate in many applications. Function tables for many of these applications are shown in Figure 6.

The fast switching speeds of the SN75368 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the overall load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 7.

7

TYPE SN75369
DUAL MOS DRIVER

BULLETIN NO. DL-S 7712380, APRIL 1976—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Inverting MOS Driver
- Low Standby Power Dissipation
- Versatile Interface Circuit for Use between TTL Levels and Level-Shifted High-Current, High-Voltage Systems
- Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source
- Designed to Be Functionally Interchangeable with National DS0026
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs and MOS Shift Registers
- V_{CC} Supply Voltage Variable over Wide Range to 22 Volts Maximum with Respect to V_{EE}
- Operates from Standard Bipolar and/or MOS Supply Voltage
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation

description

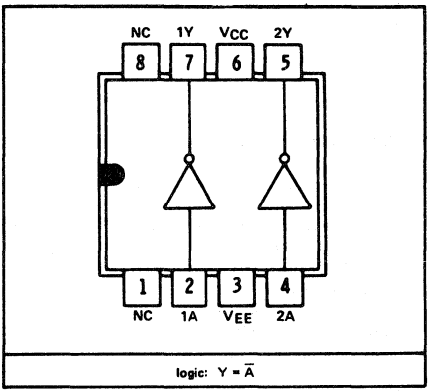
The SN75369 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The SN75369 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC} supply voltage from 12 volts to 20 volts positive with respect to V_{EE}. However, it is designed so as to be usable over a wide range of V_{CC}.

Inputs of the SN75369 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12 volts to −15 volts with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

The SN75369 is characterized for operation from 0°C to 70°C.

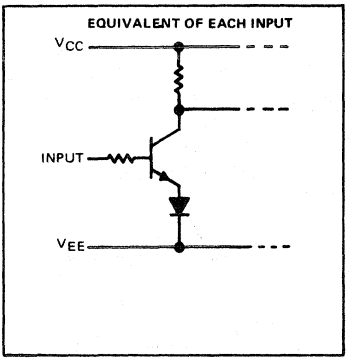
JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)

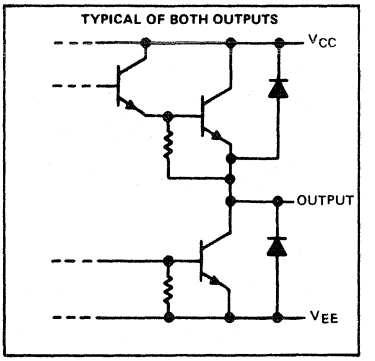


NC - No internal connection

7

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1)	−0.5 V to 22 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the JG package, SN75369 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	20	22	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.5		4.5	V
V_{IL}	Low-level input voltage			0.5	V
I_{IH}	High-level input current	8		20	mA
I_{IL}	Low-level input current			27	mA

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.5 V,	I_{OH} = −50 μA	V_{CC}−1	V_{CC}−0.7		V
		I_{IL} = 0.7 mA,	I_{OH} = −50 μA				
		V_{IL} = 0.5 V,	I_{OH} = −10 mA	V_{CC}−2.3	V_{CC}−1.8		
		I_{IL} = 0.7 mA,	I_{OH} = −10 mA				
V_{OL}	Low-level output voltage	V_{IH} = 2.5 V,	I_{OL} = 10 mA		0.15	0.3	V
		I_{IH} = 8 mA,	I_{OL} = 10 mA				
		V_{CC} = 10 V to 22 V,	V_{IH} = 2.5 V, I_{OL} = 30 mA		0.2	0.4	
		V_{CC} = 10 V to 22 V,	I_{IH} = 8 mA, I_{OL} = 30 mA				
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC}+1.5	V
V_I	Input voltage	I_I = 20 mA			3.7	5	V
		I_I = 8 mA			2.4	3	
		I_I = 0.7 mA			0.4	0.6	
I_I	Input current	V_I = 4.5 V			27	45	mA
		V_I = 2.5 V			9	15	
		V_I = 0.5 V				1.5	
$I_{CC(H)}$	Supply current from V_{CC}, both outputs high	V_{CC} = 22 V, Both inputs at 0 V,	No load			0.5	mA
$I_{CC(L)}$	Supply current from V_{CC}, both outputs low	V_{CC} = 22 V, Both inputs at 3 V,	No load		7	12	mA

†All typical values are at V_{CC} = 20 V and T_A = 25°C.

NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

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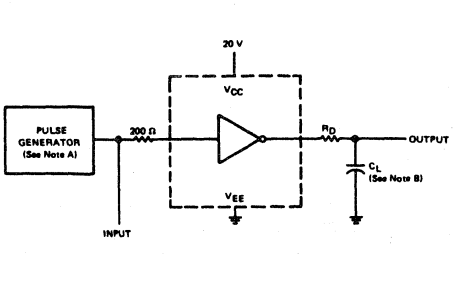
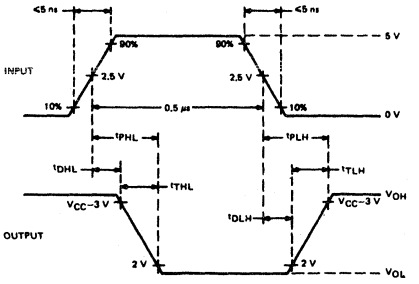
switching characteristics, V_{CC} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1	8	16	24	ns
t_{DHL}	Delay time, high-to-low-level output		4	11	20	ns
t_{TLH}	Transition time, low-to-high-level output		8	18	30	ns
t_{THL}	Transition time, high-to-low-level output		6	16	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		16	35	54	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	28	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

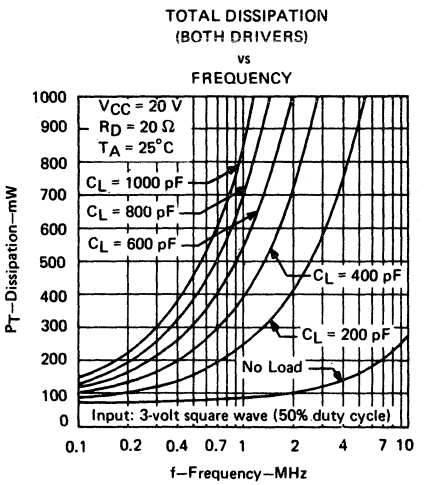


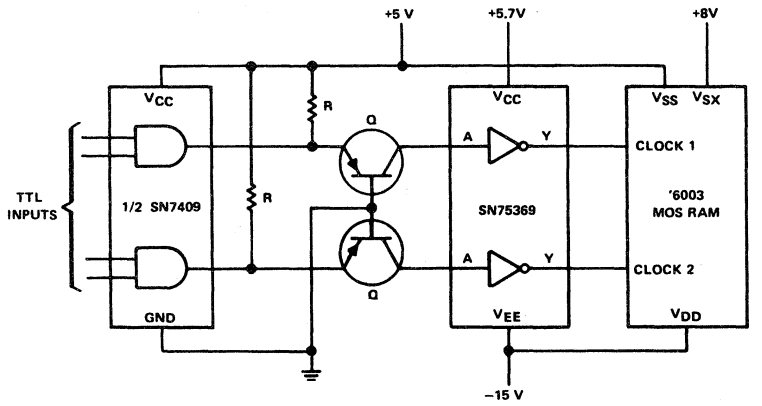
FIGURE 2

TYPICAL APPLICATION DATA

Applications of the SN75369 used as an interface device in systems converting TTL signals to negative-polarity MOS clock signals are shown in Figures 3 and 4. In both applications the SN75369 V_{EE} pin is connected to a negative MOS supply voltage. Figure 3 and 4 show the use of the SN75369 over a wide range of V_{CC} supply voltages. The device may even be used as a TTL level driver, if desired, by connecting V_{CC} to 5 volts.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the SN75369, which are referenced to the V_{EE} terminal. A p-n-p transistor current source is used to level shift in Figure 3. Resistor R sets the current and an open-collector TTL gate is used to switch the p-n-p transistor. Figure 4 shows capacitive coupling being used to level shift. The SN7437 TTL buffer gate is used as a voltage source driver with pull-up resistor R providing additional high-level drive. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

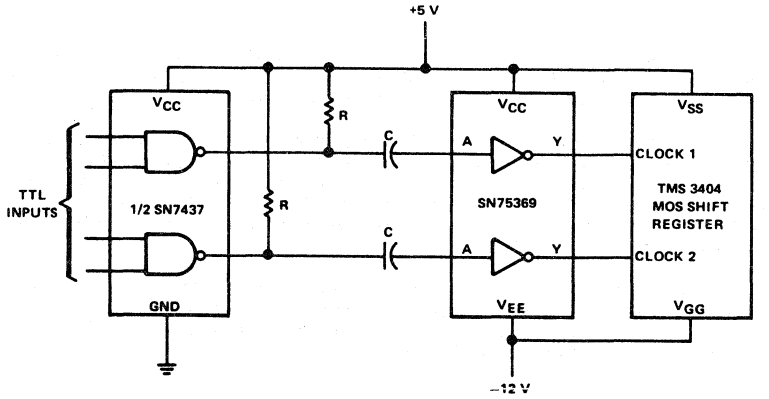
The fast switching speeds of the SN75369 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 5.



NOTES: A. R ≈ 350 Ω to 500 Ω.
B. Q is 2N3829 or equivalent.

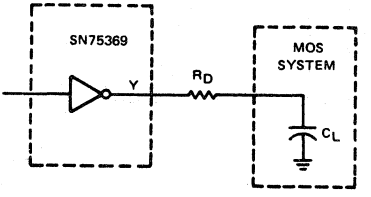
FIGURE 3—MOS RAM CLOCK DRIVER SYSTEM WITH P-N-P TRANSISTOR CURRENT SOURCE USED TO SHIFT LEVELS TO INPUTS OF SN75369

TYPICAL APPLICATION DATA



NOTE A: R ≈ 100 Ω to 250 Ω.

FIGURE 4–MOS SHIFT REGISTER CLOCK DRIVER SYSTEM WITH CAPACITIVE COUPLING USED TO SHIFT LEVELS TO INPUTS OF SN75369



NOTE: R_D ≈ 10 Ω to 30 Ω (optional)

FIGURE 5–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75369 APPLICATIONS

TYPE SN75370
DUAL-CHANNEL INTERFACE TO MOS MEMORIES

BULLETIN NO. DL-S 7712059, SEPTEMBER 1973 — REVISED APRIL 1977

DUAL READ/WRITE AMPLIFIER FOR INTERFACING BETWEEN TTL AND TMS4062-TYPE MOS RANDOM-ACCESS MEMORY (RAM)

performance features

- Node Terminals Connect Directly to I/O Terminals of TMS4062 (AMS6002) and Similar MOS RAMs
- In Write Mode, Write Driver Provides Complementary High-Voltage Outputs at Node Terminals
- In Read Mode, Read Amplifier Responds to Small Differential-Input Current in Node Terminals

ease of design features

- TTL and DTL Compatible Diode-Clamped Inputs
- TTL and DTL Compatible Data Outputs
- 50-mA Data Output Sink-Current Capability
- Data Outputs May Be Wire-AND Connected
- Operates Over Wide Range of Supply Voltages
- Minimizes or Eliminates External Components

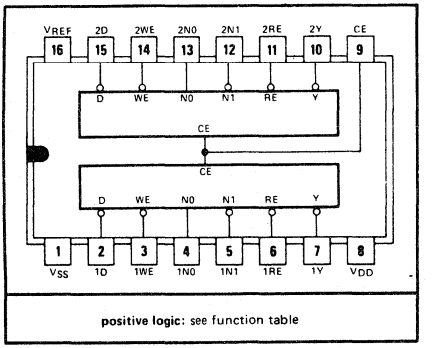
description

The SN75370 is a monolithic integrated circuit read/write amplifier that is designed to interface the Input/Output (I/O) terminals of the TMS4062 (AMS6002) and similar type MOS RAMs with TTL.

The device contains two separate channels. Each channel consists of a write driver and a read amplifier, which are common at the input/output node (N) terminals. These terminals are outputs for the write driver and inputs for the read amplifier. In the write mode, the write driver circuit is designed to write MOS-level binary information into the MOS RAM under control of TTL inputs. In the read mode, the read amplifier is designed to read MOS-level binary information from the MOS RAM and convert it to TTL levels at the data output. This is controlled by TTL inputs also.

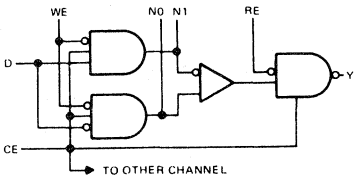
Data outputs are constructed so that they may be wire-AND connected to other outputs and/or be connected to an external pull-up resistor, if desired. The device has a chip-enable input common to both channels which can be used to enable the entire device. Internal voltage regulators permit circuit operation over a wide range of supply voltages.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table

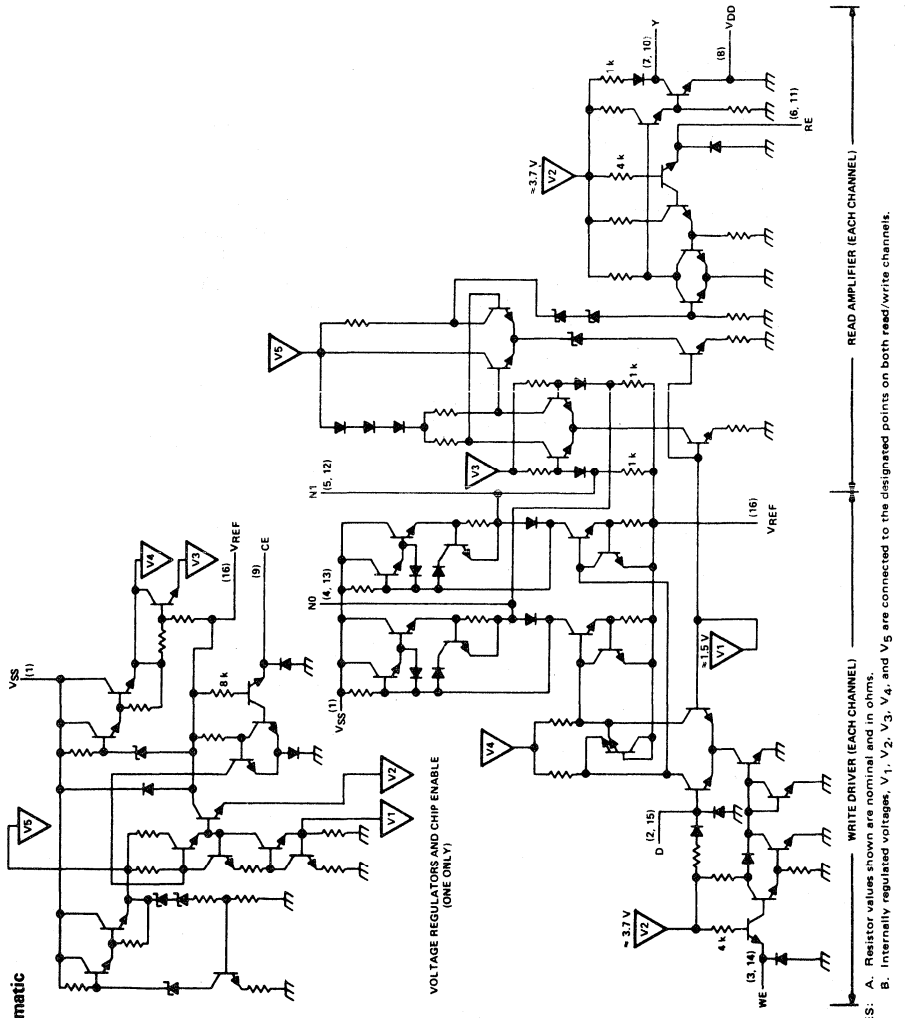
functional block diagram (each channel)



FUNCTION TABLE

MODE	VOLTAGE INPUTS				VOLTAGE OUTPUTS		DIFFERENTIAL CURRENT INPUT	OUTPUT
	CE	WE	RE	D	N0	N1	N1–N0	Y
Write 0	H	L	H	L	H	L	X	H
Write 1	H	L	H	H	L	H	X	H
Read 0	H	H	L	X	L	L	L	L
Read 1	H	H	L	X	L	L	H	H
Standby	H	H	H	X	L	L	X	H
Disabled	L	X	X	X	L	L	X	Off

H = high level (voltage or current), L = low level (voltage or current), X = irrelevant
Input levels at CE, WE, RE, and D, and output levels at Y are TTL-compatible.
Voltage output levels at N fall between V_{SS} and V_{REF}.



NOTES: A. Resistor values shown are nominal and in ohms.
B. Internally regulated voltages, V_1, V_2, V_3, V_4, and V_5 are connected to the designated points on both read/write channels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{SS} (see Note 1)	−0.5 V to 25 V
Supply voltage range, V_{REF}	−0.5 V to 15 V
Voltage-difference range between supply voltages, $V_{SS}-V_{REF}$	−0.5 V to 20 V
Input voltage at CE, WE, RE, or D	5.5 V
Output voltage at Y	7 V
Continuous output current into Y	50 mA
Continuous current into any node terminal	±40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) : J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the V_{DD} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75370 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	17	20	22	V
Supply voltage, V_{REF}	4.5	7	10	V
Voltage difference between supply voltages, $V_{SS}-V_{REF}$	8	13	16	V
Operating free-air temperature, T_A	0		70	°C

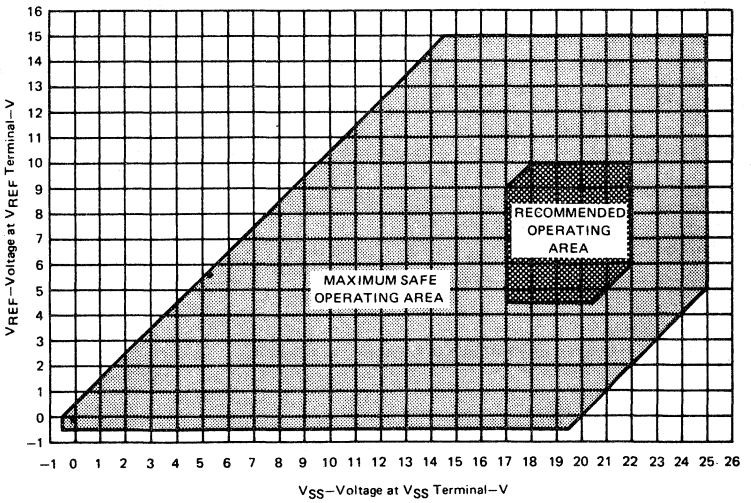


FIGURE 1—MAXIMUM SAFE OPERATING AREA AND RECOMMENDED OPERATING AREA

definition of input logic levels

PARAMETER		B (LEAST POSITIVE)	A (MOST POSITIVE)	UNIT
V_{IH}	High-level input voltage at CE, WE, RE, or D	2		V
V_{IL}	Low-level input voltage at CE, WE, RE, or D		0.8	V
I_{IDH}	High-level differential input current in node terminals (see Note 3)	50		μA
I_{IDL}	Low-level differential input current in node terminals (see Note 3)		−50	μA

NOTE 3: $I_{ID} = I_{N1} - I_{N0}$ with current into a terminal being a positive value.

electrical characteristics over recommended ranges of V_{SS}, V_{REF}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at CE, WE, RE, or D	2	I_I = −12 mA				−1.5	V
V_{ONH}	High-level output voltage at node terminals	3	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{NH} = 0		V_{SS}−2	V_{SS}−1.6		V
			V_{IH} = 2 V, V_{IL} = 0.8 V, I_{NH} = −40 mA		V_{SS}−3	V_{SS}−2		
V_{ONL}	Low-level output voltage at node terminals	3	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{NL} = 0		V_{REF}	V_{REF}+0.2	V_{REF}+1	V
			V_{IH} = 2 V, V_{IL} = 0.8 V, I_{NL} = 20 mA		V_{REF}	V_{REF}+1.2	V_{REF}+2	
I_{OH}	High-level output current into output Y	4	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{IDH} = 50 μA, V_{OH} = 5.5 V				100	μA
V_{OH}	High-level output voltage at output Y	4	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{IDH} = 50 μA, I_{OH} = −200 μA		2.2	2.8	4.5	V
V_{OL}	Low-level output voltage at output Y	4	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{IDL} = −50 μA, I_{OL} = 50 mA			0.25	0.4	V
I_I	Input current at maximum input voltage into CE, WE, RE, or D	5	V_I = 5.5 V				1	mA
I_{IH}	High-level input current into CE, WE, or RE	5	V_I = 2.4 V				40	μA
I_{IH}	High-level input current into D	5	V_I = 2.4 V			−150	+80 −600	μA
I_{IL}	Low-level input current into CE, WE, RE, or D	2	V_I = 0.4 V			−0.7	−1.6	mA
r_N	Resistance from any node to V_{REF}	6	V_{SS} open, V_{REF} = 0, I_N = 500 μA, T_A = 25°C		0.7	1‡	1.3	kΩ
I_{OS}	Short-circuit output current into D	7	V_O = 0 V	CE at 2 V		−3.2	−4.5	mA
				CE at 0.8 V			−1	

See next page for supply current and dissipation.

†All typical values, except for r_N and $I_{REF(D, O)}$, are at V_{SS} = 20 V, V_{REF} = 7 V, T_A = 25°C.
‡Typical value of r_N is with V_{SS} open, V_{REF} = 0 V, T_A = 25°C.

supply current and dissipation over operating free-air temperature range (unless otherwise noted)

PARAMETER		MODE	TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{SS(D)}$	Current from V_{SS}	Disabled	8	V_{SS} = 20 V, V_{REF} = 7 V		27	35	mA
$I_{REF(D)}$	Current from V_{REF}					−20	−25	mA
P_D	Dissipation					410	500	mW
$I_{SS(SB)}$	Current from V_{SS}	Standby	8	V_{SS} = 20 V, V_{REF} = 7 V		31	39	mA
$I_{REF(SB)}$	Current from V_{REF}					−12	−18	mA
P_{SB}	Dissipation					560	690	mW
$I_{SS(R1)}$	Current from V_{SS}	Read-1	8	V_{SS} = 20 V, V_{REF} = 7 V, I_{N1} = 100 μA		31	39	mA
$I_{REF(R1)}$	Current from V_{REF}					−12	−18	mA
P_{R1}	Dissipation					540	690	mW
$I_{SS(R0)}$	Current from V_{SS}	Read-0	8	V_{SS} = 20 V, V_{REF} = 7 V, I_{N0} = 100 μA		31	39	mA
$I_{REF(R0)}$	Current from V_{REF}					4	10	mA
P_{R0}	Dissipation					640	790	mW
$I_{SS(W)}$	Current from V_{SS}	Write	8	V_{SS} = 20 V, V_{REF} = 7 V, See Note 4		53	66	mA
$I_{REF(W)}$	Current from V_{REF}					−23	−31	mA
P_W	Dissipation					910	1100	mW
$I_{REF(D, O)}$	Current from V_{REF}	Disabled, V_{SS}-open	8	V_{SS} open, V_{REF} = 10 V		2§	5	mA

†All typical values, except for r_N and $I_{REF(D,O)}$, are at V_{SS} = 20 V, V_{REF} = 7 V, T_A = 25°C.
§Typical value of $I_{REF(D,O)}$ is with V_{SS} open, V_{REF} = 7 V, T_A = 25°C.
NOTE 4: Duty cycle in the write mode must be low enough to maintain the average dissipation within the continuous dissipation rated limit when averaged over short intervals.

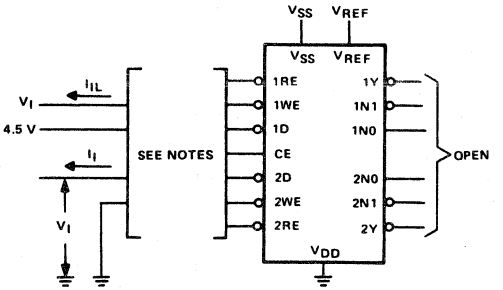
switching characteristics, V_{SS} = 20 V, V_{REF} = 7 V, $C_{I/O}$ = 40 pF, C_L = 15 pF, R_L = 400 Ω, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	WE	N	10			52	80	ns
t_{PHL}						31	47	
t_{PLH}	D	N	11			44	70	ns
t_{PHL}						30	45	
t_{PLH}	CE	N	12			60	95	ns
t_{PHL}						43	65	
t_{PLH}	RE	Y	13	I_{ID} = −100 μA		13	20	ns
t_{PHL}						19	28	
t_{PLH}	CE	Y	14	I_{ID} = −100 μA		25	38	ns
t_{PHL}						32	48	
t_{PLH}	N0	Y	15			25	40	ns
t_{PHL}						25	40	
t_{PLH}	N1	Y	16			25	40	ns
t_{PHL}						25	40	
t_{PLH}	WE	Y	17	I_{N1} = 100 μA		135	190	ns
t_{PHL}				I_{N0} = 100 μA		125	190	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

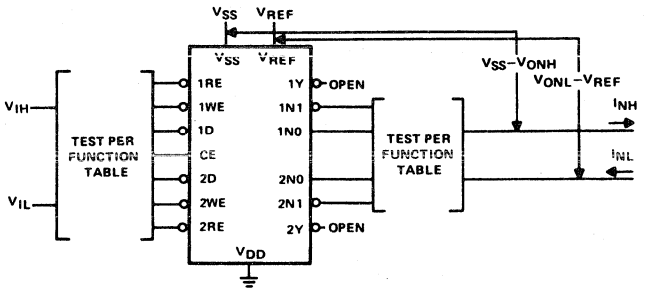
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



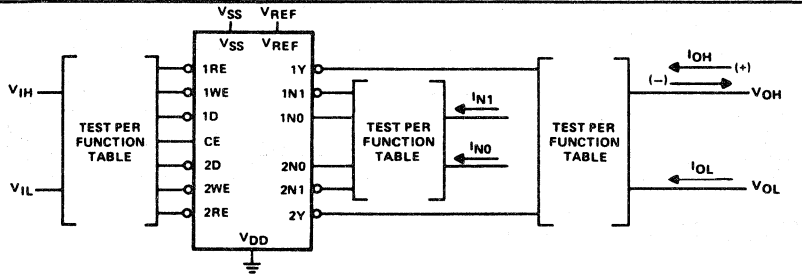
NOTES: A. WE, RE, and D inputs are tested for two conditions of CE: CE at 4.5 V and CE at 0 V.
B. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 20%.

FIGURE 2–V_I and I_{IL}



NOTE A: When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 20%.

FIGURE 3–V_{IH}, V_{IL}, V_{ONH}, and V_{ONL}



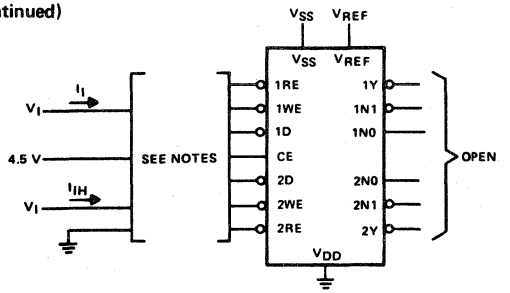
NOTES: A. I/O terminals are used as inputs.
B. For testing purposes: $I_{IDH} = I_{N1}$ with $I_{N0} = 0$. (Current into I_{N1} terminal only.)
$-I_{IDL} = I_{N0}$ with $I_{N1} = 0$. (Current into I_{N0} terminal only.)
C. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 20%.

FIGURE 4–V_{IH}, V_{IL}, I_{IDH}, I_{IDL}, V_{OH}, V_{OL}, I_{OH}

†*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.*

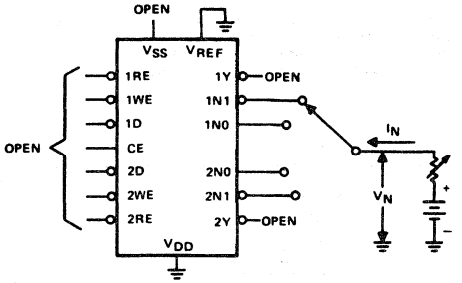
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. WE, RE, and D inputs are tested for two conditions of CE: CE at 4.5 V and CE at 0 V.
B. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 20%.

FIGURE 5–I_I and I_{IH}



NOTE A: Resistance r_N is calculated using the equation: $r_N = \frac{V_N}{I_N}$.

FIGURE 6–r_N

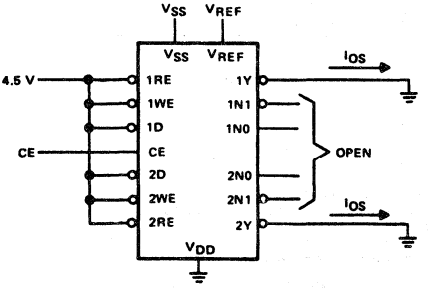


FIGURE 7–I_{OS}

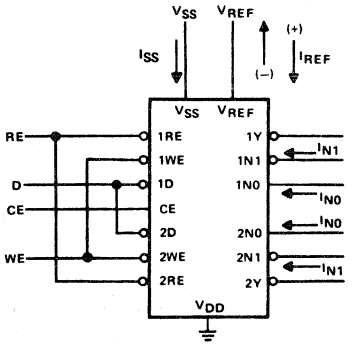
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

TEST TABLE

MODE	CE	WE	RE	D
Disabled	0 V	0 V	0 V	4.5 V
Standby	4.5 V	4.5 V	4.5 V	4.5 V
Read-1	4.5 V	4.5 V	0 V	4.5 V
Read-0	4.5 V	4.5 V	0 V	0 V
Write	4.5 V	0 V	4.5 V	4.5 V
Disabled, V_{SS}-open	0 V	0 V	0 V	0 V

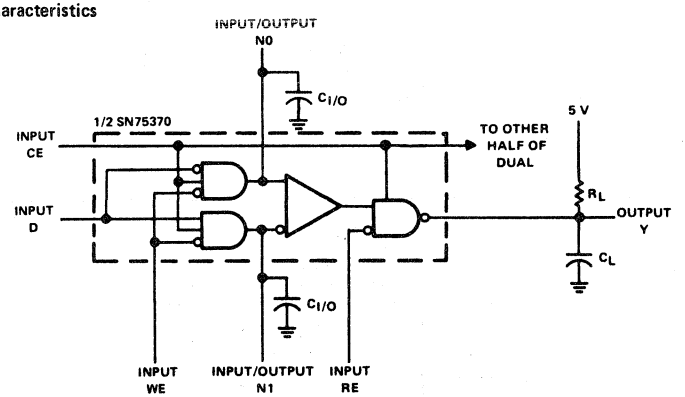


NOTES: A. I_{SS} and I_{REF} are measured simultaneously with both halves of circuit biased identically.
B. All node terminals are open except as noted otherwise in test conditions.
C. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 20%.
D. Dissipation is calculated using the equation $P = V_{SS} \cdot I_{SS} + V_{REF} \cdot I_{REF}$.

FIGURE 8–I_{SS}, I_{REF}, and P

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics

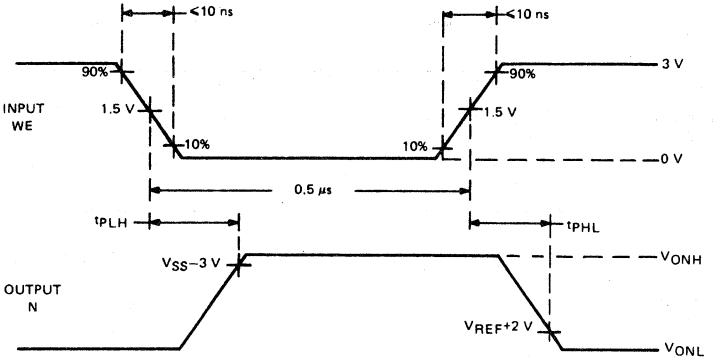


NOTES: A. Refer to this figure and notes for all switching tests.
B. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
C. C_L and $C_{I/O}$ include probe and jig capacitance.
D. Input conditions for channel not under test: WE and RE at 2.4 V, D at 0.4 V.
E. N terminals are connected only to $C_{I/O}$ unless otherwise noted.

FIGURE 9–SWITCHING TEST CIRCUIT

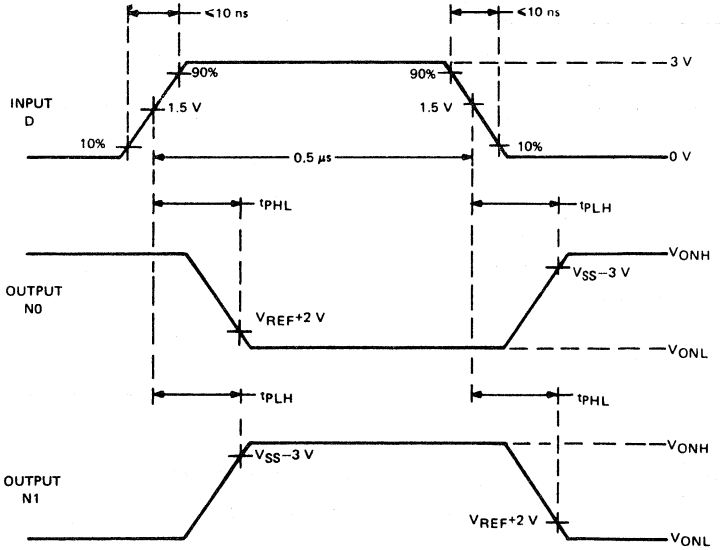
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Output N0 is tested with D at 0.4 V and output N1 is tested with D at 2.4 V.
C. Input conditions for other inputs of channel under test: CE at 2.4 V, RE at 2.4 V.

FIGURE 10–VOLTAGE WAVEFORMS, WE TO N



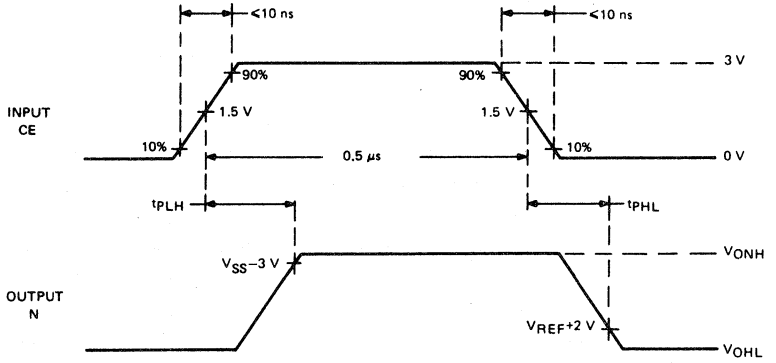
NOTES: A. See Figure 9.
B. Input conditions for other inputs of channel under test: CE at 2.4 V, WE at 0.4 V, RE at 2.4 V.

FIGURE 11–VOLTAGE WAVEFORMS, D TO N

7

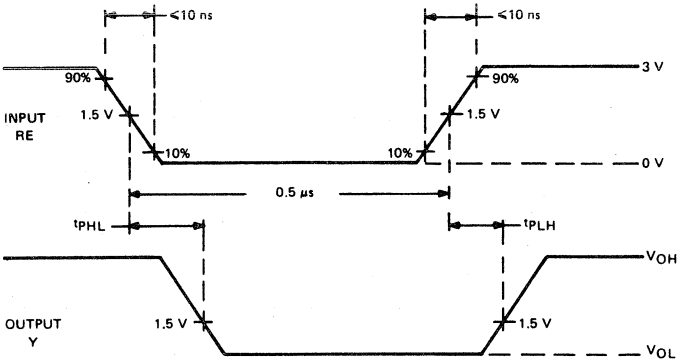
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Output N0 is tested with D at 0.4 V and output N1 is tested with D at 2.4 V.
C. Input conditions for all other inputs of channel under test: WE at 0.4 V, RE at 2.4 V.

FIGURE 12–VOLTAGE WAVEFORMS, CE TO N

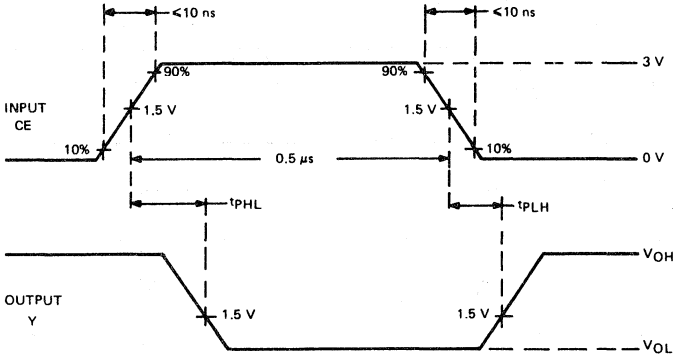


NOTES: A. See Figure 9.
B. Input conditions for all other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, D at 0.4 V.
C. I_{NO} = 100 μA.

FIGURE 13–VOLTAGE WAVEFORMS, RE TO Y

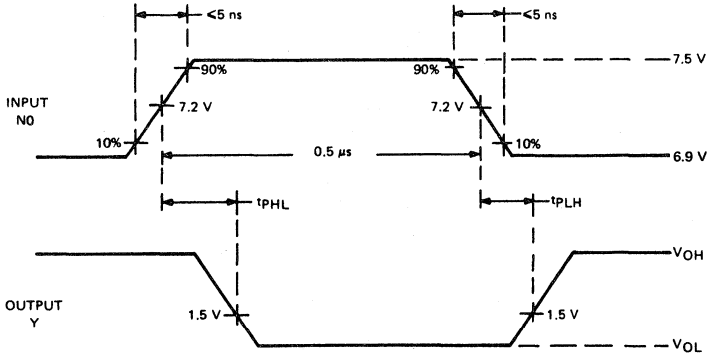
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Input conditons for all other inputs of channel under test: WE at 2.4 V, RE at 0.4 V, D at 0.4 V.
C. I_{NO} = 100 μA.

FIGURE 14–VOLTAGE WAVEFORMS, CE TO Y

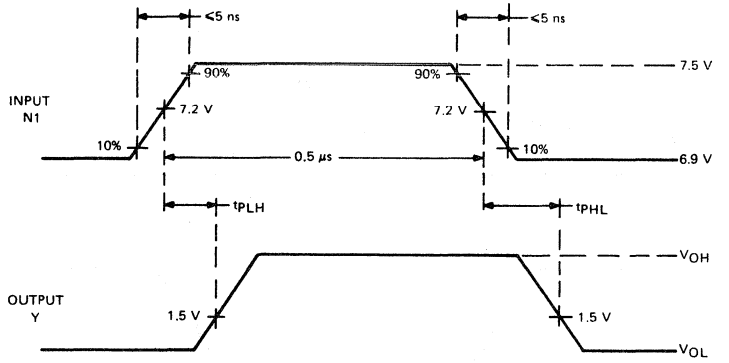


NOTES: A. See Figure 9.
B. Input conditions for all other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, RE at 0.4 V, D at 2.4 V.

FIGURE 15–VOLTAGE WAVEFORMS, N0 TO Y

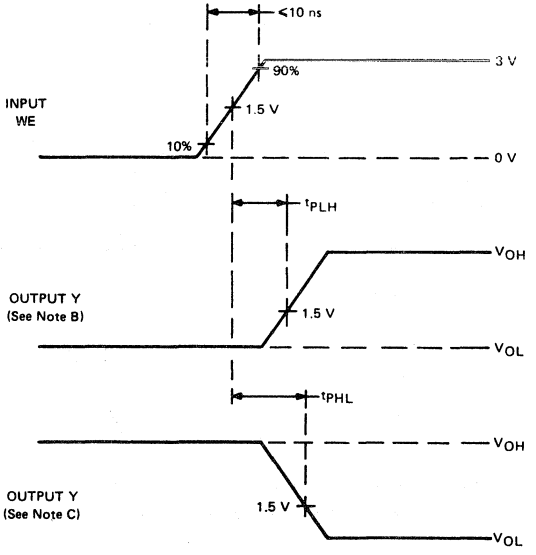
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Input conditions for other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, RE at 0.4 V, D at 2.4 V.

FIGURE 16–VOLTAGE WAVEFORMS, N1 TO Y



NOTES: A. See Figure 9.
B. t_{PLH} is tested with I_{N1} = 100 µA, D at 0.4 V, CE at 2.4 V, RE at 0.4 V.
C. t_{PHL} is tested with I_{N0} = 100 µA, D at 2.4 V, CE at 2.4 V, RE at 0.4 V.
D. Duty cycle of input WE pulse generator is 50%.

FIGURE 17–VOLTAGE WAVEFORMS, WE TO Y

TYPICAL CHARACTERISTICS

LOW-LEVEL NODE VOLTAGE
(READ MODE)
vs
NODE CURRENT

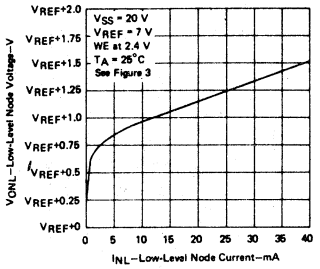


FIGURE 18

LOW-LEVEL NODE VOLTAGE
(READ MODE)
vs
NODE CURRENT

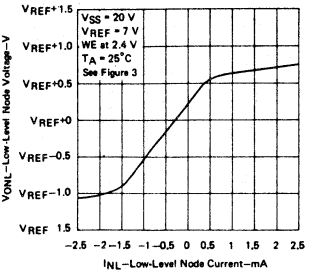


FIGURE 19

DIFFERENTIAL INPUT VOLTAGE
(READ MODE)
vs
DIFFERENTIAL INPUT CURRENT

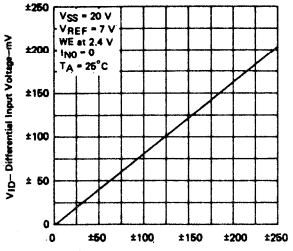


FIGURE 20

OUTPUT VOLTAGE AT Y
(READ MODE)
vs
DIFFERENTIAL INPUT CURRENT

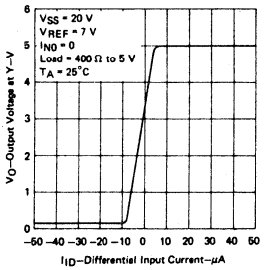


FIGURE 21

SUPPLY CURRENT FROM VSS
(DISABLED MODE)
vs
SUPPLY VOLTAGE VREF

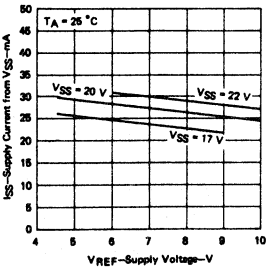


FIGURE 22

SUPPLY CURRENT FROM VREF
(DISABLED MODE)
vs
SUPPLY VOLTAGE VREF

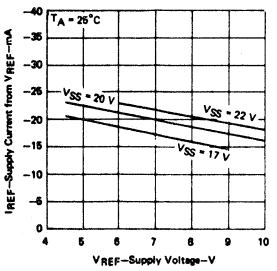


FIGURE 23

7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT FROM V_{SS}
(READ-1, READ-0, OR STANDBY MODE)
vs
SUPPLY VOLTAGE V_{REF}

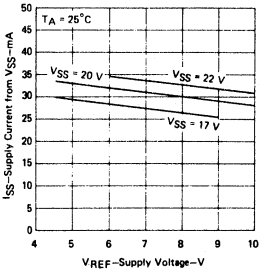


FIGURE 24

SUPPLY CURRENT FROM V_{REF}
(READ-1, READ-0, OR STANDBY MODE)
vs
SUPPLY VOLTAGE V_{REF}

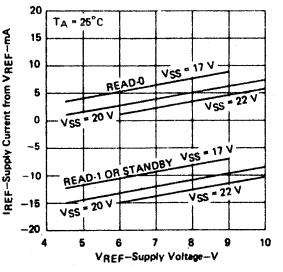


FIGURE 25

SUPPLY CURRENT FROM V_{SS}
(WRITE MODE)
vs
SUPPLY VOLTAGE V_{REF}

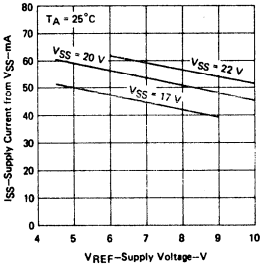


FIGURE 26

SUPPLY CURRENT FROM V_{REF}
(WRITE MODE)
vs
SUPPLY VOLTAGE V_{REF}

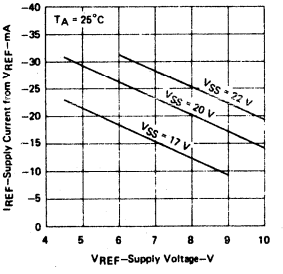


FIGURE 27

SUPPLY CURRENT FROM V_{SS}
vs
FREE-AIR TEMPERATURE

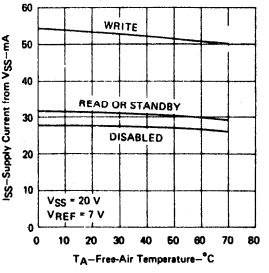


FIGURE 28

SUPPLY VOLTAGE FROM V_{REF}
vs
FREE-AIR TEMPERATURE

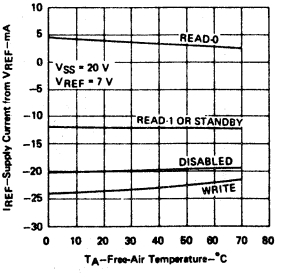


FIGURE 29

TYPICAL APPLICATION DATA

Figure 30 illustrates a typical MOS memory system using SN75370, TMS4062, and SN75361A. All inputs and outputs from this system are TTL-compatible. The SN75361A is a high-speed monolithic dual TTL-to-MOS driver.The address SN75361As select a cell in each of the 72 TMS4062s. In Figure 30 the I/O terminals of the eight TMS4062 RAMs in each row have been connected to the node terminals of the associated SN75370 channel. Time multiplexing of the column of RAMs (M) by the SN75361A Clock/CS and Reset drivers is then used to write into or read from the cells that have been selected by the address SN75361As.

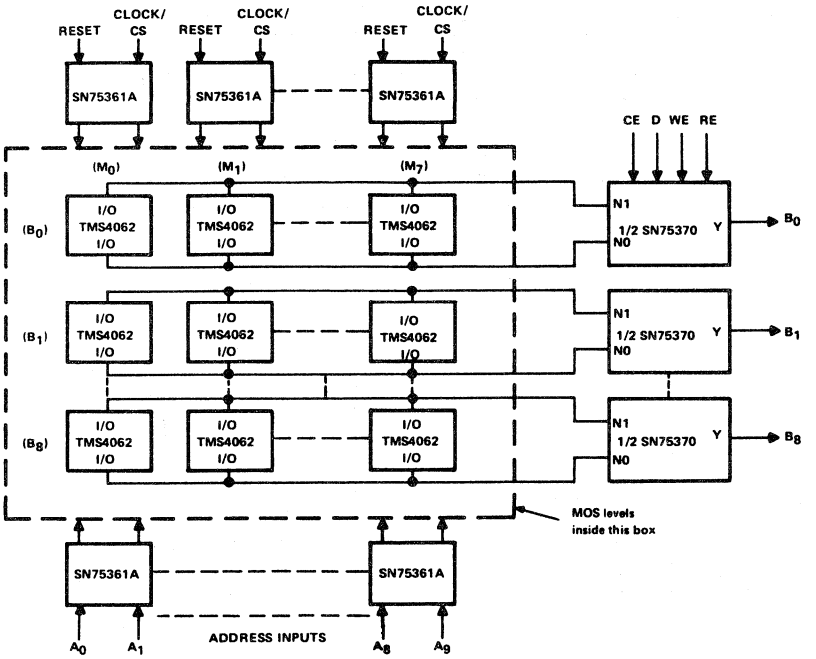


FIGURE 30—BLOCK DIAGRAM OF TOTALLY TTL-COMPATIBLE 8K X 9-BIT MOS-MEMORY SYSTEM USING SN75370, TMS4062, AND SN75361A

TYPICAL APPLICATION DATA

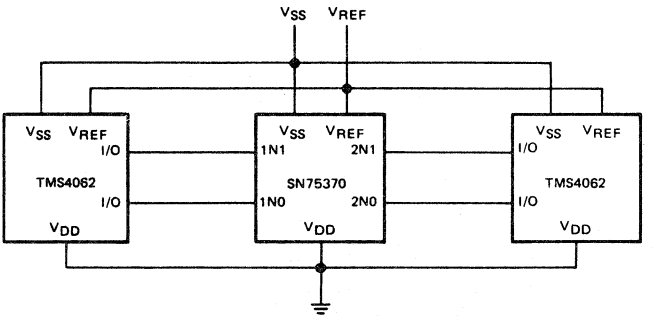
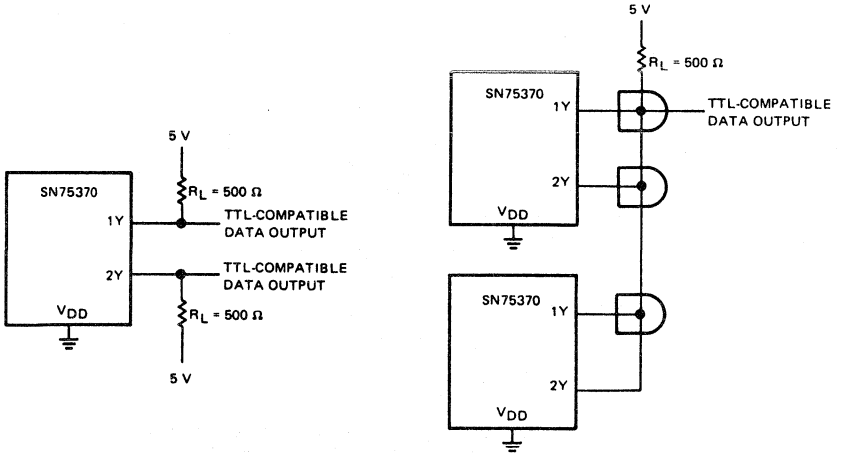


FIGURE 31–INTERCONNECTION OF SN75370 WITH TMS4062 MOS RAM



NOTE A: Pull-up resistor R_L is not necessary, but may be desirable for faster low-to-high-level transition of data output and increased TTL high-level noise margin. The value of R_L is determined by the user based upon the constraints of the system.

FIGURE 32–METHODS OF USING DATA OUTPUTS OF SN75370

TYPICAL APPLICATION DATA

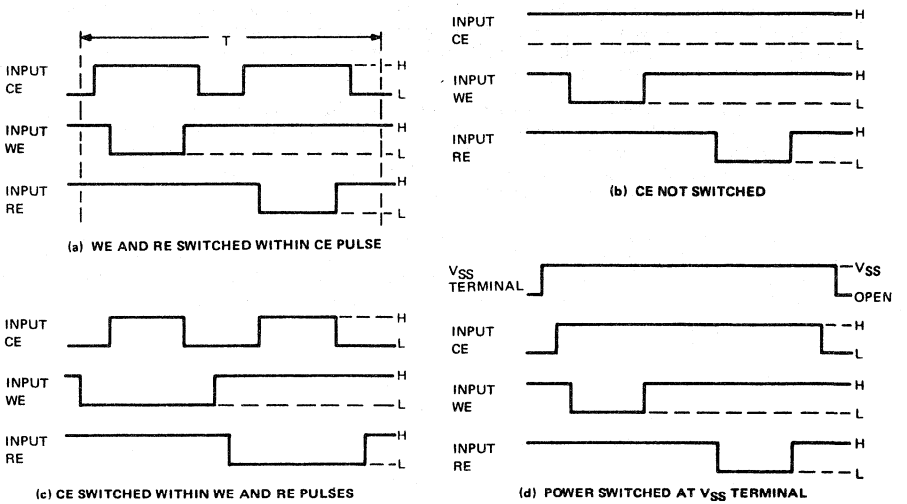


FIGURE 33–TYPICAL OPERATING INPUT VOLTAGE WAVEFORMS FOR SN75370

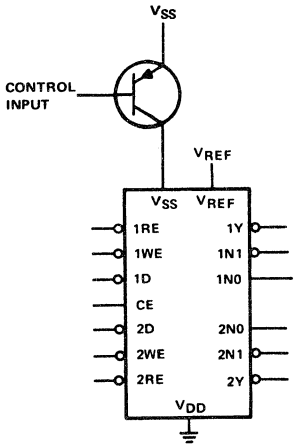


FIGURE 34–SWITCHING POWER TO V_{SS} TERMINAL OF SN75370 USING P-N-P TRANSISTOR

THERMAL INFORMATION

Power generated by the device depends on the mode of operation and the supply voltages used. Under some conditions, the SN75370 may generate sufficient instantaneous power to exceed, on average, the rated continuous power dissipation capability of the package. Appropriate duty-cycling of high-power conditions must be used to keep average power generated by the SN75370 within ratings.

Figure 33 shows typical methods to lower average power dissipation by pulsing the CE, WE, and RE inputs. Highest power occurs when both channels are in the write mode. Usually the write mode must be duty-cycled to reduce average power. Figure 33 (d) and Figure 34 demonstrate the use of a discrete P-N-P transistor to switch power to the V_{SS} terminal of the SN75370 to minimize average power. In addition, forced-air cooling or heat-sinking techniques may be used to increase the dissipation capability of the SN75370.

The following example illustrates a method to calculate average d-c supply power for the SN75370. The typical average power over a period T will be calculated using Figure 33(a). Assume both channels are operating identically, except in read mode when one channel is reading a 1 and the other channel is reading a 0. Let V_{SS} = 20 V, V_{REF} = 7 V and T_A = 25°C. The subscripts W, R, SB, and D refer to write, read, standby, and disabled, respectively.

$$P_{AV} = \frac{t_W P_W + t_R P_R + t_{SB} P_{SB} + t_D P_D}{T}$$

$$T = t_W + t_R + t_{SB} + t_D$$

Typical power for each mode is stated in the electrical characteristics table. This example uses duty cycles (t/T) estimated from Figure 33(a). These values are then substituted in order:

$$P_{AV} = (0.25)\ (910) + (0.25)\ \left(\frac{560+640}{2}\right) + (0.2)\ (560) + (0.3)\ (410)$$

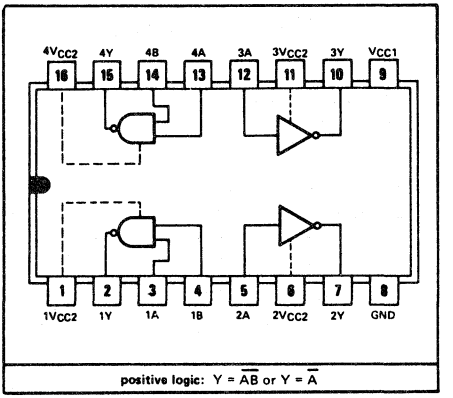
$$P_{AV} = 613\ \text{mW}$$

TYPE SN75375
QUADRUPLE TTL-TO-MOS/PERIPHERAL DRIVER

BULLETIN NO. DL-S 7712564, JULY 1977

- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- Individual V_{CC2} Supplies for Each of the Drivers
- TTL- and DTL-Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$ or $Y = \overline{A}$

description

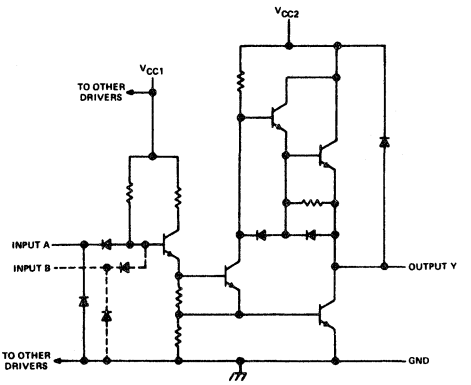
The SN75375 is a monolithic quadruple TTL-to-MOS/peripheral driver and interface circuit. This versatile device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits and peripheral equipment.

The device features individual V_{CC2} supplies for each of the drivers. The individual V_{CC2} pins allow for individual adjustment of high-level output voltage to match various load conditions. The circuit performance is similar to that of the SN75365.

Typical applications include data line transceivers, quad relay drivers, TTL-to-MOS converters, and sink or source drivers for LED's, LCD's, and vacuum fluorescent drivers.

The SN75375 is characterized for operation from 0°C to 70°C.

schematic (each driver)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 25 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Output current	150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the two inputs of either one of the gates.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75375 chips are glass-mounted.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC1}	4.75	5	5.25	V
Supply Voltage, V_{CC2}	4.75	20	24	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	I_{OL} = 1 mA		0.15	0.3	V
		V_{IH} = 2 V,	I_{OL} = 30 mA		0.3	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−1	−1.6	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all 4 drivers, all outputs high					0.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all 4 drivers, all outputs low				14	24	
$I_{CC2(S)}$	Supply current from V_{CC2}, all 4 drivers, standby condition	V_{CC1} = 0 V, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

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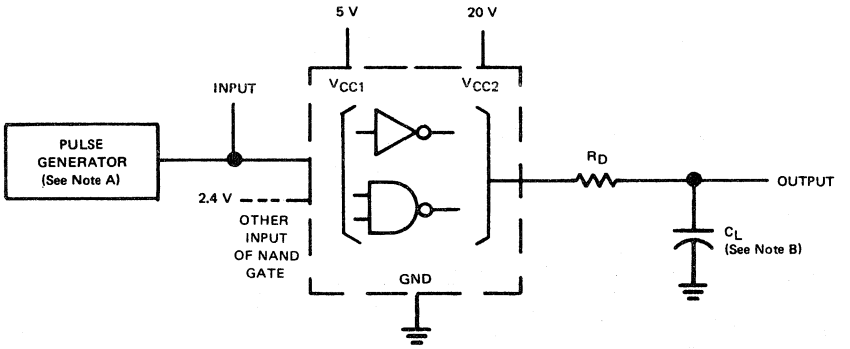
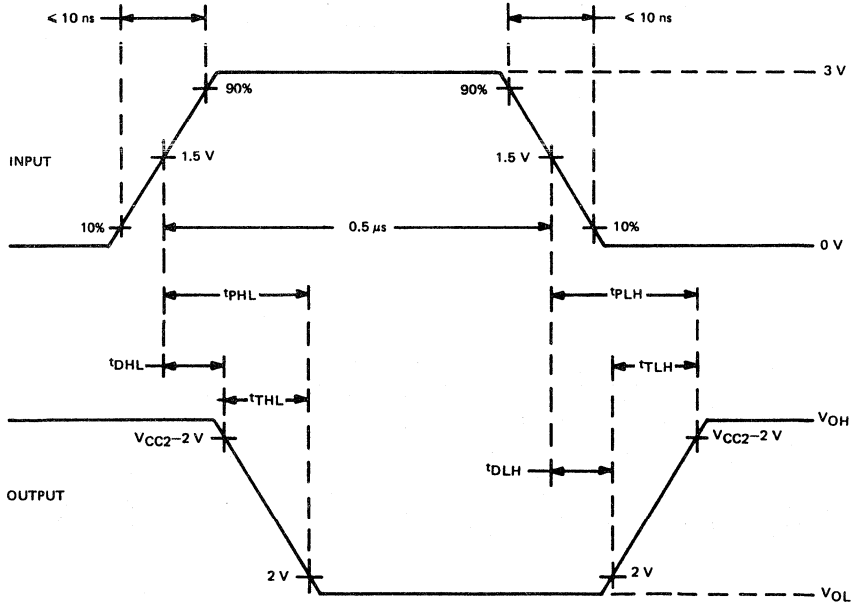
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		18	27	ns
t_{DHL}	Delay time, high-to-low-level output			14	21	ns
t_{TLH}	Transition time, low-to-high-level output			18	27	ns
t_{THL}	Transition time, high-to-low-level output			21	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	36	54	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	34	54	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

Memory Drivers

8

MEMORY DRIVERS

- TTL-COMPATIBLE INPUTS
- CORE MEMORY APPLICATIONS

DESCRIPTION	MAXIMUM OUTPUT CURRENT	t_{pD}¶ TYPICAL	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	ADDITIONAL FEATURES	PAGE NO.
				–55°C TO 125°C	0°C TO 70°C			
DUAL SINK/SOURCE MEMORY DRIVERS	400 mA	75 ns	V_{CC} = 14 V		SN75324	J,N	• Internal decoding and timing circuitry • Output short-circuit protection • Source output terminals swing between 14 V and ground	8–3
	600 mA	35 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V	SN55325	SN75325	J J,N	• Also used for high-voltage, high-current driver applications • Output transient voltage protection • Source output terminals swing between V_{CC2} and ground	8–10
QUADRUPLE MEMORY DRIVERS	600 mA	35 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V	SN55327	SN75327	J J,N	• Also used for high speed magnetic memory applications • Output transient voltage protection • Output capable of swinging between V_{CC2} and ground	8–25
		40 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V		SN75328	J,N	• Also used for bubble memory applications • Output transient voltage protection • Output capable of swinging between V_{CC2} and ground • Uncommitted collectors and emitters • Common external base drive control (SN75238) • Individual external base drive control (SN75330)	8–31
					SN75330			
QUADRUPLE SINK MEMORY DRIVER	600 mA	30 ns	V_{CC} = 5 V	SN55326	SN75326	J J,N	• Also used for high-voltage, high-current driver applications • Output transient voltage protection • 24 V output capability	8–25
EIGHT-CHANNEL MEMORY DRIVER	350 mA	85 ns	V_{CC1} = 5 V, V_{CC2} = 12 V	SN55329		RA	• Bipolar output currents controlled to within 5% • 3-state outputs • Internal power control – does not require power supply sequencing • Contains 3-line to 8-line decoder • 24-pin ceramic flat package • Temperature range: –55°C to 110°C	See Note 1

¶ t_{pD} = Propagation Delay Time

NOTE 1: For additional information, contact your nearest TI field sales office.

TYPE SN75324
MEMORY CORE DRIVER WITH DECODE INPUTS

BULLETIN NO. DL-S 7711169, APRIL 1969–REVISED APRIL 1977

SERIES 75 MEMORY DRIVER

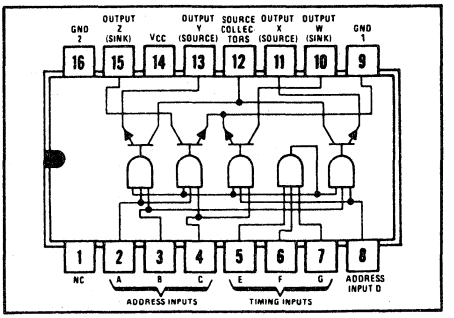
PERFORMANCE

- Fast Switching Times
- 400-mA Output Capability
- Internal Decoding and Timing Circuitry
- Dual Sink/Source Outputs
- Output Short-Circuit Protection

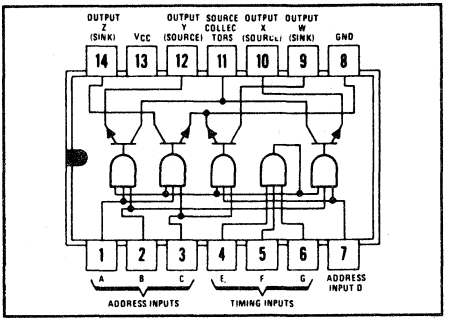
EASE OF DESIGN

- TTL or DTL Compatibility
- Eliminates Transformer Coupling
- Reduces Drive-Line Lengths
- Increases Reliability
- Minimizes External Components

J CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



N PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



NC–No internal connection
GND 1 and GND 2 are to be connected together.

description

The SN75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

The SN75324 is characterized for operation from 0°C to 70°C.

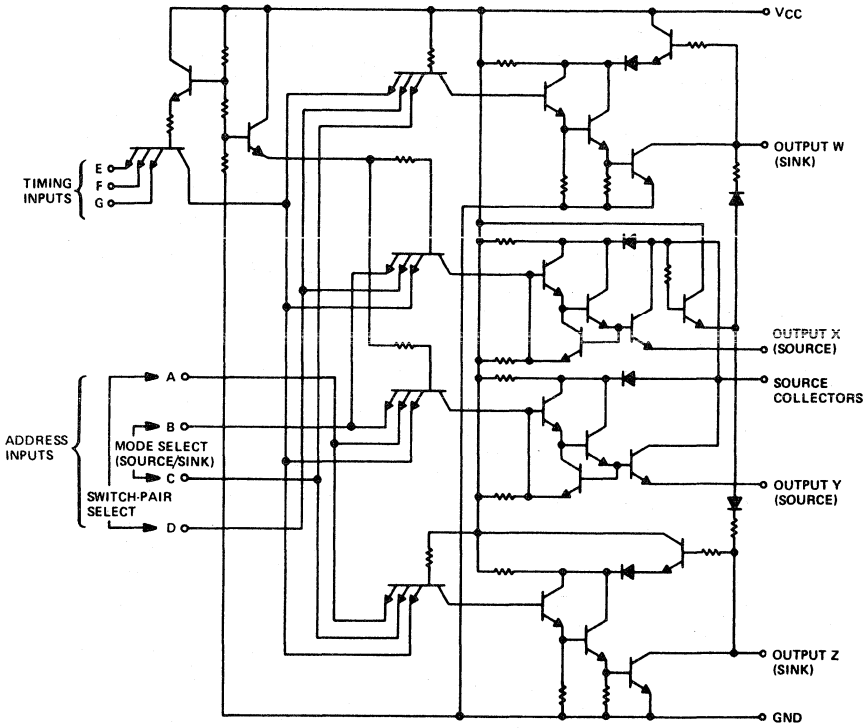
FUNCTION TABLE

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
L	L	H	H	H	H	H	ON	OFF	OFF	OFF
L	H	L	H	H	H	H	OFF	ON	OFF	OFF
H	H	L	L	H	H	H	OFF	OFF	ON	OFF
H	L	H	L	H	H	H	OFF	OFF	OFF	ON
X	X	X	X	L	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	L	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	L	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at one time: When all timing inputs are high, two of the address inputs must be low.

schematic


VCC
OUTPUT W (SINK)
OUTPUT X (SOURCE)
SOURCE COLLECTORS
OUTPUT Y (SOURCE)
OUTPUT Z (SINK)
GND
TIMING INPUTS
E
F
G
ADDRESS INPUTS
A
B
MODE SELECT (SOURCE/SINK)
C
SWITCH-PAIR SELECT
D

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 17 V
Input voltage (See Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Continuous total power dissipation at (or below) 25°C free-air temperature (See Note 3):
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75324 chips are alloy-mounted.

electrical characteristics (unless otherwise noted, V_{CC} = 14 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	1		3.5			V
V_{IL}	Low-level input voltage	1				0.8	V
I_{IH}	High-level input current, address inputs	1	V_I = 5 V			200	μA
I_{IH}	High-level input current, timing inputs	1	V_I = 5 V			100	μA
I_{IL}	Low-level input current, address inputs	1	V_I = 0 V			−6	mA
I_{IL}	Low-level input current, timing inputs	1	V_I = 0 V			−12	mA
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \simeq$ 420 mA, R_L = 53 Ω		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \simeq$ −420 mA, R_L = 47.5 Ω		0.75	0.85	V
I_{off}	Output off-state current	1	V_I = 0 V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_I = 0 V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	42	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

†All typical values are at T_A = 25°C

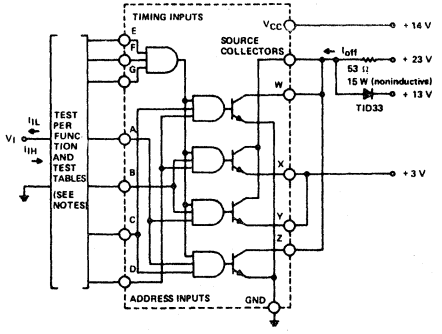
switching characteristics, V_{CC} = 14 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level source output	5	R_{L1} = 53 Ω, R_{L2} = 500 Ω, C_L = 20 pF			90	ns
t_{PHL}	Propagation delay time, high-to-low-level source output	5				50	ns
t_{PLH}	Propagation delay time, low-to-high-level sink output	6	R_L = 53 Ω, C_L = 20 pF			110	ns
t_{PHL}	Propagation delay time, high-to-low-level sink output	6				40	ns
t_s	Sink storage time	6				70	ns

8

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

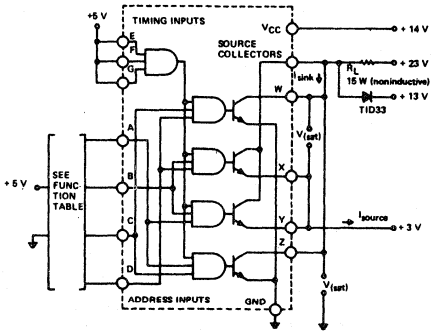


TEST TABLE FOR I_{IL}

APPLY 3.5 V	GROUND	TEST I_{IL}
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES: 1. Check V_{IH} and V_{IL} per Function Table.
2. Measure I_{IL} per Test Table.
3. When measuring I_{IH}, all other inputs are at ground. Each input is tested separately.

FIGURE 1–V_{IL}, V_{IH}, I_{IL}, I_{IH}, and I_{off}



NOTE: This parameter must be using pulse techniques. t_w = 500 ns, duty cycle < 1%.

FIGURE 2 – $V_{(sat)}$

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

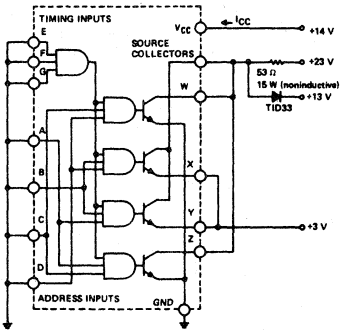
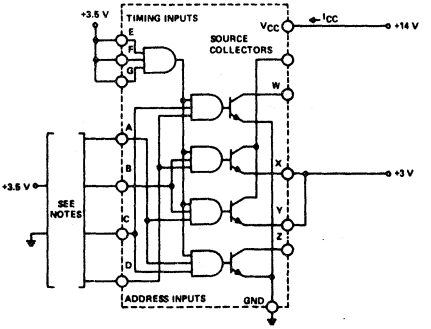


FIGURE 3 – I_{CC} (ALL OUTPUTS OFF)



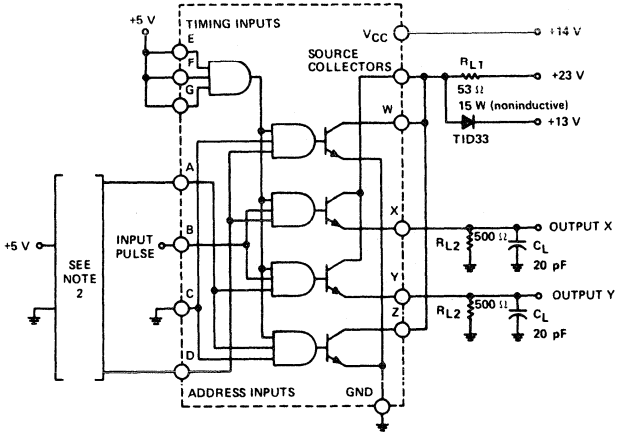
NOTES: 1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4 – I_{CC} (ONE OUTPUT ON)

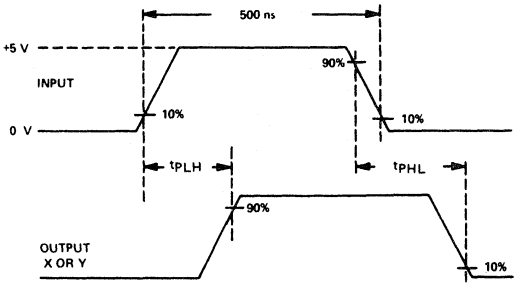
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



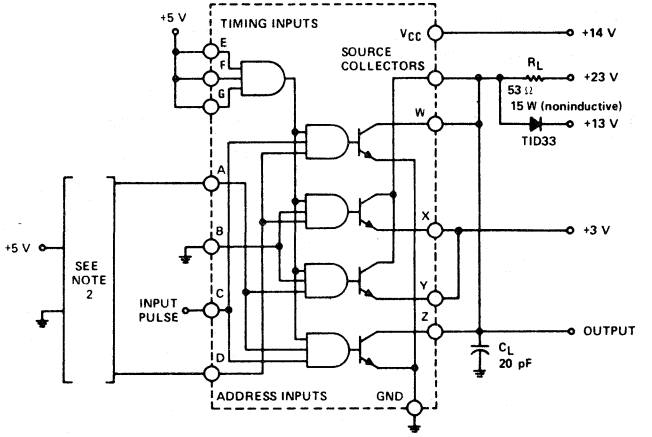
VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W.

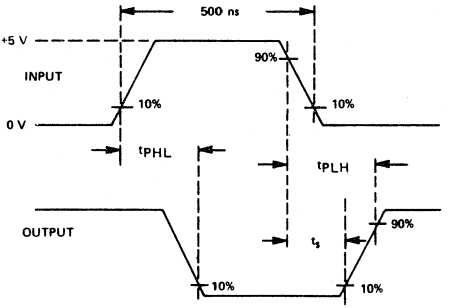
FIGURE 5 – SOURCE-OUTPUT SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output W, apply +5 V to input D, and ground A. When measuring delay times at output Z, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SINK-OUTPUT SWITCHING TIMES

TYPES SN55325, SN75325 MEMORY CORE DRIVERS

BULLETIN NO. DL-S 7711437, MARCH 1971 – REVISED APRIL 1977

SERIES 55/75 MEMORY DRIVER
featuring

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Transient-Voltage Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

description

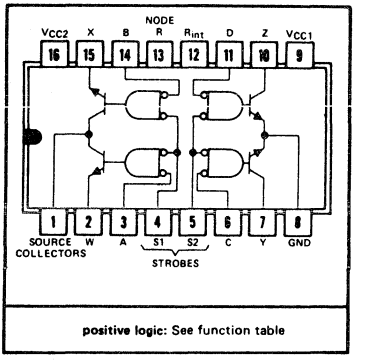
The SN55325 and SN75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source switches and two 600-milliampere sink switches. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75325 is characterized for operation from 0°C to 70°C.

REVISED APRIL 1977

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55325	SN75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1375	mW
	N package		1150	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN55325 and SN75325 chips are alloy-mounted.

electrical characteristics over rated operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS		SN55325 MIN	SN55325 TYP‡	SN55325 MAX	SN75325 MIN	SN75325 TYP‡	SN75325 MAX	UNIT
V_{IH}	High-level input voltage		1 & 2			2			2			V
V_{IL}	Low-level input voltage		3 & 4					0.8			0.8	V
V_{IK}	Input clamp voltage		5	V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		1	V_{CC1} = 4.5 V, V_{CC2} = 24 V	T_A = full range †			500			200	μA
					T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		2	V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage	source outputs	3	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA§, See Note 3	T_A = full range †			0.9			0.9	V
					T_A = 25°C		0.43	0.7		0.43	0.75	
		sink outputs	4	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA§, See Note 3	T_A = full range †			0.9			0.9	
					T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	5	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs						2			2	
I_{IH}	High-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs					6	80		6	80	
I_{IL}	Low-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs					−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	6	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}					7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		7	V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		8	V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA, See Note 3	V_{CC2} = 24 V, T_A = 25°C,		32	50		32	50	mA

†Full range for SN55325 is −55°C to 125°C and for SN75325 is 0°C to 70°C.

‡All typical values are at T_A = 25°C.

§Under these conditions, not more than one output is to be on at any one time.

NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle < 2%.

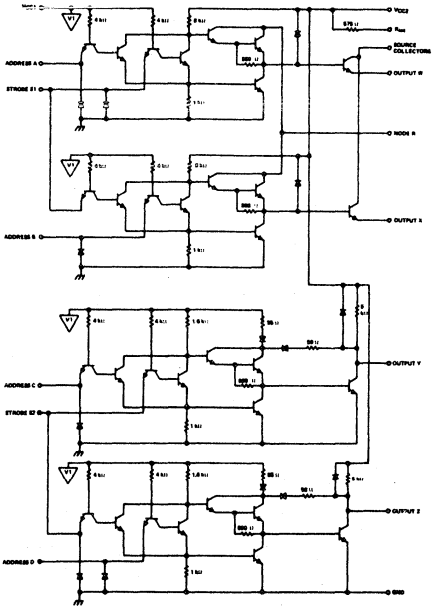
8

switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER[1]	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		35	50	ns
t_{PHL}					35	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

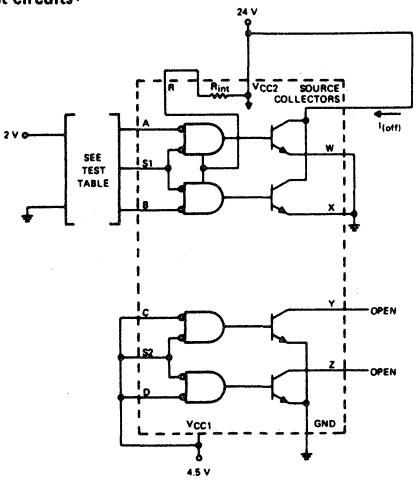
schematic



Component values shown are nominal.
V1 . . . V_{CC1} bus

PARAMETER MEASUREMENT INFORMATION

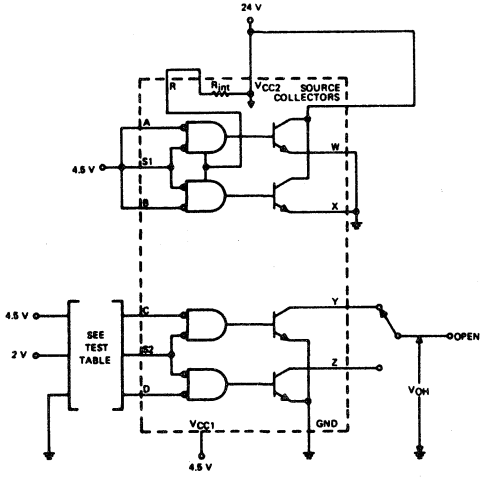
d-c test circuits†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

FIGURE 1–V_{IH} AND $I_{(off)}$



TEST TABLE

C	D	S2	Y	Z
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

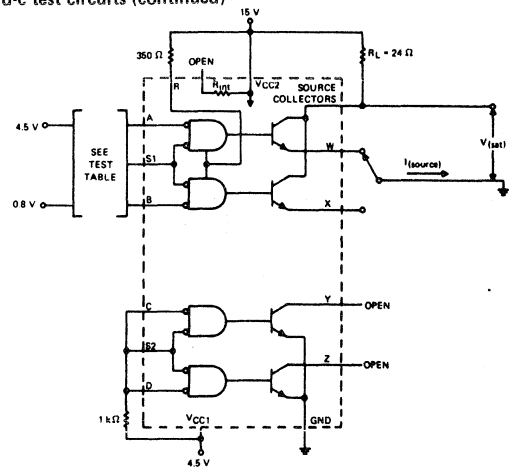
FIGURE 2–V_{IH} AND V_{OH}

†Arrows indicate actual direction of current flow.

8

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†

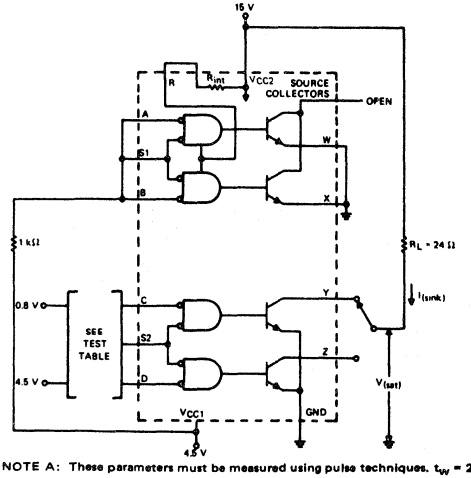


TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle < 2%.

FIGURE 3–V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

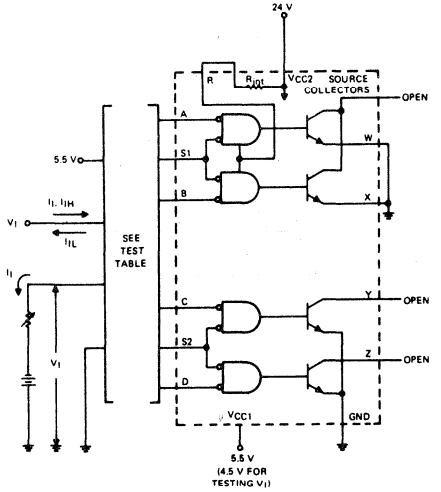
NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle < 2%.

FIGURE 4–V_{IL} AND SINK $V_{(sat)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5 V, MEASURE I_I APPLY V_I = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4 V, MEASURE I_{IL} APPLY I_I = −10 mA MEASURE V_I	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5–V_I, I_I, I_{IH}, AND I_{IL}

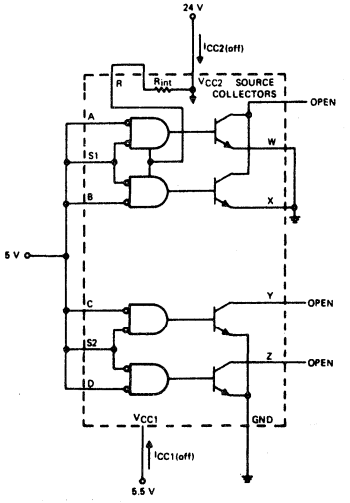
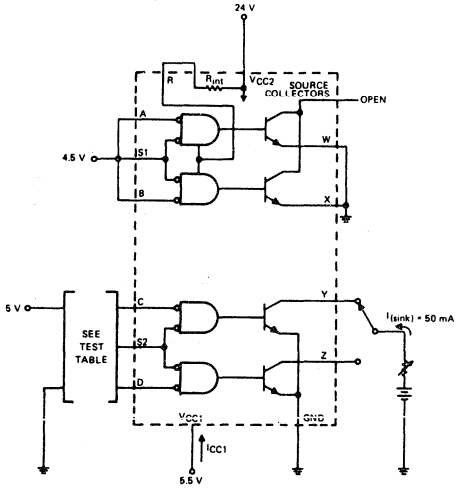


FIGURE 6–$I_{CC1(off)}$ AND $I_{CC2(off)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

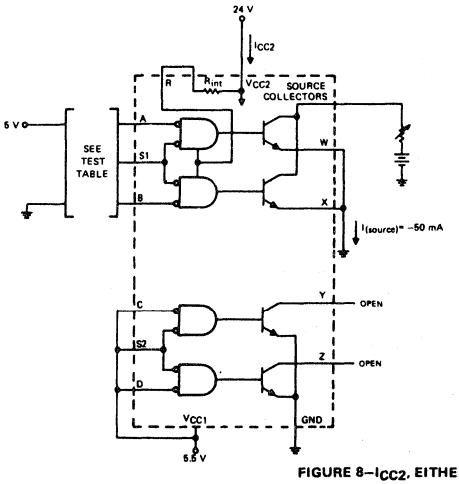
d-c test circuits (continued)†



TEST TABLE

C	D	S2	Y	Z
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

FIGURE 7–I_{CC1}, EITHER SINK ON



TEST TABLE

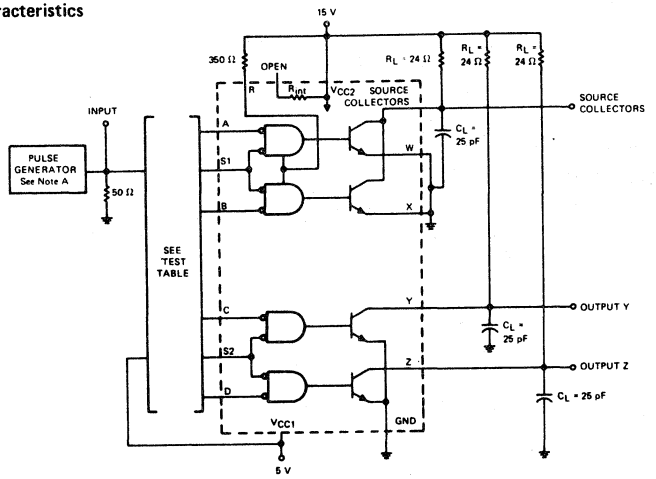
A	B	S1
GND	5 V	GND
5 V	GND	GND

FIGURE 8–I_{CC2}, EITHER SOURCE ON

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

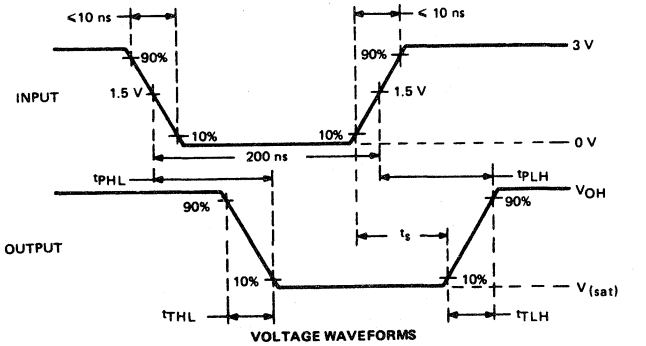
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1



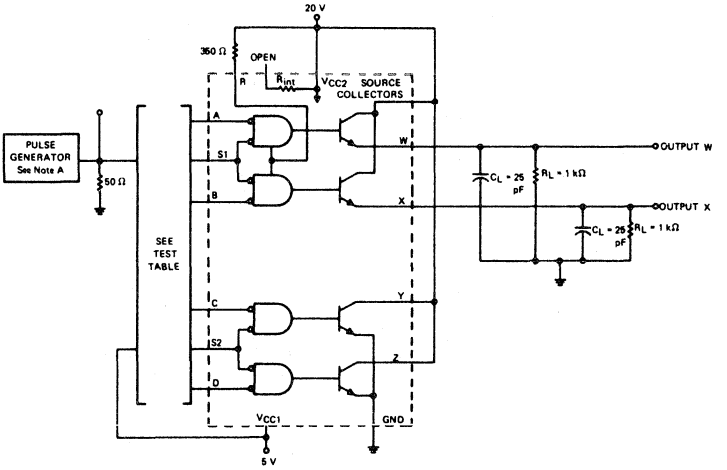
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

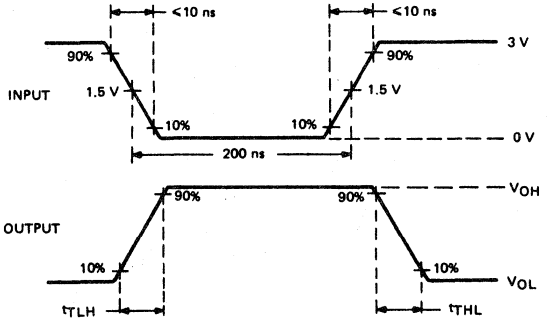
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle < 1%.
B. C_L includes probe and jig capacitance.

FIGURE 10–TRANSITION TIMES OF SOURCE OUTPUTS

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS
vs
FREE-AIR TEMPERATURE

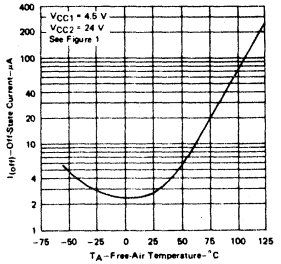


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

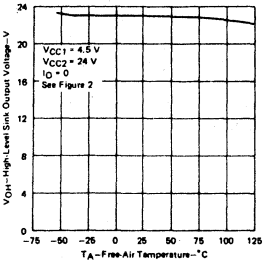


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE
vs
SOURCE CURRENT OR SINK CURRENT

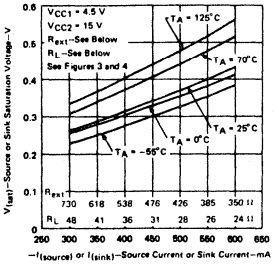


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

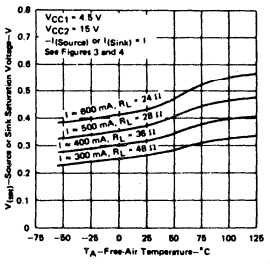


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF
vs
FREE-AIR TEMPERATURE

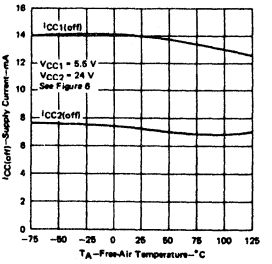


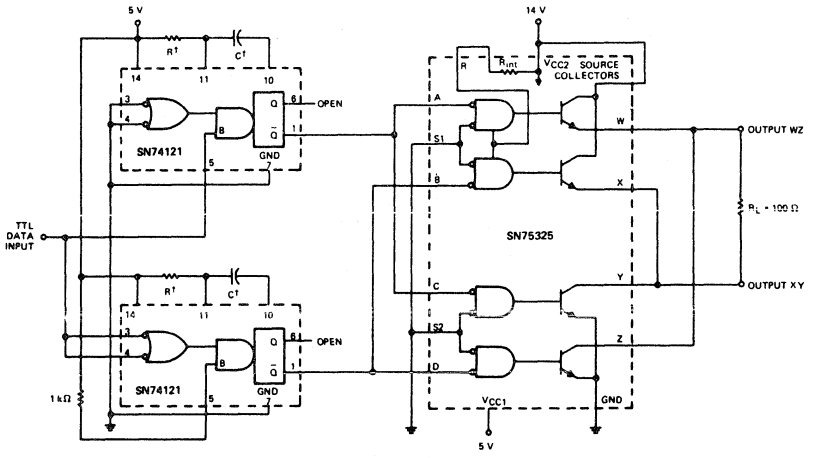
FIGURE 15

8

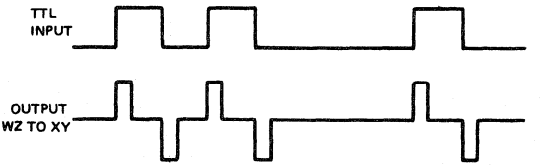
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a three-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several thousand feet in length or low-impedance coaxial lines.



TEST CIRCUIT



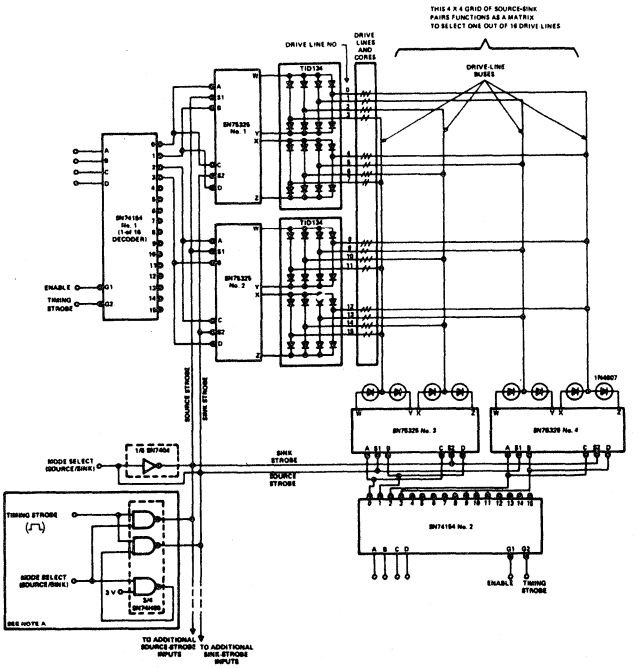
VOLTAGE WAVEFORMS

†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 16–BALANCED BIPOLAR LOGIC–LINE DRIVER

TYPICAL APPLICATION DATA

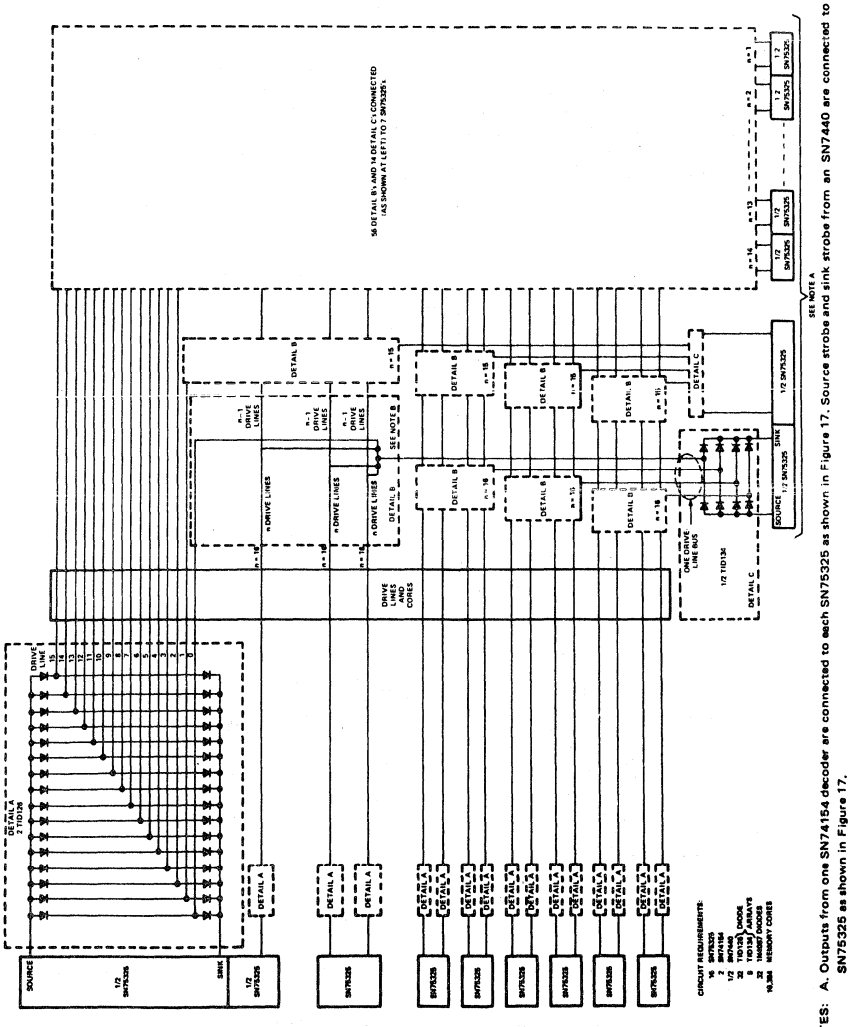
In memory-drive applications the SN75325 (or for full-temperature operation, the SN55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN74154 No. 1 must be set to 3 (with mode select high), enabling source X of SN75325 No. 2 to drive lines 12 through 15, and SN74154 No. 2 must be set to 2, providing a sink at Y of SN75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN7440 mode-select and SN74154 timing-strobe when minimum time skew is desired.

FIGURE 17–SN75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

TYPICAL APPLICATION DATA



NOTES: A. Outputs from one SN74154 decoder are connected to each SN75325 as shown in Figure 17. Source strobe and sink strobe from an SN7440 are connected to each SN75325 as shown in Figure 17.
B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

FIGURE 18—SN75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one SN75325 delivers load current (I_L). The sink-output transistor of another SN75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\, I_L \qquad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20 V and V_L = 3 V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

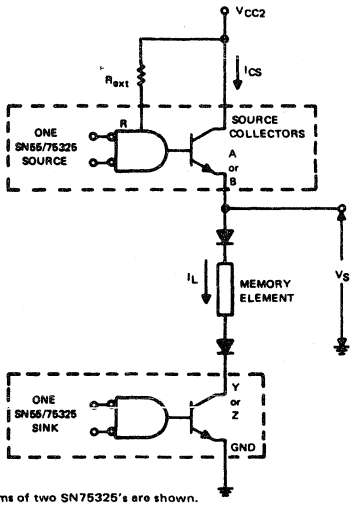
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN75325's are shown.
B. Source and sink shown are in different packages.

FIGURE 19

8

TYPES SN55326, SN55327, SN75326, SN75327 MEMORY CORE DRIVERS

BULLETIN NO. DL-S 7712063, SEPTEMBER 1973 – REVISED APRIL 1977

SERIES 55/75 MEMORY DRIVERS
featuring

SN55326, SN75326 PERFORMANCE

- Quad Positive-OR Sink Memory Drivers
- 600-mA Output Current Sink Capability
- 24-V Output Capability
- Clamp Voltage Variable to 24 V

SN55327, SN75327 PERFORMANCE

- Quad Memory Switches
- 600-mA Output Current Capability
- V_{CC2} Drive Voltage Variable to 24 V
- Output Capable of Swinging Between V_{CC2} and Ground

EASE OF DESIGN

- High-Repetition-Rate Driver Compatible with High-Speed Magnetic Memories
- Inputs Compatible with TTL Decoders
- Minimum Time Skew between Strobe and Output-Current Rise
- Pulse-Transformer Coupling Eliminated
- Drive-Line Lengths Reduced

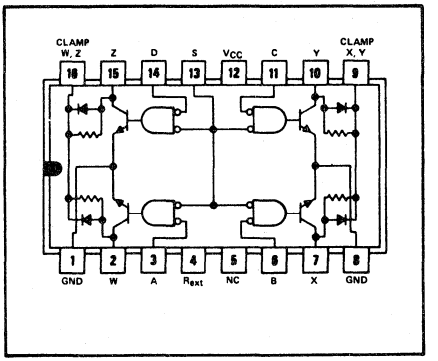
description

The SN55326, SN55327, SN75326, and SN75327 are monolithic integrated circuit quadruple memory drivers. These devices accept standard TTL decoder input signals and provide high-current and high-voltage output levels suitable for driving magnetic memory elements. Output transistor selection is determined by using one of the four address inputs and the common timing strobe.

The SN55326 and SN75326 memory drivers can sink up to 600 milliamperes and operate from a single 5-volt supply. Each driver is similar to the sink drivers of the SN55325/SN75325. The four output transistors share a common base-drive resistor and it is recommended that only one of the four driver gates be selected at a time. Output-transistor base current may be increased by connecting an external resistor between R_{ext} (pin 4) and V_{CC}. Each output collector is protected from voltage surges during inductive switching by a clamp diode in parallel with its internal pull-up resistor. The two clamp pins may be returned to a power supply of from 4.5 volts to 24 volts.

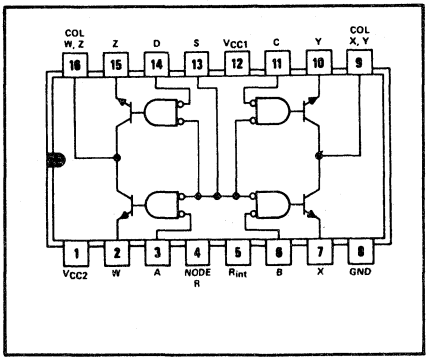
The SN55327 and SN75327 memory switches can source or sink up to 600 milliamperes and operate from two supplies; one of five volts and the other from 4.5 volts to 24 volts. Each switch is similar to the source drivers of the SN55325/SN75325. They can function as either sink drivers or source drivers since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground. The four output transistors share a common base-drive resistor and it is recommended that only one of the four outputs be selected at a time. An internal base-drive resistor is available on the chip and can be

SN55326, SN75326
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

SN55327, SN75327
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



8

description (continued)

used by connecting Node R (pin 4) to R_{int} (pin 5). This resistor provides adequate base current to the output transistors for output sink currents up to 375 milliamperes with V_{CC2} at 15 volts or 600 milliamperes with V_{CC2} at 24 volts. Base current can be regulated to within ±5 percent by substituting for this resistor an external resistor connected between Node R (pin 4) and V_{CC2} with R_{int} (pin 5) remaining open. This method is preferable in high-duty-cycle, high-power applications since the power dissipated in this resistor is outside the package. When a source current and V_{CC2} voltage other than the above values are required, it is recommended that the base drive be supplied through an external resistor of the appropriate value calculated using Equation 1 shown in the SN55325, SN75325 data sheet.

FUNCTION TABLE

INPUTS					OUTPUTS			
ADDRESS				STROBE				
A	B	C	D	S	W	X	Y	Z
L	H	H	H	L	ON	OFF	OFF	OFF
H	L	H	H	L	OFF	ON	OFF	OFF
H	H	L	H	L	OFF	OFF	ON	OFF
H	H	H	L	L	OFF	OFF	OFF	ON
H	H	H	H	X	OFF	OFF	OFF	OFF
X	X	X	X	H	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

The SN55326 and SN55327 circuits are characterized for operation over the full military temperature range of –55°C to 125°C; the SN75326 and SN75327 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55326	SN75326	SN55327	SN75327	UNIT
Supply voltage, V_{CC} or V_{CC1} (see Note 1)		7	7	7	7	V
Supply voltage, V_{CC2}				25	25	V
Input voltage, any address or strobe		5.5	5.5	5.5	5.5	V
Output collector voltage		25	25	25	25	V
Output clamp voltage		25	25			V
Output collector current		750	750	750	750	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1375	1375	1375	mW
	N package		1150		1150	
Operating free-air temperature range		–55 to 125	0 to 70	–55 to 125	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260	260	260	260	°C

recommended operating conditions

	SN55326			SN75326			SN55327			SN75327			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} or V_{CC1}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{CC2}							4.5		24	4.5		24	V
Output collector voltage			24			24			24			24	V
Output-clamp voltage, $V_{(clamp)}$	4.5		24	4.5		24							V
Output collector current			600			600			600			600	mA
Operating free-air temperature, T_A	–55		125	0		70	–55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal(s).
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, these chips are alloy-mounted.

SN55326, SN75326 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55326			SN75326			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA,		−1	−1.7		−1	−1.7	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_O = 0	19	23		19	23		V
$V_{(sat)}$	Saturation voltage		V_{CC} = 4.5 V, $I_{(sink)}$ = 600 mA§, See Note 3	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
$V_{F(clamp)}$	Output-clamp-diode forward voltage		$V_{(clamp)}$ = 0, T_A = 25°C	$I_{(clamp)}$ = −10 mA,			1.5			1.5	V
$I_{(clamp)}$	Output-clamp current, one output on		$I_{(sink)}$ = 50 mA, T_A = 25°C			5	7		5	7	mA
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off		All inputs at 5 V, T_A = 25°C			18	25		18	25	mA
$I_{CC(on)}$	Supply current, one output on		$I_{(sink)}$ = 50 mA, T_A = 25°C			58	75		58	75	mA

SN55326, SN75326 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 3		30	50	ns
t_{PHL}				25	50	
t_{TLH}	W, X, Y, or Z			7	15	ns
t_{THL}				10	20	
t_s	W, X, Y, or Z			24	35	ns
V_{OH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 3	V_S−25			mV

†Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 1.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
t_s ≡ Storage time
V_{OH} ≡ High-level output voltage (after switching)
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle < 2%.

For typical characteristic curves, Figures 11 through 14 of the SN55325/SN75325 data sheet apply for these circuits.

SN55327, SN75327 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55327 MIN	SN55327 TYP‡	SN55327 MAX	SN75327 MIN	SN75327 TYP‡	SN75327 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA		−1	−1.7		−1	−1.7	V
$I_{(off)}$	Collectors terminal off-state current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full range			500			200	μA
				T_A = 25°C			150			200	
$V_{(sat)}$	Saturation voltage		V_{CC1} = 4.5 V, V_O = 0, $I_{(source)}$ = −600 mA§, See Notes 3 and 4	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off	From V_{CC1}	All inputs at 5 V,	T_A = 25°C		7	10		7	10	mA
		From V_{CC2}				13	20		13	20	
$I_{CC(on)}$	Supply current, one output on	From V_{CC1}	$V_{(col)}$ = 6 V,	$I_{(source)}$ = −50 mA,		8	12		8	12	mA
		From V_{CC2}	T_A = 25°C,	See Note 3		36	55		36	55	

SN55327, SN75327 switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 3 and Note 4		35	55	ns
t_{PHL}				30	55	
t_{TLH}	W, X, Y, or Z	$V_{(col)}$ = V_{CC2} = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 4 and Note 4		30		ns
t_{THL}				10		
V_{OH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 24 V, $I_{(sink)}$ ≈ 500 mA, R_L = 47 Ω, C_L = 25 pF, See Figure 3 and Note 4	V_S−25			mV

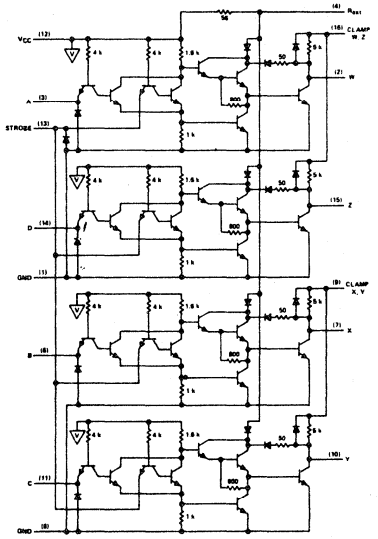
†Unless otherwise noted, V_{CC1} = 5.5 V, V_{CC2} = 24 V. See Figure 2.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
V_{OH} ≡ High-level output voltage (after switching)

NOTES: 3. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.
4. A 350-Ω resistor is connected between node R (pin 4) and V_{CC2} (pin 1) with R_{int} (pin 5) open.

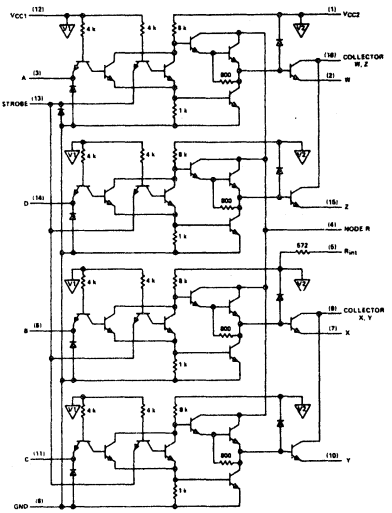
For typical characteristic curves, Figures 11 through 14 of the SN55326/SN75326 data sheet apply for these circuits.

schematics

SN55326, SN75326



SN55327, SN75327



▽ ▽ ▽ . . . V_{CC}, V_{CC1}, or V_{CC2} bus, respectively.

Resistor values shown are nominal and in ohms.

PARAMETER MEASUREMENT INFORMATION

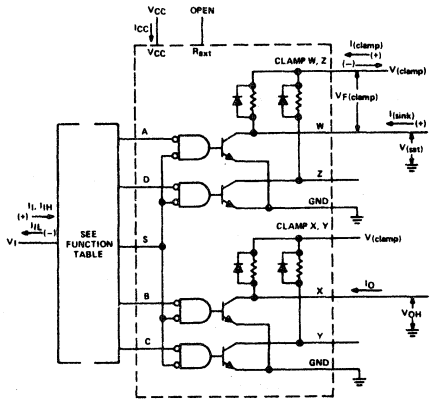
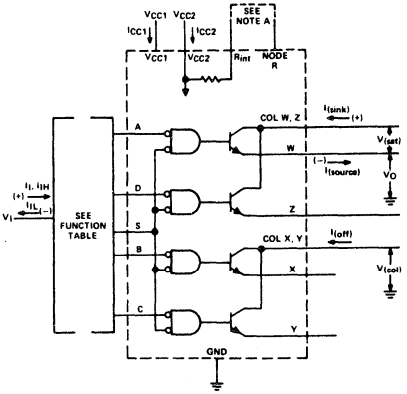


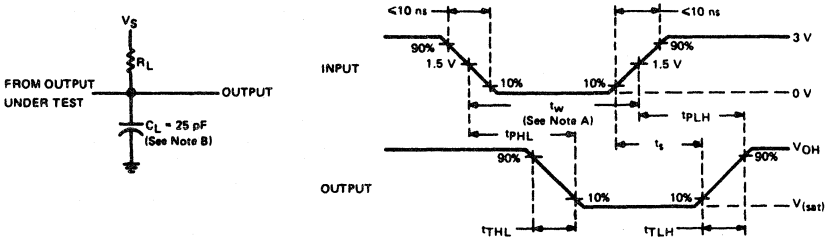
FIGURE 1–GENERALIZED TEST CIRCUIT
FOR SN55326, SN75326



NOTE A: R_{int} is connected to Node R unless otherwise noted.

FIGURE 2–GENERALIZED TEST CIRCUIT
FOR SN55327, SN75327

PARAMETER MEASUREMENT INFORMATION

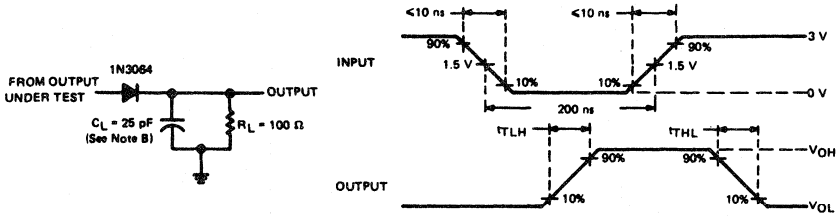


LOAD CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For testing V_{OH} (after switching), t_w = 40 μs, PRR = 12.5 kHz. For all other tests, t_w = 200 ns, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES

8



LOAD CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 4–SWITCHING TIMES

TYPES SN75328, SN75330 QUADRUPLE MEMORY SWITCHES

BULLETIN NO. DL-S 7712458, APRIL 1977

- Quadruple Interface for Core and Bubble Memories
- Characterized for Use to 600 mA
- 24-V Output Capability
- Output Transient Voltage Protection
- Fast Switching Times . . . 40 ns Typ
- Outputs Capable of Swinging Between V_{CC2} and Ground
- Source/Sink Base Drive Externally Adjustable
- TTL- or DTL-Compatible Inputs
- Input Clamping Diodes

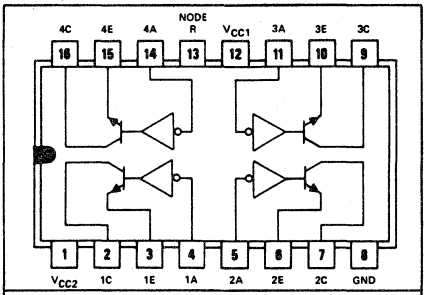
description

The SN75328 and SN75330 are monolithic integrated circuit memory switches with TTL logic inputs that are designed for use with core and bubble memories. Each device contains four 600-milliampere memory switches and operates from two power supplies, one of 5 volts and the other from 4.75 volts to 24 volts. Each switch is similar to the SN75327 except that the strobe circuitry is omitted, which allows the collectors of the output transistors to be assigned to individual package pins.

Each switch can function as either source driver or sink driver since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground. On SN75328 the base drive of all four output transistors is provided by connecting an external resistor of the appropriate value between V_{CC2} and Node R. On SN75330 the base drive of each individual output transistor is provided by connecting an external resistor of the appropriate value between V_{CC2} and the corresponding Node R. By using this method the base current may usually be regulated within ±5%, and the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher currents for a given junction temperature.

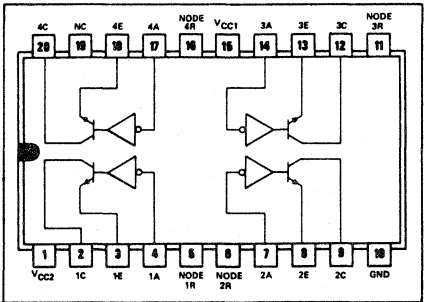
The SN75328 and SN75330 are characterized for operation from 0°C to 70°C.

SN75328
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: A low logic level at input A turns the switch on.

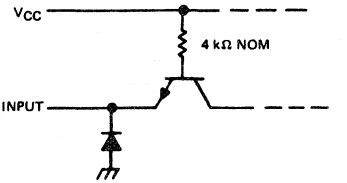
SN75330
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: A low logic level at input A turns the switch on.

NC = No internal connection

schematic of each input



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 25 V
Input voltage . . . . . 5.5 V
Output collector voltage . . . . . 25 V
Output collector current . . . . . 750 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1. In the J package, SN75328 and SN75330 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75		24	V
Output collector voltage			24	V
Output collector current			600	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_{IK}	Input clamp voltage	V_{CC1} = 4.75 V, I_I = −10 mA					−1	−1.7	V
$I_{(off)}$	Collector off-state current	V_{CC1} = 4.75 V, $V_{(col)}$ = 24 V, See Figure 1						200	μA
$V_{(sat)}$	Saturation voltage	V_{CC1} = 4.75 V, V_{CC2} = 15 V, See Figure 1, See Note 3	R_L = 285 Ω,	R_{ext} = 3.9 kΩ,	$I_{(sink)}$ ≈ 50 mA		120	200	mV
			R_L = 95 Ω,	R_{ext} = 1.3 kΩ,	$I_{(sink)}$ ≈ 150 mA		300	400	
			R_L = 48 Ω,	R_{ext} = 650 Ω,	$I_{(sink)}$ ≈ 300 mA§		420	550	
			R_L = 32 Ω,	R_{ext} = 430 Ω,	$I_{(sink)}$ ≈ 450 mA§		500	650	
			R_L = 24 Ω,	R_{ext} = 350 Ω,	$I_{(sink)}$ ≈ 600 mA§		600	750	
I_I	Input current at maximum input voltage	V_I = 5.5V						1	mA
I_{IH}	High-level input current	V_I = 2.4 V						40	μA
I_{IL}	Low-level input current	V_I = 0.4 V					−1	−1.6	mA
$I_{CC(off)}$	Supply current, all outputs off	All inputs at 5 V, T_A = 25°C			From V_{CC1}		7	10	mA
					From V_{CC2}		13	20	
$I_{CC(on)}$	Supply current, one output on	$V_{(col)}$ = 6 V, T_A = 25°C,	$I_{(source)}$ = −50 mA, See Note 3		From V_{CC1}		8	12	mA
					From V_{CC2}		36	55	

†Unless otherwise noted, V_{CC1} = 5.25 V' V_{CC2} = 24 V.
‡All typical values are at T_A = 25°C.
§Under these conditions, only one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques, t_w = 200 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$V_S = V_{CC2} = 15V$, $R_L = 24\ \Omega$, $C_L = 25$ pF, $R_{ext} = 350\ \Omega$, See Figure 2		40	60	ns
t_{PHL}	Propagation delay time, high-to-low level output			30	50	ns
t_{TLH}	Transition time, low-to-high level output			20	30	ns
t_{THL}	Transition time, high-to-low level output			15	25	ns
V_{OH}	High-level output voltage after switching	$V_S = V_{CC2} = 24$ V, $R_L = 47\ \Omega$, $C_L = 25$ pF, $R_{ext} = 350\ \Omega$, $I_{(sink)} \approx 500$ mA, See Figure 2	$V_S - 25$			mV

§Under these conditions, only one output is to be on at any one time.

PARAMETER MEASUREMENT INFORMATION†

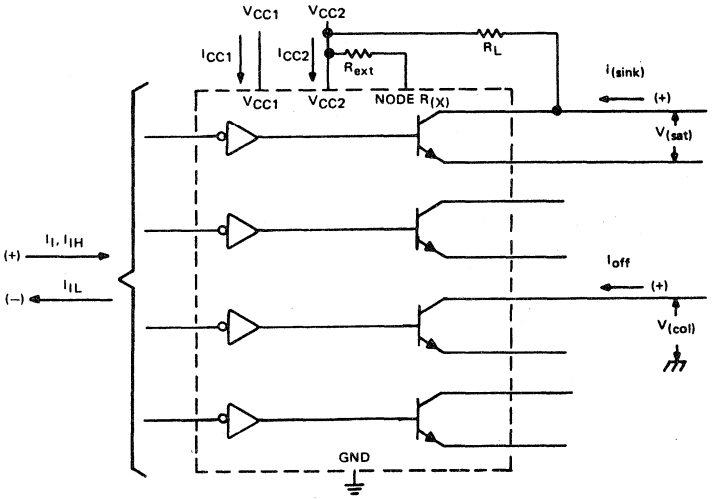
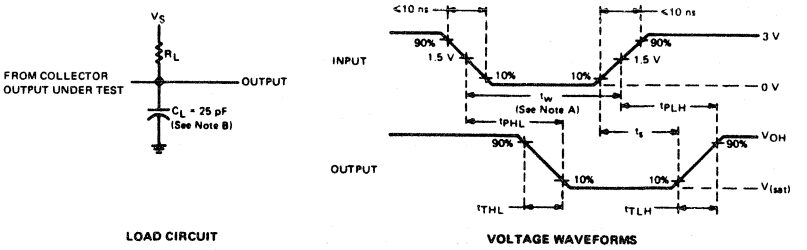


FIGURE 1–GENERALIZED TEST CIRCUIT

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



LOAD CIRCUIT VOLTAGE WAVEFORMS

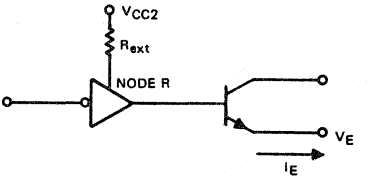
NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For testing V_{OH} after switching, t_w = 40 μs, PRR = 12.5 kHz. For all other tests, t_w = 200 ns, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES

TYPICAL APPLICATION DATA

external resistor calculation

The value of R_{ext} for any particular output current level may be determined by using the following equation:



$$R_{ext} = \frac{16(V_{CC2} - V_E - 2.2)}{|I_E| - 1.6\,(V_{CC2} - V_E - 2.9)}$$

where I_E is in mA and R_{ext} in kΩ.

Example 1. For I_E = –300 mA, V_E = 4 V, V_{CC2} = 24 V
R_{ext} = 1 kΩ

Example 2. For I_E = –600 mA, V_E = 4 V, V_{CC2} = 24 V
R_{ext} = 0.5 kΩ

Display Drivers

9

DISPLAY DRIVERS
FOR COMMERCIAL TEMPERATURE RANGE

DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	ADDITIONAL FEATURES	PAGE NO.
AC PLASMA DISPLAYS	AXIS DRIVERS	CMOS	V_{CC1} = 12 V, V_{CC2} variable from 40 V to 90 V	4	SN75426B	J,N	• Independent addressing of each gate for serial and parallel applications • High input impedance (typically 1 megohm) • 30-mA clamp diodes on output • Switches 70 V in 1.2 μs • AND driver (SN75426); NAND driver (SN75427)	9–9
					SN75427B	J,N		
		CMOS	V_{CC1} = 12 V, V_{CC2} variable from V_{CC1} to 100 V	32	SN75500A	N	• High-speed serially shifted data input (4 MHz max) • Fast output transitions (less than 150 ns) • 25-mA output current capability • Output short-circuit capability • Static shift registers can retain data on all outputs of SN75501 and SN75503A indefinitely • X-axis driver – SN75500A and SN75502A • Y-axis driver – SN75501A and SN75503A perform Y-axis sustaining function)	9–43
		TTL			SN75502A	N		
		CMOS			SN75501A	N		9–47
		TTL			SN75503A	N		
LED DISPLAYS	SEGMENT DRIVERS	MOS	10 V	4	SN75491	N	• 50-mA source/sink capability	9–25
			20 V	4	SN75491A	N		
			Variable from 3.2 V to 8.8 V	4	SN7593	N	• 50-mA regulated source capability • Display blanking provisions	9–33
	DIGIT DRIVERS	MOS	10 V	6	SN75492	N	• 250-mA sink capability	9–25
			20 V	6	SN75492A	N		
			Variable from 3.2 V to 8.8 V	6	SN75494	N	• 250-mA sink capability • Display blanking provisions	9–33
		TTL	10 V	6	SN75496	N	• 250-mA sink capability	9–37
			20 V	6	SN75496A	N		
		MOS, TTL	Variable from 2.7 V to 6.6 V	7	SN75497	N	• 100-mA sink capability • Input threshold . . . 2.7 V max • Low voltage saturating outputs (0.4 V maximum)	9–39
		MOS, TTL	Variable from 2.7 V to 6.6 V	9	SN75498	N	• 100-mA sink capability • Input threshold . . . 2.7 V max	9–39

DISPLAY DRIVERS
FOR COMMERCIAL TEMPERATURE RANGE (continued)

DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	ADDITIONAL FEATURES	PAGE NO.
GAS DISCHARGE DISPLAYS	HIGH-VOLTAGE BCD-TO-SEVEN-SEGMENT DECODER CATHODE DRIVERS	TTL	5 V	7	SN75480	N	• Outputs regulated to insure constant brightness • Blanking and ripple-blanking provisions • High off-state breakdown voltage (120 V typical) • Designed for seven segment displays such as Beckman and Panaplex II◇	9–13
		CMOS	Variable from 5 V to 15 V	7½	SN75580	N	Same features as the SN75480 plus: • Decimal point provided • Latches to hold BCD information • Lower supply power requirements • Higher output voltage breakdown capability	9–59
		TTL	Variable from 4.75 V to 15 V	7½	SN75584A	N		9–65
	ANODE DRIVER	MOS	V_{EE} = −55 V, V_{BB} = −18 V	6	SN75481	N	• 13-mA output capability • Designed for time-multiplexed displays such as Panaplex II◇	9–17
THERMAL PRINT DISPLAYS	THERMAL PRINTHEAD DRIVERS	TTL, CMOS	±5 V	6	SN75490	J,N	• Common strobe • 30-mA source, 50-mA sink capability	9–21
		MOS	5 V	7	SN75270	J,N	• Single ended, noninverting operation	9–5
VACUUM FLUORESCENT DISPLAYS	DRIVERS	CMOS	V_{CC1} = 12 V, V_{CC2} = 60 V	12	SN75510	N	• 12 drivers for dot-matrix or segmented displays • 60-V output and 25-mA input • Serial input • SN75511 has latched outputs for continuous display	9–51
				12	SN75511	N		9–55

◇Trademark of the Burroughs Corporation

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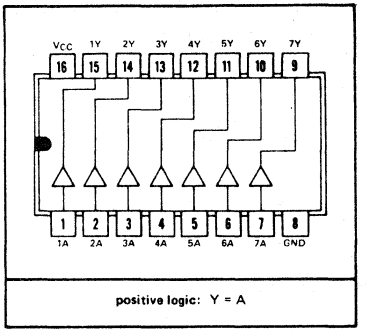
TYPE SN75270
7-UNIT MOS-TO-TTL CONVERTER AND THERMAL PRINTHEAD DRIVER ARRAY

BULLETIN NO. DL-S 7712061, SEPTEMBER 1973—REVISED APRIL 1977

- 7 Single-Ended Noninverting Drivers Per Package
- Inputs Compatible with MOS
- TTL-Compatible Outputs
- Single 5-V Supply

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

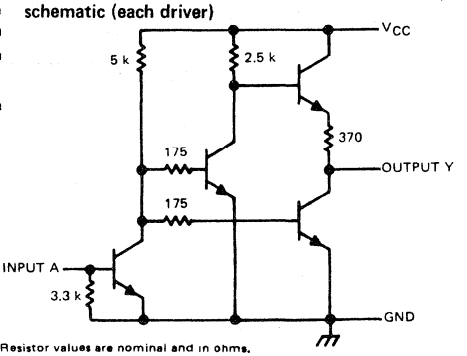


description

The SN75270 is a monolithic integrated circuit designed for use as a sense amplifier or thermal printhead driver. As a sense amplifier, the device can be used to convert from MOS to TTL levels. As a thermal printhead driver, this device is used with EPN3600-type thermal printheads.

The SN75270 is characterized for operation from 0°C to 70°C.

schematic (each driver)



Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input current	4 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input current, I_{IH}	0.5		2	mA
Low-level input current, I_{IL}	0		0.1	mA
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1. In the J package, SN75270 chips are glass-mounted.

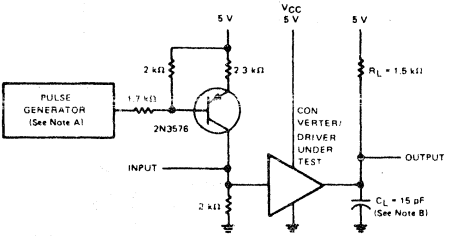
electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	V_{CC} = 4.75 V, I_{IH} = 500 µA, I_{OH} = −80 µA	2.4			V
V_{OL} Low-level output voltage	V_{CC} = 4.75 V, I_{IL} = 100 µA, I_{OL} = 3.2 mA			0.4	V
I_{OH} High-level output current	V_{CC} = 4.75 V, I_{IH} = 500 µA, V_O = 1 V	−5			mA
	V_{CC} = 5.25 V, I_{IH} = 500 µA, V_O = 0.25 V			−15	mA
I_{CCL} Total supply current, all outputs low	V_{CC} = 5 V; I_{IL} = 100 µA, I_O = 0		20	35	mA

switching characteristics, T_A = 25°C

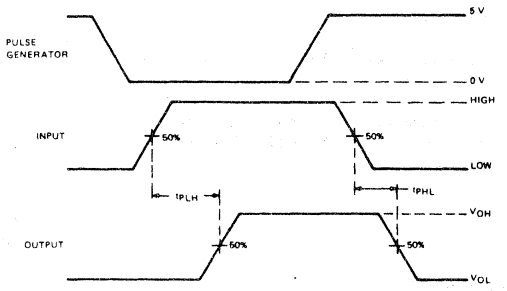
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	V_{CC} = 5 V, C_L = 15 pF,		30		ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 1.5 kΩ, See Figure 1		8		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

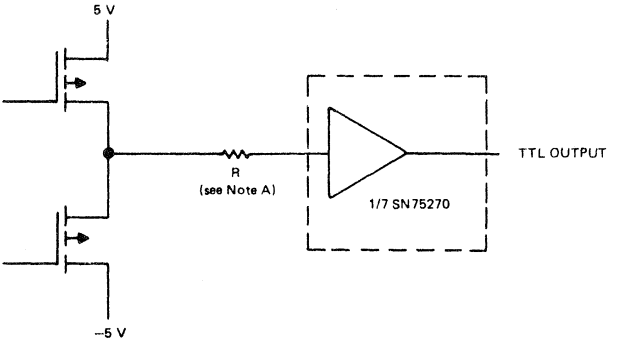
TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

TYPICAL APPLICATION DATA



Note A: $R = \dfrac{V_{OH} - V_{BE}}{I_{OH}}$

V_{OH} = High-level output voltage of MOS device
V_{BE} = Base-Emitter voltage of input transistor of SN75270
I_{OH} = High-level output current of MOS device

example: let $V_{OH} = 4$ V
$I_{OH} = 1$ mA
$V_{BE} = 0.7$ V

$$R = \frac{4 - 0.7}{1} \approx 3.3\ \text{k}\Omega$$

FIGURE 2–MOS TO SN75270 CONNECTION

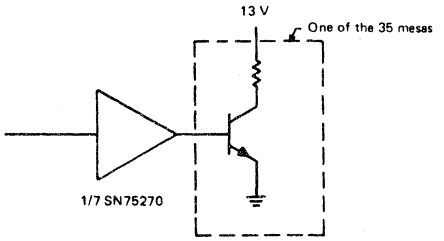


FIGURE 3–THERMAL PRINTHEAD DRIVER FOR THE EPN3600 THERMAL PRINTHEAD

TYPES SN55426B, SN55427B, SN75426B, SN75427B AC PLASMA DISPLAY DRIVERS

BULLETIN NO. DL-S 12499, MARCH 1979

- 90-V Output Swing
- CMOS-Compatible Inputs
- Quad Drivers with Independent Addressing of Each Gate for Serial or Parallel Applications
- High Data Input Impedance . . . 1 MΩ Typ
- 30-mA Clamp Diodes on Output

description

The SN55426B, SN55427B, SN75426B, and SN75427B are monolithic integrated-circuit plasma display drivers. The logic of the two drivers is complementary to permit controlled writing or erasing at a specified point on the display. The '426B noninverting pulser is normally near ground potential and is pulsed near V_{CC2}, while the '427B inverting pulser is normally near V_{CC2} potential and is pulsed near ground potential. The devices are designed to accept CMOS logic input signals and drive one display line per output.

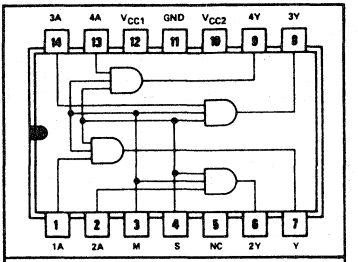
There are four gates per package with individual data inputs. Additionally, each device has a strobe and a multiplex input controlling all four gates. The devices require two power supplies, the logic section power supply V_{CC1}, and the high-voltage bias supply V_{CC2}. V_{CC2} controls the magnitude of the output swing.

Each output is designed to sustain 20-milliampere switching transients on the output. Each output is also protected by source and sink clamp diodes with 30-milliampere current capability. Each device is designed to be operated at 50 kilohertz but may be operated as high as 85 kilohertz.

The multiplex and strobe inputs (inputs M and S, respectively) act on all four gates simultaneously and aid in plasma panel design.

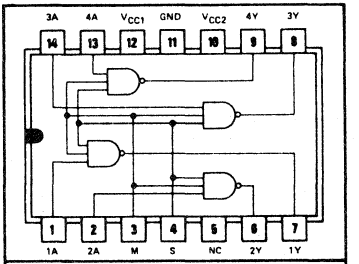
The SN55426B and SN55427B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75426B and SN75427B are characterized for operation from 0°C to 70°C.

SN55426B . . . J
SN75426B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \cdot M \cdot S$

SN55427B . . . J
SN75427B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot M \cdot S}$

NC—No internal connection

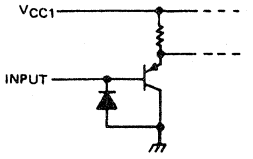
FUNCTION TABLE (EACH DRIVER)

INPUTS			OUTPUTS	
A	M	S	'426B	'427B
L	X	X	L	H
X	L	X	L	H
X	X	L	L	H
H	H	H	H	L

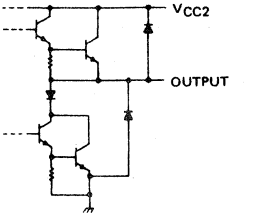
H=high level, L=low level, X=irrelevant

schematics of inputs and outputs

EQUIVALENT OF EACH A, M, OR S INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 95 V
Input voltage, V_I . . . . . 15 V
Continuous output current, I_O . . . . . 20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 800 mW
Operating free-air temperature range: SN55426B, SN55427B . . . . . −55°C to 125°C
SN75426B, SN75427B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	800 mW	8.2 mW/°C	52°C
N	800 mW	9.2 mW/°C	63°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10	12	14	V
Supply voltage, V_{CC2}	40	70	90	V
Strobe frequency	0		85	kHz
Data input frequency	0	50	85	kHz
Width of strobe pulse	1.5	5		μs
Operating free-air temperature, T_A	0		70	°C

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SN55426B, SN55427B electrical characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = −55°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{OH}	High-level output voltage		V_{IH} = 7V, V_{IL} = 3 V	I_O = −1 mA	V_{CC2}−4	V_{CC2}−1		V
				I_O = −15 mA	V_{CC2}−8	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 7 V, V_{IL} = 3 V	I_O = 1 mA		2	4	V
				I_O = 15 mA		3.5	8	
V_{OK}	Output clamp voltage		Output high,	I_O = 30 mA		V_{CC2}+0.8	V_{CC2}+2	V
			Output low,	I_O = −30 mA		−0.9	−2	
I_{IH}	High-level input current	A	V_{IH} = 12 V			12	60	μA
		M, S				50	200	
I_{CC1}	Supply current, logic section		V_{CC1} = 12 V,	All inputs at 12 V		10	15	mA
I_{CC2}	Supply current, output section		V_{CC2} = 90 V, No load	All outputs high		1.1	1.7	mA
				All outputs low		0.1	0.6	
$I_{CC1(av)}$	Average supply current, logic section		t_w = 5 μs,	f = 50 kHz,		10		mA
$I_{CC2(av)}$	Average supply current, output section		No load			1.3		mA

†All typical values are at 25°C.

SN75426B, SN75427B electrical characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = 0°C to 70°C (unless otherwise noted)

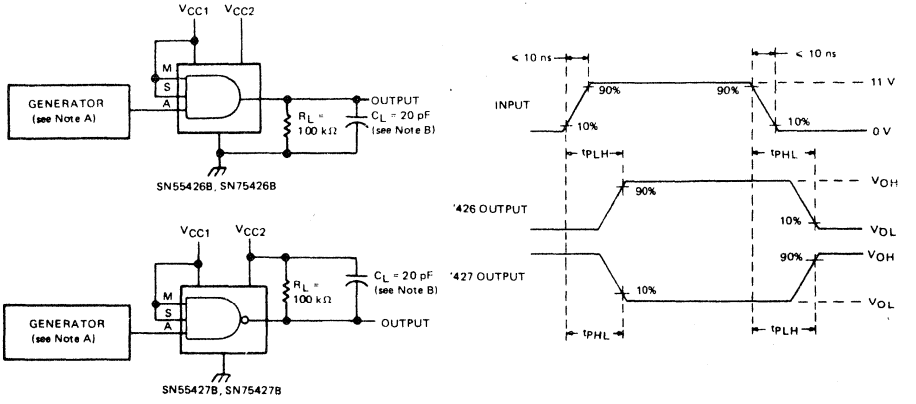
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{OH}	High-level output voltage		V_{IH} = 7V, V_{IL} = 3 V	I_O = −1 mA	V_{CC2}−3	V_{CC2}−1		V
				I_O = −15 mA	V_{CC2}−6	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 7 V, V_{IL} = 3 V	I_O = 1 mA		2	3	V
				I_O = 15 mA		3.5	6	
V_{OK}	Output clamp voltage		Output high,	I_O = 30 mA		V_{CC2}+0.8	V_{CC2}+1.5	V
			Output low,	I_O = −30 mA		−0.9	−1.5	
I_{IH}	High-level input current	A	V_{IH} = 12 V			12	30	μA
		M, S				50	100	
I_{CC1}	Supply current, logic section		V_{CC1} = 12 V,	All inputs at 12 V		10	14	mA
I_{CC2}	Supply current, output section		V_{CC2} = 90 V, No load	All outputs high		1.1	1.4	mA
				All outputs low		0.1	0.5	
$I_{CC1(av)}$	Average supply current, logic section		t_w = 5 μs, No load	f = 50 kHz,		10		mA
$I_{CC2(av)}$	Average supply current, output section					1.3		mA

† All typical values are at 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 20 pF, R_L = 100 kΩ, See Figure 1		0.7	1.2	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.3	0.8	μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 50 kHz, t_w = 5 μs.
B. C_L includes probe and jig capacitance.

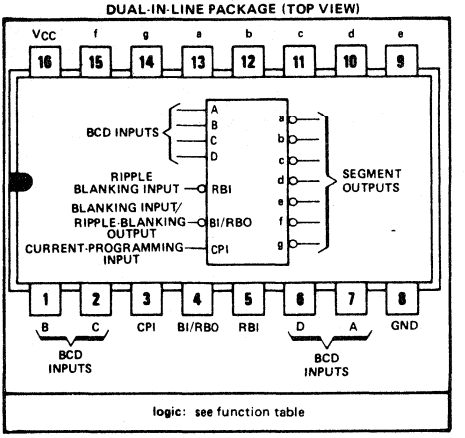
FIGURE 1–SWITCHING TIMES

TYPE SN75480 HIGH-VOLTAGE 7-SEGMENT DECODER/CATHODE DRIVER

BULLETIN NO. DL-S 7712244, MAY 1975—REVISED AUGUST 1977

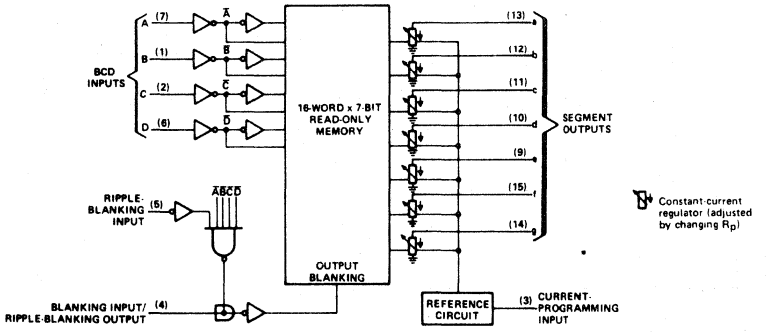
- Plug-In Replacement for National Semiconductor DS8880
- Adjustable Output Current from 0.2 mA to 1.5 mA
- High Off-State Output Breakdown Voltage (120 Volts Typical)
- Outputs Regulated to Ensure Constant Brightness
- Blanking and Ripple-Blanking Provisions
- Low Power Dissipation
- TTL-Compatible Inputs
- Single 5-V Supply

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

functional block diagram



description

The SN75480 is designed to decode four lines of BCD input and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. The design employs a 112-bit read-only memory that provides BCD-input-to-full-hexadecimal decoding by switching current sinks on or off in accordance with the function table.

The output current into the current sink is adjusted by connecting an external program resistor (R_P) from V_{CC} to the current programming input in accordance with the programming curve, Figure 1. This adjustment can vary the output sink current from nominally 0.2 milliamperes to 1.5 milliamperes in order to drive various tube types or to permit multiplex operation. The sink current for the other segments is proportioned to the b-segment current to provide even illumination of all segments. Each sink output is regulated to ensure a constant brightness of the display with a fluctuating supply voltage. Typically the on-state output current varies 1% for an output voltage change of 3 to 50 volts. The off-state voltage applied to these current sinks can vary from 3 volts to at least 80 volts.

The blanking input provides unconditional blanking of any output display, while the $\overline{A}$ through $\overline{D}$ inputs into the blanking circuit allow simple leading or trailing-zero blanking.

†Trademark of Burroughs Corporation.

FUNCTION TABLE

SEGMENT IDENTIFICATION

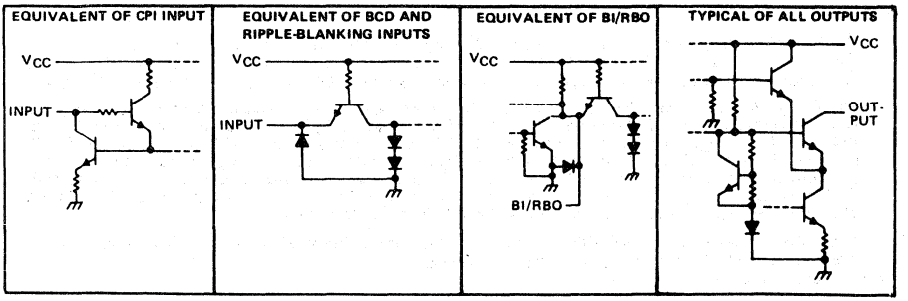
DECIMAL OR FUNCTION	INPUTS					BI/RBO	SEGMENT OUTPUTS							DISPLAY
	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	0
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	2
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	3
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	4
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	5
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	6
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	7
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	8
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	9
10	X	H	L	H	L	H	ON	ON	ON	OFF	ON	ON	ON	A
11	X	H	L	H	H	H	OFF	OFF	ON	ON	ON	ON	ON	b
12	X	H	H	L	L	H	ON	OFF	OFF	ON	ON	ON	OFF	C
13	X	H	H	L	H	H	OFF	ON	ON	ON	ON	OFF	ON	d
14	X	H	H	H	L	H	ON	OFF	OFF	ON	ON	ON	ON	E
15	X	H	H	H	H	H	ON	OFF	OFF	OFF	ON	ON	ON	F
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
RBI	L	L	L	L	L	L†	OFF	OFF	OFF	OFF	OFF	OFF	OFF	

H = high level, L = low level, X = irrelevant

†BI/RBO is wire-AND logic serving as a blanking input (BI) and/or ripple-blanking output (RBO). When RBI and inputs A, B, C, and D are all low, all segment outputs go off and RBO goes to a low-level (response condition).

9

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: All inputs except BI/RBO . . . . . 6 V
BI/RBO . . . . . V_{CC}
On-state output voltage . . . . . 55 V
Continuous on-state segment output current . . . . . 2.3 mA
Peak transient on-state segment output current (see Note 2) . . . . . 50 mA
Continuous total dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In all applications, peak transient segment current must be limited to 50 mA. This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (See Figure 4).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage			80	V
On-state output voltage	3		50	V
Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 5.25 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = 4.75 V, I_{OH} = −200 μA		2.4	3.0		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.17	0.4	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI/RBO at 0 V, I_O = 250 μA		80	120		V
$I_{O(off)}$	Off-state output current	a thru g	BI/RBO at 0 V, V_O = 75 V			0.003	3	μA
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 5 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18.1 kΩ	0.18	0.20	0.22	mA
				R_p = 7.03 kΩ	0.45	0.50	0.55	
				R_p = 3.4 kΩ	0.9	1.0	1.1	
				R_p = 2.2 kΩ	1.35	1.5	1.65	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 5 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
I_I	Input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 5.5 V			7	400	μA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 2.4 V			6	40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 0.4 V			−0.4	−0.6	mA
		BI/RBO				−1.5	−2	
I_{CC}	Supply current		V_{CC} = 5.25 V, All inputs at 0 V, R_p = 2.2 kΩ			27	43	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.4	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.4	10	
t_{off}	Turn-off time of segment outputs from BI/RBO		0.4	10	µs
t_{on}	Turn-on time of segment outputs from BI/RBO		0.4	10	
t_{off}	Turn-off time of segment outputs from RBI		0.4	10	µs
t_{on}	Turn-on time of segment outputs from RBI		0.7	10	
t_{PLH}	Propagation delay time, low-to-high-level RBO from RBI		0.4	10	µs
t_{PHL}	Propagation delay time, high-to-low-level RBO from RBI		0.4	10	

TYPICAL CHARACTERISTICS

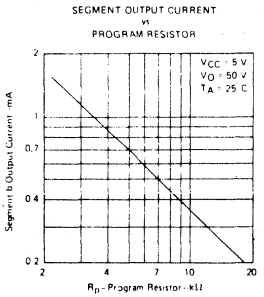


FIGURE 1

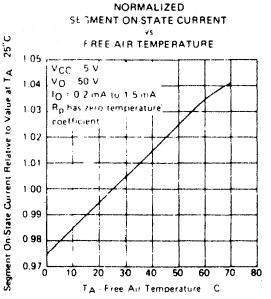


FIGURE 2

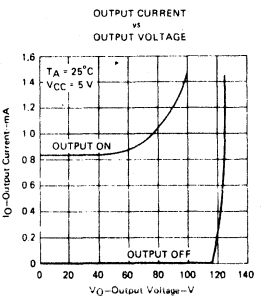


FIGURE 3

TYPICAL APPLICATION DATA

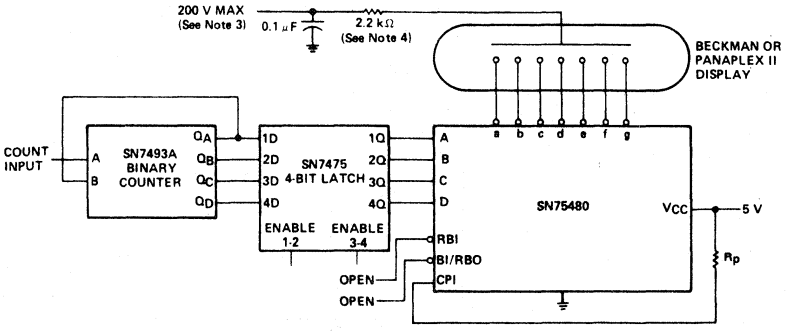


FIGURE 4–HEXADECIMAL DISPLAY

NOTES: 3. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 55 V and 80 V, respectively, at the outputs of the SN75480.

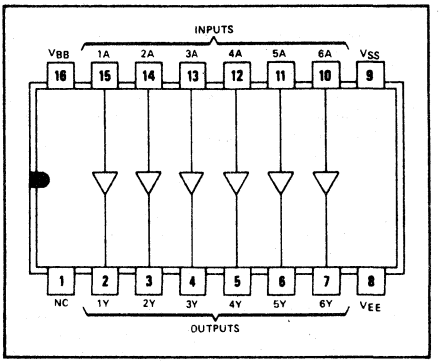
4. In all applications, peak transient segment current must be limited to 50 mA. This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

TYPE SN75481
ANODE DRIVERS FOR GAS DISCHARGE DISPLAYS

BULLETIN NO. DL-S 7512514, APRIL 1975

- MOS-Compatible Inputs
- Designed for Use with Panaplex II† Displays
- 55-Volt Operation
- 13-mA Output Capability

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection.

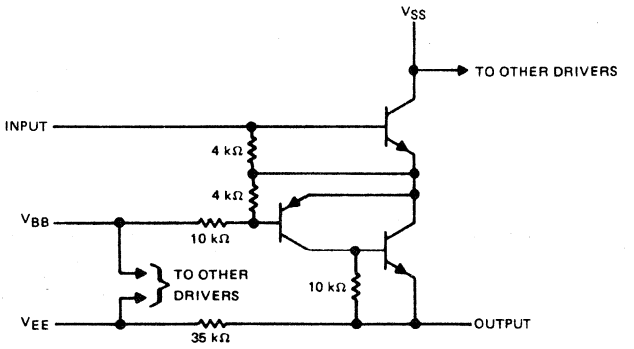
description

The SN75481 is a hex digit driver designed to be used as an anode driver for Panaplex II† gas discharge displays. The guaranteed 55-volt minimum breakdown voltage, MOS compatible inputs, and six drivers per package make it ideally suited for time-multiplexed calculator displays.

When the input is open or low ($\approx V_{BB}$), the output will be off and at approximately V_{EE}. When the input is high ($\approx V_{SS}$), the output will be on and at approximately $V_{SS}-2$ volts. Each output is designed to supply up to 13 milliamperes when in the on state.

The SN75481 is characterized for operation from 0°C to 70°C.

schematic (each driver)



†Trademark of Burroughs Corporation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{BB} (see Note 1)	−25 V
Supply voltage, V_{EE}	−60 V
Input voltage	V_{BB}
Continuous output current	−20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 2-1.

electrical characteristics over recommended operating free-air temperature range, V_{SS} = 0, V_{BB} = −18 V, V_{EE} = −55 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(on)}$	On-state output voltage	V_I = V_{SS} thru 1 kΩ, V_{BB} = −9 V, I_O = −12 mA	0		−3.5	V
$V_{O(off)}$	Off-State output voltage	I_{IL} = 100 μA, V_{BB} = −9 V, I_O = 0	−53		−55	V
I_{IH}	High-level input current	V_I = V_{SS} thru 100 Ω, I_O = −12 mA			1.5	mA
I_{BB}	Supply current from V_{BB}	One input to V_{SS} thru 100 Ω, All other inputs open, I_O = −12 mA			−3.5	mA
I_{EE}	Supply current from V_{EE}	One input to V_{SS} thru 100 Ω, All other inputs and all outputs open			−3	mA
I_{SS}	Supply current from V_{SS}	One input to V_{SS} thru 1 kΩ, All other inputs open, I_O = −12 mA			20	mA

9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

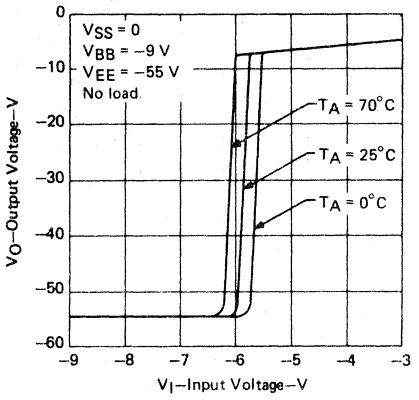


FIGURE 1

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

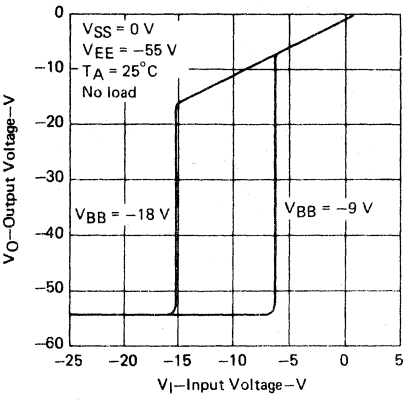


FIGURE 2

OUTPUT VOLTAGE
vs
INPUT CURRENT

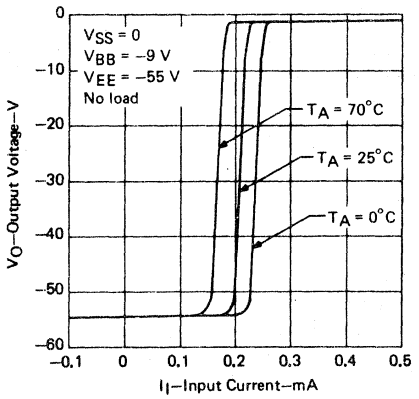


FIGURE 3

ON-STATE OUTPUT VOLTAGE
vs
OUTPUT CURRENT

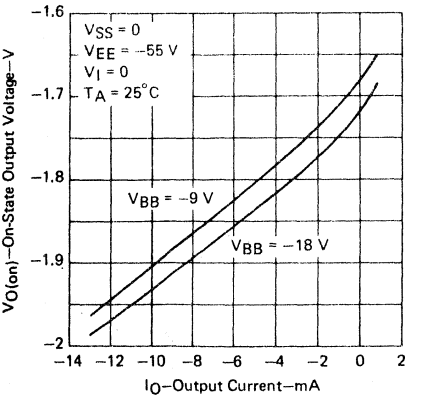


FIGURE 4

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

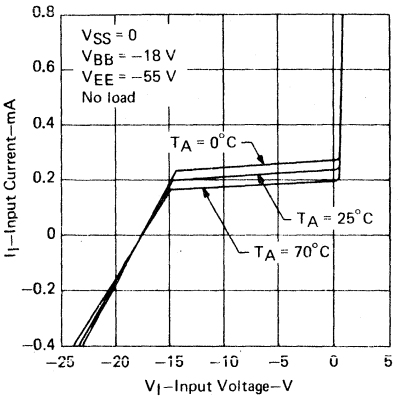


FIGURE 5

INPUT CURRENT
vs
OUTPUT CURRENT

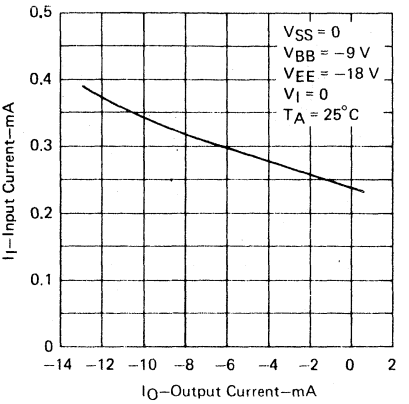
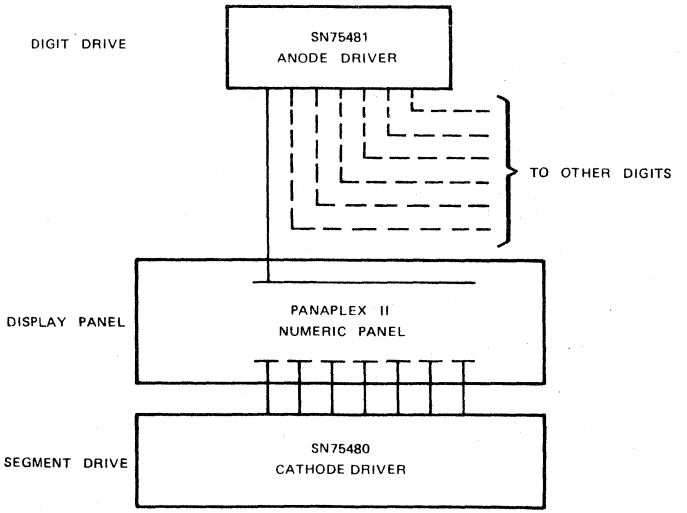


FIGURE 6

TYPICAL APPLICATION DATA



9

TYPE SN75490
THERMAL PRINTHEAD DRIVER

BULLETIN NO. DL-S 7712513, MAY 1977

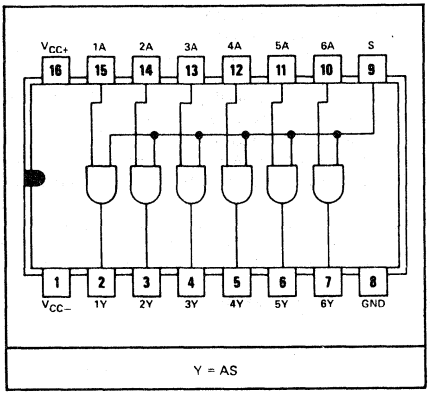
- Inputs Compatible with TTL and 5-V CMOS
- 30-mA Source Current Capability
- 50-mA Sink Current Capability
- Standard Supply Voltages . . . ±5 V
- Six Positive-AND Drivers per Package
- Common Strobe

description

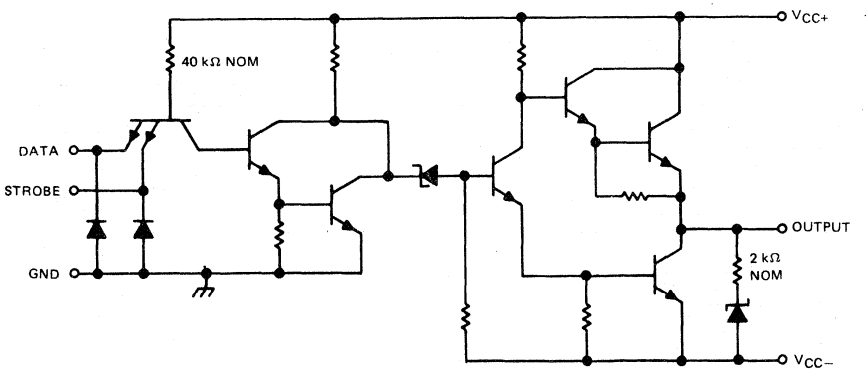
These circuits are designed to drive many of the popular thermal printheads including the EPN5200 and EPN3620. The SN75490 features six AND drivers with common strobe. Each driver has a totem-pole output with a nominal voltage range of −4.75 V to 3.5 V.

The SN75490 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-} (see Note 1)	−7 V
High-level output current	−40 mA
Low-level output current	60 mA
Input voltage	5.25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which begins on page 2-1. In the J package, SN75490 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level output current, I_{OH}			−30	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.7	V
V_{IK}	Input clamp voltage		V_{CC+} = 4.75 V,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{IH} = 2 V,	V_{CC+} = 4.75 V,	I_{OH} = −30 mA	2.75			V
				V_{CC+} = 5 V,	I_{OH} = −30 mA	3	3.5		
V_{OL}	Low-level output voltage (see Note 3)		V_{IL} = 0.7 V	V_{CC-} = −4.75 V,	I_{OL} = 50 mA			−4.15	V
				V_{CC-} = −5 V,	I_{OL} = 50 mA		−4.75	−4.4	
I_{IH}	High-level input current	A inputs	V_I = 5 V					0.05	mA
		S input						0.3	
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V					−0.18	mA
		S input						−1.1	
$I_{CC+}(H)$	Supply current from V_{CC+}, all outputs high		$V_{CC\pm}$ = ±5.25 V, V_I = 5 V				30	43	mA
$I_{CC-}(H)$	Supply current from V_{CC-}, all outputs high						−6.5	−10	
$I_{CC+}(L)$	Supply current from V_{CC+}, all outputs low		$V_{CC\pm}$ = ±5.25 V, V_I = 0.4 V				40	58	mA
$I_{CC-}(L)$	Supply current from V_{CC-}, all outputs low						−40	−58	

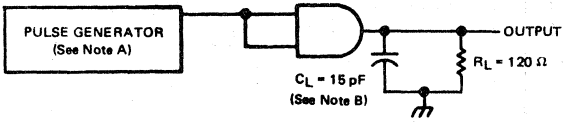
†All typical values are at $V_{CC\pm}$ = ±5 V, T_A = 25°C.

NOTE 3: The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −4.4 V is a maximum, the typical value is a more negative voltage.

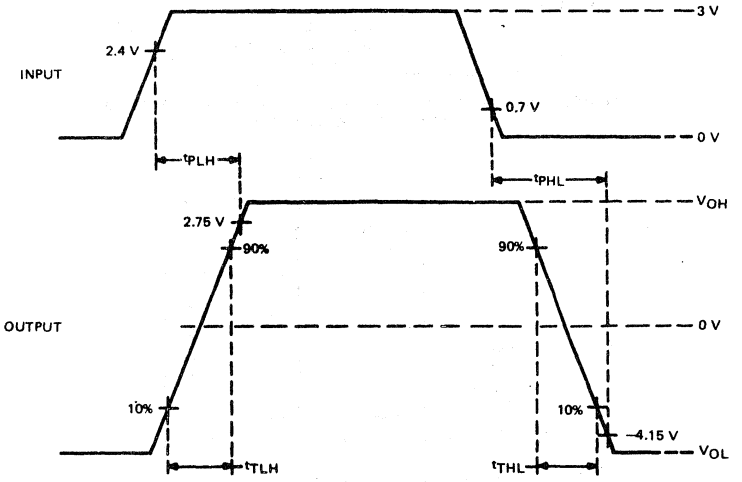
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 120 Ω, See Figure 1		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output			50		ns
t_{TLH}	Transition time, low-to-high-level output			8		ns
t_{THL}	Transition time, high-to-low-level output			8		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, f = 100 kHz, t_w = 1 μs, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

FIGURE 1—SWITCHING TIMES

9

TYPICAL APPLICATION DATA

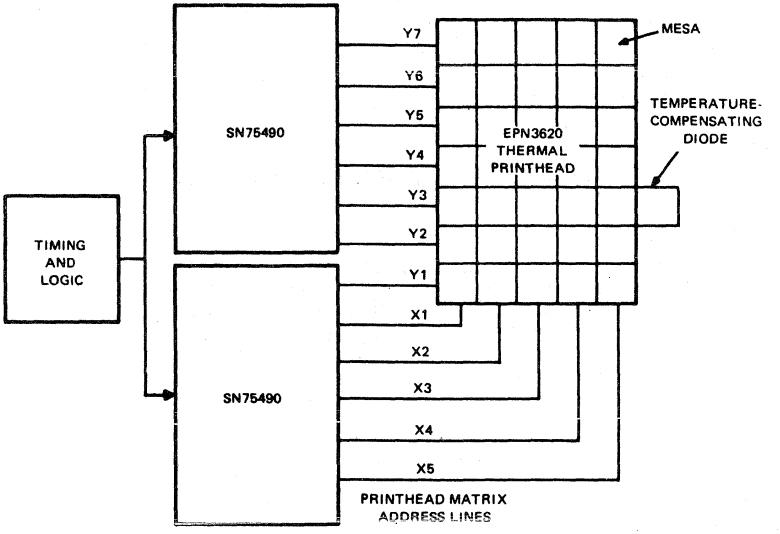


FIGURE 2–PRINTER SYSTEM BLOCK DIAGRAM USING SN75490 DRIVERS AND EPN3620 THERMAL PRINTHEAD

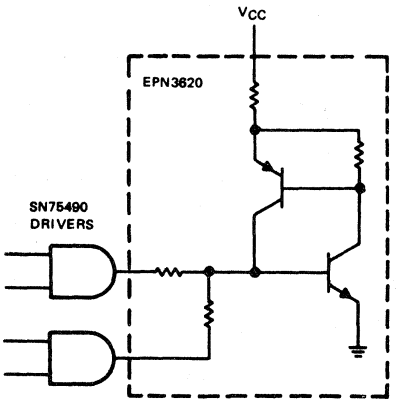


FIGURE 3–DIAGRAM SHOWING THE CONNECTION WITH ONE OF THE MESAS OF THE EPN3620

For a detailed description of the EPN3620 thermal printhead, see data sheet DL-S 7712505 and Texas Instruments Application Report, Bulletin CA-190.

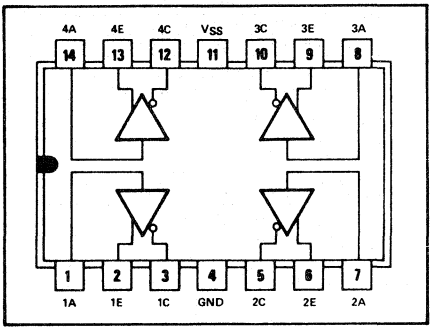
TYPES SN75491, SN75491A, SN75492, SN75492A MOS-TO-LED DRIVERS

BULLETIN NO. DL-S 7711769, OCTOBER 1972–REVISED MAY 1977

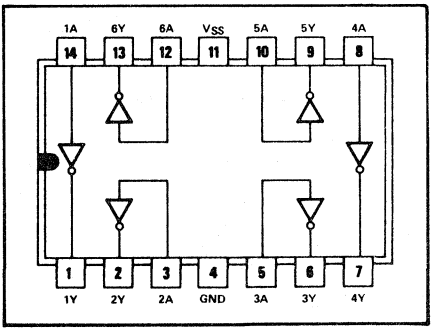
QUAD SEGMENT DRIVER AND HEX DIGIT DRIVER FOR INTERFACING BETWEEN MOS AND LIGHT-EMITTING-DIODE (LED) DISPLAYS

- 50-mA Source or Sink Capability ('491, '491A)
- 250-mA Sink Capability ('492, '492A)
- Rated for 10-V Operation ('491, '492)
- Rated for 20-V Operation ('491A, '492A)
- Low Input Current for MOS Compatability
- Low Standby Power
- High-Gain Darlington Circuits

SN75491, SN75491A
N DUAL-IN-LINE PACKAGE (TOP VIEW)



SN75492, SN75492A
N DUAL-IN-LINE PACKAGE (TOP VIEW)



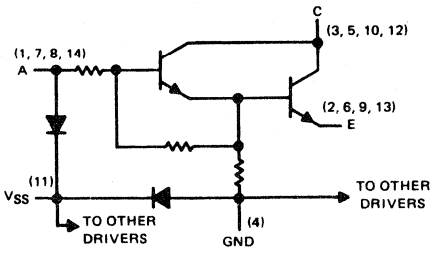
description

The SN75491, SN75491A, SN75492, and SN75492A are monolithic integrated circuits designed to be used together with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. This time-multiplexed system, which uses a segment-address-and-digit-scan method of LED drive, minimizes the number of drivers required.

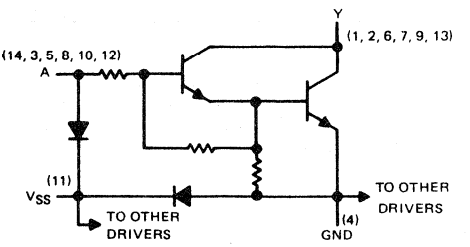
The SN75491 and SN75491A are quadruple segment drivers. The SN75492 and SN75492A are hex digit drivers. The SN75491 and SN75492 are characterized for operation to 10 volts. The SN75491A and SN75492A are characterized for operation to 20 volts.

schematic

SN75491, SN75491A (each driver)



SN75492, SN75492A (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN75491	SN75491A	SN75492	SN75492A	UNIT
Input voltage range (see Note 1)		−5 to V_{SS}	−5 to V_{SS}	−5 to V_{SS}	−5 to V_{SS}	V
Collector (output) voltage (see Note 2)		10	20	10	20	V
Collector (output)-to-input voltage		10	20	10	20	V
Emitter-to-ground voltage (V_I > 5 V)		10	20			V
Emitter-to-input voltage		5	5			V
Voltage at V_{SS} terminal with respect to any other device terminal		10	20	10	20	V
Collector (output) current	each collector (output)	50	50	250	250	mA
	all collectors (outputs)	200	200	600	600	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)		800	800	800	800	mW
Operating free-air temperature range		0 to 70	0 to 70	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds		260	260	260	260	°C

NOTES: 1. The input is the only device terminal that may be negative with respect to ground.
2. Voltage values are with respect to network ground terminal unless otherwise noted.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1.

'491, '491A electrical characteristics, V_{SS} = 10 V for SN75491, V_{SS} = 20 V for SN75491A, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{CE(on)}$	On-state collector-emitter voltage	Input = 8.5 V through 1 kΩ, V_E = 5 V, I_C = 50 mA, T_A = 25°C			0.9	1.2	V
		Input = 8.5 V through 1 kΩ, V_E = 5 V, I_C = 50 mA				1.5	
$I_{C(off)}$	Off-state collector current	V_C = V_{SS}, V_E = 0,	I_I = 40 μA			100	μA
		V_C = V_{SS}, V_E = 0,	V_I = 0.7 V			100	
I_I	Input current at maximum input voltage	V_I = V_{SS}, V_E = 0, I_C = 20 mA	'491		2.2	3.3	mA
			'491A		4.7	6.5	
I_E	Emitter reverse current	V_I = 0, V_E = 5 V,	I_C = 0			100	μA
I_{SS}	Current into V_{SS} terminal					1	mA

'492, '492A electrical characteristics, V_{SS} = 10 V for SN75492, V_{SS} = 20 V for SN75492A, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	Input = 6.5 V through 1 kΩ, I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		Input = 6.5 V through 1 kΩ, I_{OL} = 250 mA				1.5	
I_{OH}	High-level output current	V_{OH} = V_{SS}, I_I = 40 μA				200	μA
		V_{OH} = V_{SS}, V_I = 0.5 V				200	
I_I	Input current at maximum input voltage	V_I = V_{SS}, I_{OL} = 20 mA	'492		2.2	3.3	mA
			'492A		4.7	6.5	
I_{SS}	Current into V_{SS} terminal					1	mA

† All typical values are at T_A = 25°C

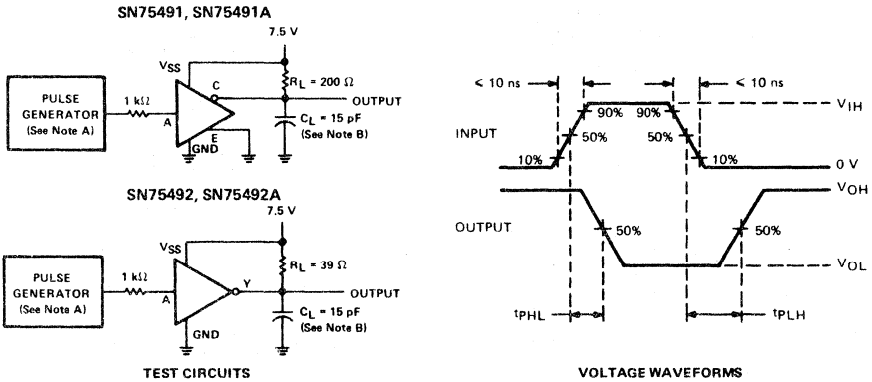
SN75491, SN75491A switching characteristics, V_{SS} = 7.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output (collector)	V_{IH} = 4.5 V, V_E = 0,		100		ns
t_{PHL}	Propagation delay time, high-to-low-level output (collector)	R_L = 200 Ω, C_L = 15 pF		20		ns

SN75492, SN75492A switching characteristics, V_{SS} = 7.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{IH} = 7.5 V, R_L = 39 Ω,		300		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF		30		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

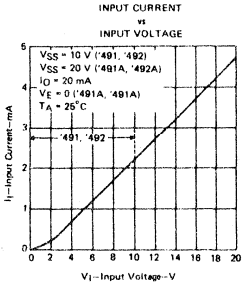


FIGURE 2

TYPICAL CHARACTERISTICS

SN75491, SN75491A
COLLECTOR CURRENT
vs
INPUT CURRENT

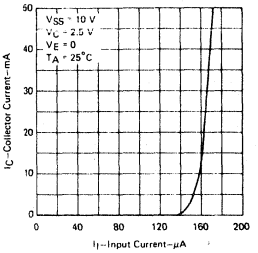


FIGURE 3

SN75492, SN75492A
OUTPUT CURRENT
vs
INPUT CURRENT

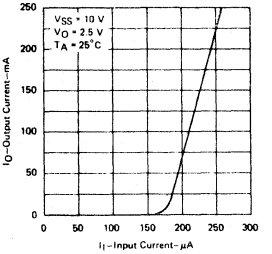


FIGURE 4

SN75491, SN75491A
COLLECTOR CURRENT
vs
INPUT VOLTAGE

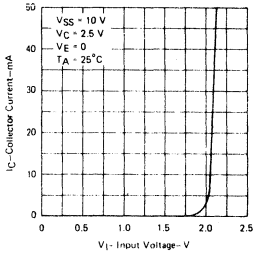


FIGURE 5

SN75492, SN75492A
OUTPUT CURRENT
vs
INPUT VOLTAGE

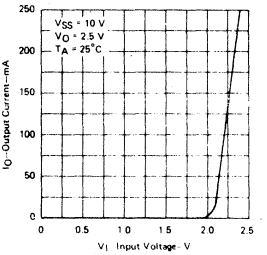


FIGURE 6

SN75491, SN75491A
ON-STATE COLLECTOR EMITTER VOLTAGE
vs
COLLECTOR CURRENT

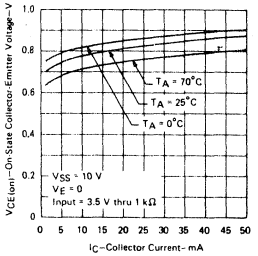


FIGURE 7

SN75492, SN75492A
LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

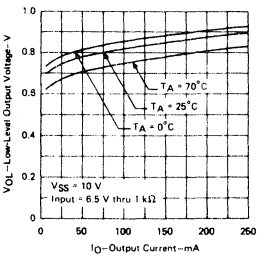


FIGURE 8

TYPICAL APPLICATION DATA

Figure 9 is an example of time multiplexing the individual digits in a visible display to minimize display circuitry. Up to twelve digits, each of which use a seven-segment display with decimal point, may be displayed using only two SN75491 and two SN75492 drivers.

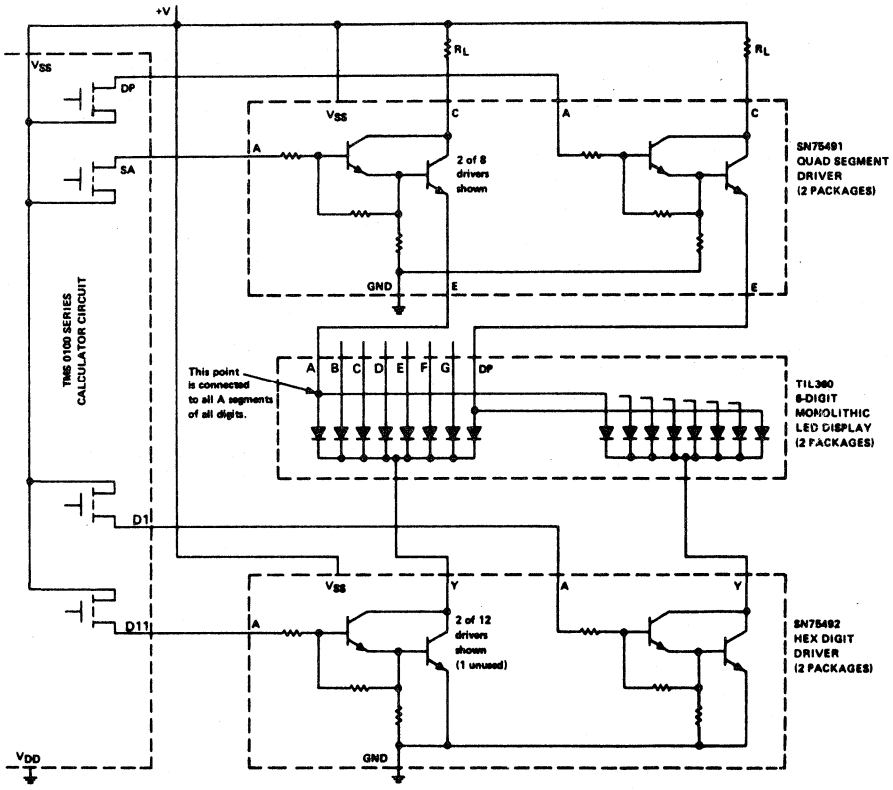


FIGURE 9—INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY

9

TYPICAL APPLICATION DATA

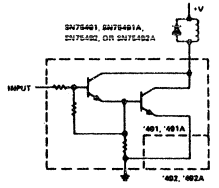


FIGURE 10–QUAD OR HEX RELAY DRIVER

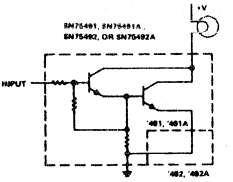


FIGURE 11–QUAD OR HEX LAMP DRIVER

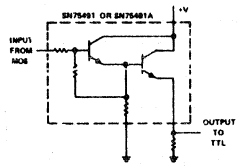


FIGURE 12–MOS-TO-TTL LEVEL SHIFTER

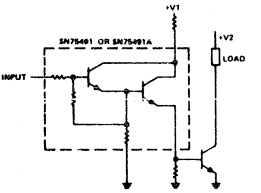
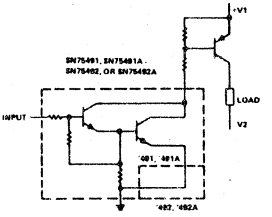


FIGURE 13–QUAD HIGH-CURRENT N-P-N TRANSISTOR DRIVER



NOTE A: This circuit may be used as a digit driver for common-anode LED displays.

FIGURE 14–QUAD OR HEX HIGH-CURRENT P-N-P TRANSISTOR DRIVER

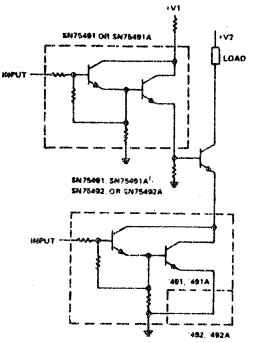


FIGURE 15–BASE/EMITTER SELECT N-P-N TRANSISTOR DRIVER

TYPICAL APPLICATION DATA

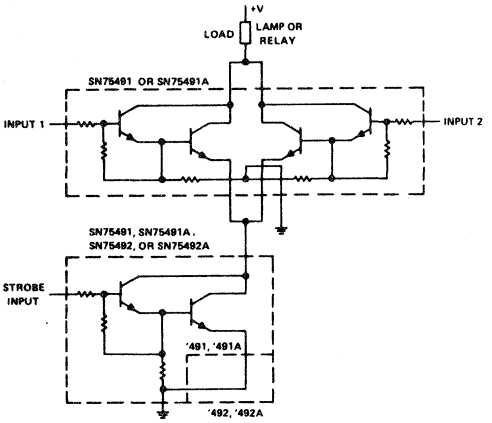


FIGURE 16–STROBED "NOR" DRIVER

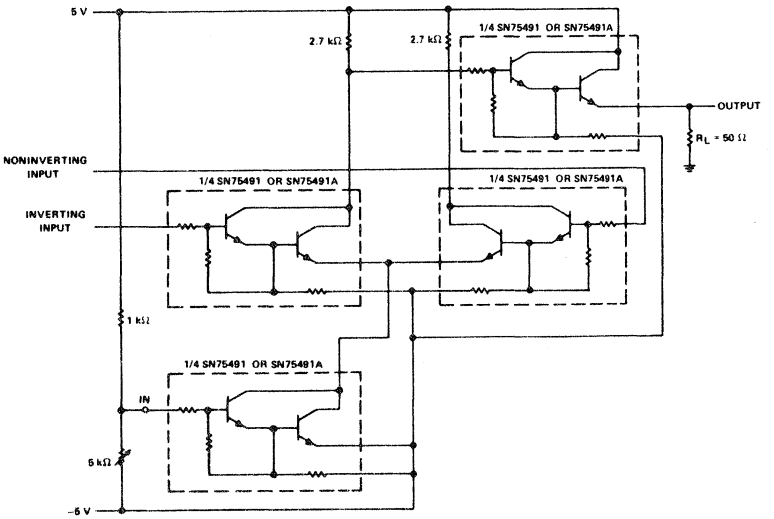


FIGURE 17–SN75491/SN75491A USED AS AN INTERFACE CIRCUIT BETWEEN THE BALANCED 30-MHz OUTPUT OF AN RF AMPLIFIER AND A COAXIAL CABLE

TYPES SN75493, SN75494
MOS-TO-LED SEGMENT AND DIGIT DRIVERS

BULLETIN NO. DL-S 7712454, MAY 1977

- Low Input Current for MOS Compatibility
- Low-Voltage Operation
- Low Standby Power
- Display Blanking Capability

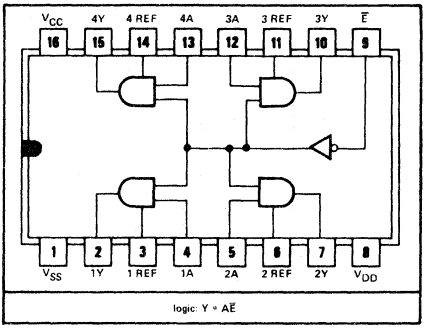
additional SN75493 features

- 50-mA Source Capability
- Output Current Regulation
- Quad High-Gain Circuits

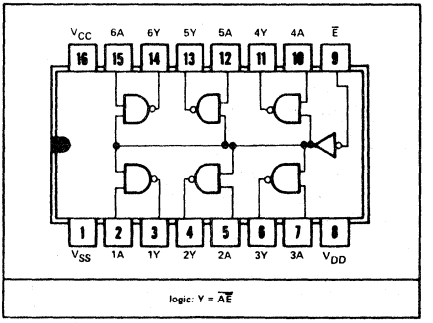
additional SN75494 features

- 250-mA Sink Capability
- Low-Voltage Saturating Outputs
- Hex High-Gain Circuits

SN75493
N DUAL-IN-LINE PACKAGE (TOP VIEW)



SN75494
N-DUAL-IN-LINE PACKAGE (TOP VIEW)

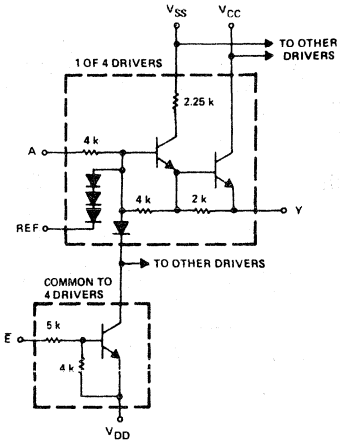


description

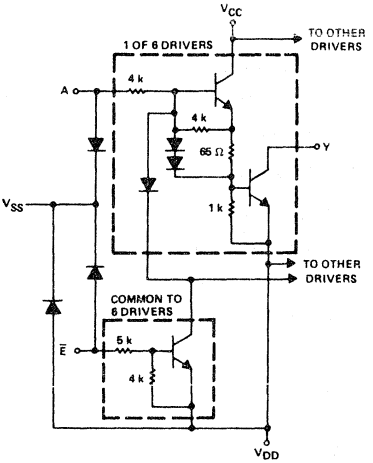
The SN75493 and SN75494 are designed to be used to interface between MOS integrated circuits and LEDs in serially addressed multidigit displays. These two devices are similar in operation to the SN75491 and SN75492, but have several advantages over those earlier circuits. The SN75493 and SN75494 can be operated at lower supply voltages and, therefore, reduce power consumption. The SN75493 is designed to give relatively constant current through an external resistor, independent of supply voltage. The enable ($\overline{E}$) pin of each circuit is intended for use as a blanking input.

schematics

75493
SEGMENT DRIVER



75494
DIGIT DRIVER



NOTES: A. The V_{SS} terminal of the SN75494 must be connected to the most positive voltage that is applied to the device.
B. Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75493	SN75494	UNITS
Supply voltage, V_{CC} (see Note 1)	10	10	V
Supply voltage, V_{SS}	10	10	V
Input voltage	V_{SS}	V_{SS}	V
Off-state output voltage		10	V
Input-to-reference voltage	8.8		V
Continuous output current (each driver)	50	250	mA
Continuous V_{DD} current		600	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800	800	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

NOTES: 1. All voltage values are with respect to the most negative device terminal, V_{DD}, unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 2-1.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.2	8.8	V
Supply voltage, V_{SS}	6.5	8.8	V
Operating free-air temperature, T_A	0	70	°C

SN75493 electrical characteristics, V_{CC} = 8.8 V, V_{SS} = 8.8 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current	A input	A at 8.8 V, REF at 0 V, Y to 0 V thru 50 Ω	$\overline{E}$ at 0 V		1.7	2.5	mA
				$\overline{E}$ at 8.8 V		2	3	
		$\overline{E}$ input	A at 0 V, $\overline{E}$ at 8.8 V, REF at 0 V, Y at 0 V			1.6	2.5	
$I_{O(on)}$	On-state output current		V_{CC} = 3.2 V, V_{SS} = 6.5 V, A to 6.5 V thru 1 kΩ, REF at 2.15 V,	$\overline{E}$ to 8.8 V thru 100 kΩ, Y to 2.15 V thru 50 Ω	−8	−13		mA
$I_{O(off)}$	Off-state output current (from Y to V_{DD})		A to 8.8 V thru 100 kΩ, REF at 0 V,	$\overline{E}$ at 0 V, Y at 0 V		−100	−300	μA
			A at 8.8 V, REF at 0 V,	$\overline{E}$ to 6.5 V thru 1 kΩ, Y at 0 V		−200	−1000	
$V_{O(on)}$	On-state output voltage		V_{CC} = 3.2 V, V_{SS} = 6.5 V, A to 6.5 V thru 1 kΩ, REF open,	$\overline{E}$ to 8.8 V thru 100 kΩ, $I_{O(on)}$ = −50 mA	2.5	2.9		V
I_{CC}	Current into V_{CC} terminal		All A inputs at 0 V, REF at 0 V,	$\overline{E}$ at 0 V, Y at 0 V		10	500	μA
I_{SS}	Current into V_{SS} terminal		All A inputs at 8.8 V, REF at 2.15 V,	$\overline{E}$ to 8.8 V thru 100 kΩ, Y to 0 V thru 50 Ω		2	8	mA
			V_{CC} = 0 V, REF at 0 V,	All A inputs at 0 V, $\overline{E}$ at 0 V, Y at 0 V		10	500	μA

SN75494 electrical characteristics, V_{CC} = 8.8 V, V_{SS} = 8.8 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current	A input	A at 8.8 V,	$\overline{E}$ at 8.8 V		2	3	mA
			V_{CC} = 3.2 V, A at 8.8 V,	$\overline{E}$ to 8.8 V thru 100 kΩ,		1.8	2.5	
		$\overline{E}$ input	V_{CC} = 3.2 V,	$\overline{E}$ at 8.8 V		1.6	2.5	
$I_{O(off)}$	Off-state output current (from Y to V_{DD})		A to 8.8 V thru 100 kΩ, Y at 10 V	$\overline{E}$ at 0 V,		1	200	μA
			A at 8.8 V, Y at 10 V	$\overline{E}$ to 6.5 V thru 1 kΩ,		1	100	
$V_{O(on)}$	On-state output voltage		V_{CC} = 3.2 V, V_{SS} = 6.5 V, $\overline{E}$ to 6.5 V thru 1 kΩ,	A to 6.5 V thru 1 kΩ, I_{OL} = 250 mA		0.25	0.4	V
I_{CC}	Current into V_{CC} terminal		One A input to 8.8 V thru 100 kΩ, All other A inputs at 0 V	$\overline{E}$ at 0 V,		10	500	μA
			One A input at 8.8 V, All other A inputs at 0 V	$\overline{E}$ to 6.5 V thru 1 kΩ,		60	500	
			One A input at 8.8 V, All other A inputs at 0 V	$\overline{E}$ at 0 V,		11	20	mA
I_{SS}	Current into V_{SS} terminal		V_{CC} = 3.2 V,	$\overline{E}$ at 0 V, All A inputs at 0 V		10	500	μA

†All typical values are at T_A = 25°C.

9

TYPICAL APPLICATION DATA

Figure 1 is an example of time multiplexing the individual digits in a visible display to minimize display circuitry. Up to twelve digits, each of which use a seven-segment display with decimal point, may be displayed using only two SN75493 and two SN75494 drivers.

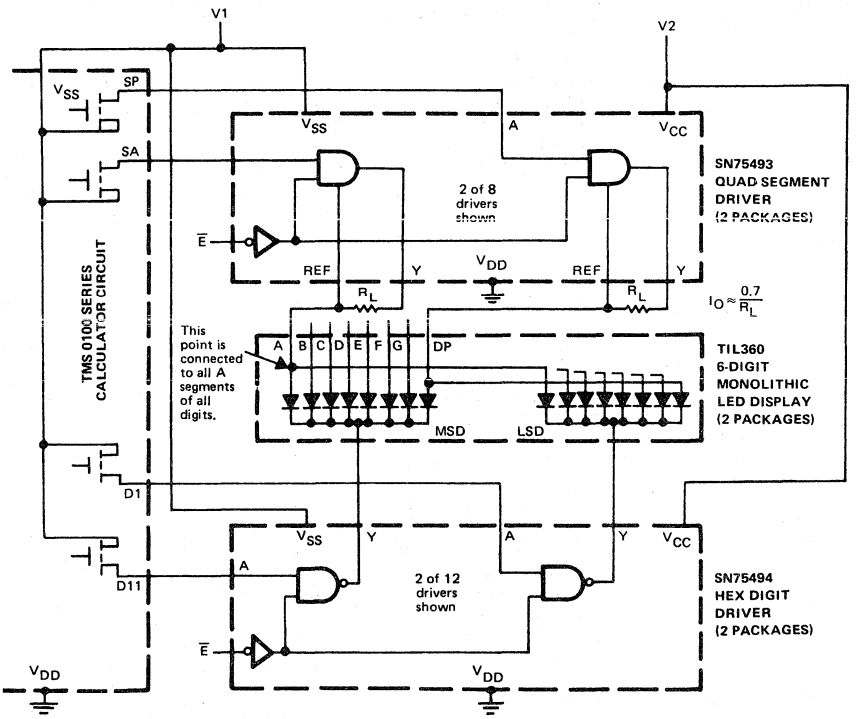


FIGURE 1–INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTIDIGIT DISPLAY

NOTE: Operating ranges of V1 and V2 are 6.5 V to 8.8 V and 3.2 V to 8.8 V, respectively.

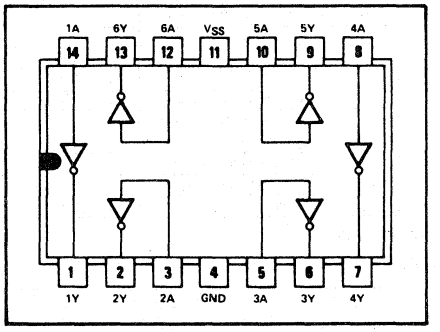
TYPES SN75496, SN75496A
HEX TTL-TO-LED DIGIT DRIVERS

BULLETIN NO. DL-S 12585, FEBRUARY 1978

HEX DIGIT DRIVER FOR INTERFACING BETWEEN TTL AND LIGHT-EMITTING-DIODE (LED) DISPLAYS

- 250-mA Sink Capability
- Rated for 10-V Operation ('496)
- Rated for 20-V Operation ('496A)
- TTL Input Compatability
- Low Standby Power
- High-Gain Darlington Circuits

N DUAL-IN-LINE PACKAGE (TOP VIEW)

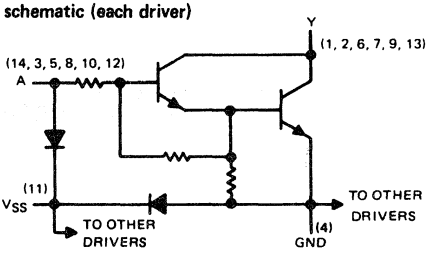


description

The SN75496 and SN75496A are monolithic integrated circuits designed to be used with TTL integrated circuits and common-cathode LED's in serjally addressed multi-digit displays. In a time-multiplexed system, which uses a segment-address-and-digit-scan method of LED drive, the number of drivers required can be minimized.

The SN75496 is characterized for operation to 10 volts, and the SN75496A is characterized for operation to 20 volts.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN75496	SN75496A	UNIT
Input voltage range (see Note 1)		−5 to V_{SS}	−5 to V_{SS}	V
Output voltage (see Note 2)		10	20	V
Output-to-input voltage		10	20	V
Voltage at V_{SS} terminal with respect to any other device terminal		10	20	V
Output current	each output	250	250	mA
	all outputs	600	600	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)		800	800	mW
Operating free-air temperature range		0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds		260	260	°C

NOTES: 1. The input is the only device terminal that may be negative with respect to ground.
2. Voltage values are with respect to network ground terminal unless otherwise noted.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 9.2 mW/°C from 63°C to 736 mW at 70°C.

9

electrical characteristics, V_{SS} = 10 V for SN75496, V_{SS} = 20 V for SN75496A, T_A = 0°C to 70°C (unless otherwise noted)

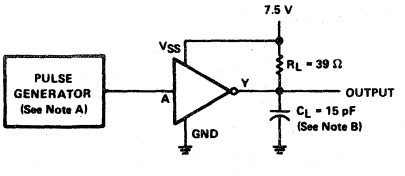
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2.4			V
V_{IL}	Low-level input voltage						0.8	V
V_{OL}	Low-level output voltage	V_I = 2.4 V, I_{OL} = 250 mA, T_A = 25°C				0.9	1.2	V
		V_I = 2.4 V, I_{OL} = 250 mA					1.5	
I_{OH}	High-level output current	V_{OH} = V_{SS}, V_I = 0.8 V					200	μA
I_I	Input current at maximum input voltage	V_I = V_{SS}, I_{OL} = 20 mA		SN75496		2.2	3.3	mA
				SN75496A		4.7	7.2	
I_{IH}	High-level input current	V_I = 2.4 V, V_O = V_{SS}					400	μA
I_{IL}	Low-level input current	V_I = 0.8 V					100	μA
I_{SS}	Current into V_{SS} terminal	V_I = −5 V to V_{SS}					1	mA

†All typical values are at 25°C.

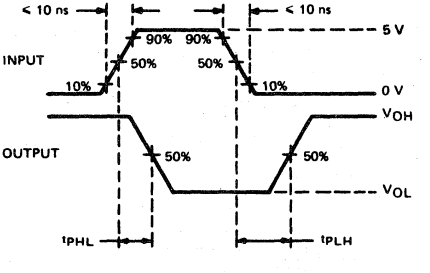
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 39 Ω, C_L = 15 pF, See Figure 1		300		ns
t_{PHL}	Propagation delay time, high-to-low-level output			30		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

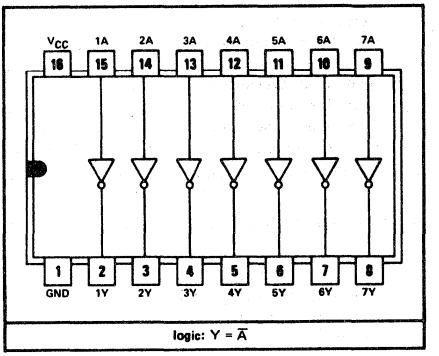
FIGURE 1–PROPAGATION DELAY TIMES

TYPES SN75497, SN75498
MOS-TO-LED 7- OR 9-CHANNEL DRIVERS

BULLETIN NO. DL-S 7712490, MAY 1977

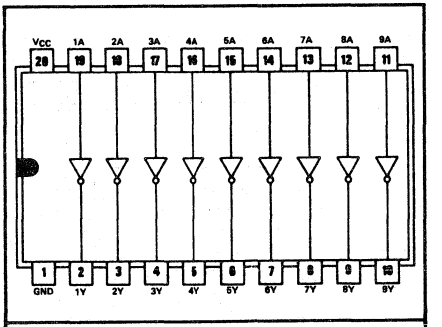
- 100-mA Output Sink Current Capability
- Low-Voltage Operation
- MOS- and TTL-Compatible Inputs
- Input Threshold . . . 2.7 V Max
- 7 Drivers (SN75497) or 9 Drivers (SN75498) per Package
- Low-Voltage Saturating Outputs
- Low Standby Power

SN75497 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: $Y = \overline{A}$

SN75498 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



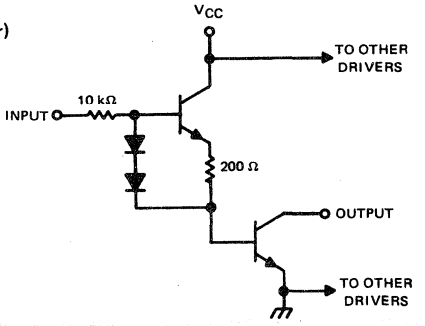
logic: $Y = \overline{A}$

description

The SN75497 and SN75498 are designed to drive common-cathode LED's in serially addressed multi-digit displays used in conjunction with MOS calculator circuits. The input of each circuit is capable of interfacing with an MOS push-pull output buffer while the output is capable of sinking the output current from a strobed LED display. These drivers are also essentially compatible with TTL inputs. They have a guaranteed threshold of 2.7 volts maximum, making them ideal for two-battery calculators or other low-voltage battery systems. They are designed to be used with active-pull-down MOS devices, but can also be used with open-drain MOS outputs with the addition of pull-down resistors on each input.

The 100-mA output current capability (open collector) and low output saturation voltage makes these devices ideal for other applications such as lamp drivers, relay drivers, line drivers, high-fan-out TTL buffers, etc. The advantages over earlier digit drivers include lower operating voltage, lower output saturation voltage, lower input current, and higher input voltage range.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . −11 V to V_{CC}
Output voltage . . . . . V_{CC}
Continuous output collector current . . . . . 125 mA
Ground-terminal current . . . . . 250 mA
Continuous total dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2.7	6.6	V
High-level input voltage, V_{IH}	2.7	V_{CC}	V
Low-level input voltage, V_{IL}	−8.5	0	V
Output Current, I_O		100	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

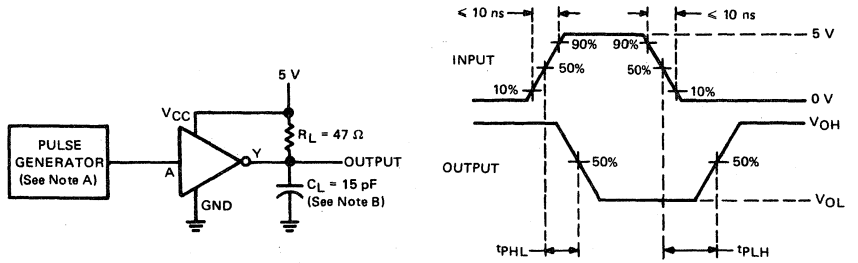
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_{CC} = 6.6 V,	A at 0 V,	Y at 6.6 V		10	100	μA
$V_{O(on)}$	On-state output voltage		V_{CC} = 6.6 V,	A at 6.6 V thru 500 Ω,	I_O = 100 mA		0.24	0.4	V
			V_{CC} = 2.7 V,	A at 2.7 V thru 500 Ω	I_O = 50 mA		0.12	0.25	
					I_O = 100 mA		0.24	0.4	
I_{IH}	High-level input current		V_{CC} = 6.6 V,	A at 6.6 V,	I_O = 100 mA		0.6	1	mA
			V_{CC} = 2.7 V,	A at 2.7 V,	I_O = 100 mA			0.4	
I_{IL}	Low-level input current		V_{CC} = 6.6 V,	A at −8.5 V,	V_O = 6.6 V		−10	−100	μA
			V_{CC} = 2.7 V,	A at −8.5 V,	V_O = 2.7 V			−100	
I_{CC}	Supply current	One driver on	V_{CC} = 6.6 V, I_O = 100 mA,	One A input at 6.6 V, Other A inputs at 0 V			2.5	5	mA
		All drivers off	V_{CC} = 6.6 V,	All inputs at 0 V				200	μA

† All typical values are at T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 15 pF, R_L = 47 Ω		250		ns
t_{PHL}	Propagation delay time, high-to-low level output			40		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

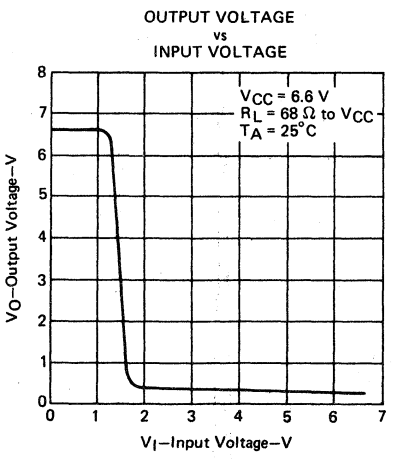


FIGURE 2

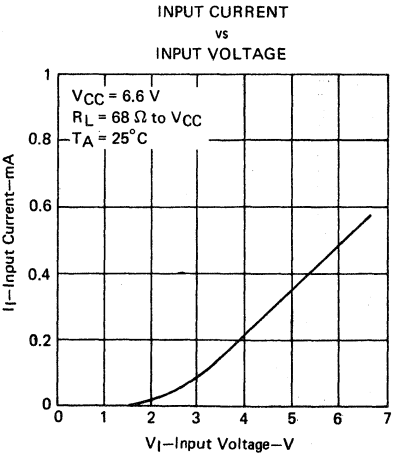


FIGURE 3

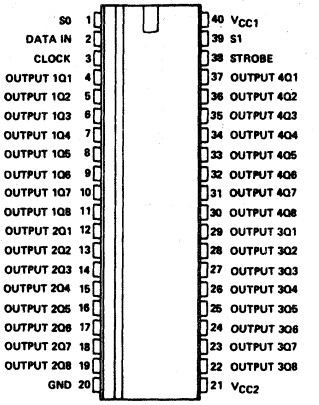
9

TYPES SN75500A, SN75502A AC PLASMA DISPLAY X-AXIS DRIVERS

BULLETIN NO. DL-S 12622, APRIL 1980

- Each Device Drives 32 Axis Lines
- High-Speed Serially Shifted Data Input Operation (4 MHz max)
- 100-V Output Voltage Swing Capability
- 20-mA Output Current Operation
- Low-Power Nonswitching Operation
- Fast Output Transitions
- Totem Pole Outputs
- Sink and Source Clamp Diodes
- SN75500A Has CMOS-Compatible Inputs
- SN75502A Has TTL-Compatible Inputs
- Selects 1 of 8 Lines Within 1 of 4 Groups
- Shift Register Can Retain Data on All Outputs Indefinitely While Clock is High

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

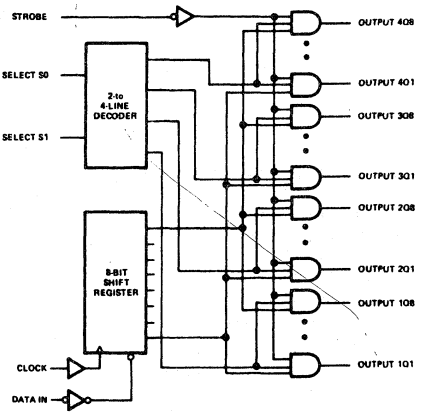


description

The SN75500A and SN75502A are monolithic BIDFET integrated circuits (bipolar, double-diffused MOS, n-channel MOS, and p-channel MOS transistors on the same chip†) designed to perform the select operation along the X-axis of a plasma display. The SN75500A is designed with CMOS-compatible inputs while the SN75502A is designed to be driven by TTL circuitry.

These devices each have an 8-bit shift register and a 2-to-4-line decoder, which steers the 8-bit data string to one of four groups of eight outputs. The shift register has indefinite latch capability when the clock input is held high. The decoder is controlled by inputs S0 and S1. The outputs are activated by the strobe input. When the strobe input is driven low, the selected 8-bit output group reflects the inverted data input string while the other twenty-four outputs remain low. With a capacitive load, this requires minimal power for driving the output.

functional block diagram



The device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open circuited. The nominal input threshold is 5 volts for the SN75500A and 1.5 volts for the SN75502A. The device outputs are totem-pole structures formed by double-diffused MOS (DMOS) transistors with clamp diodes to both ground and V_{CC2}.

†Patent pending

FUNCTION TABLE

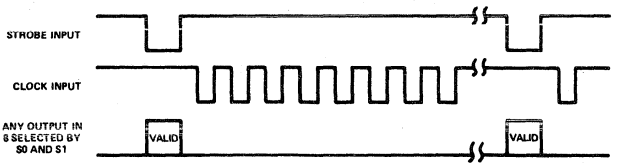
FUNCTION	INPUTS					OUTPUTS				
	DATA	CLOCK	S1	S0	STROBE	SHIFT REGISTERS R1 R2 R3 ... R8	1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
LOAD	H	↑	X	X	H	L $R1_n$ $R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H $R1_n$ $R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$ $R2_n$ $R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$ $R2_n$ $R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$ $R2_n$ $R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$ $R2_n$ $R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$ $R2_n$ $R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition

R1 ... R8 = levels currently at internal outputs of shift registers one through eight, respectively.

$R1_n$ ... $R8_n$ = levels at internal outputs of shift registers one through eight, respectively, before the most recent low-level pulse at the clock input.

typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

9

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13,2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	V_{CC1}		100	V
Peak high-level output current			−20	mA
Peak low-level output current			20	mA
High-level output clamp current			20	mA
Low-level output clamp current			−20	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH}	125			ns
Width of low clock pulse, t_{wL}	125		600	ns
Data setup time before low-to-high transition of clock, t_{su}	125			ns
Data hold time after low-to-high transition of clock, t_h	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75500A			SN75502A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage			7			2			V
V_{IL}	Low-level input voltage					3			0.8	V
V_{IK}	Input clamp voltage	V_{CC1} = 12 V, I_I = −12 mA			−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	95	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		92	94.5		
			I_{OH} = −15 mA	91	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	$V_I = V_{IH}$ min		−0.1	40		0.1	40	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	$V_I = V_{IL}$ max		−20	−150		−20	−150	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V	$V_I = V_{IH}$ min		1	2		1	2	mA
			$V_I = V_{IL}$ max		8	12		8	12	mA
I_{CC2}	Supply current	V_{CC2} = 100 V	Eight outputs high		1	3		1	3	mA
			All outputs low		1	2		1	2	mA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

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PARAMETER MEASUREMENT INFORMATION

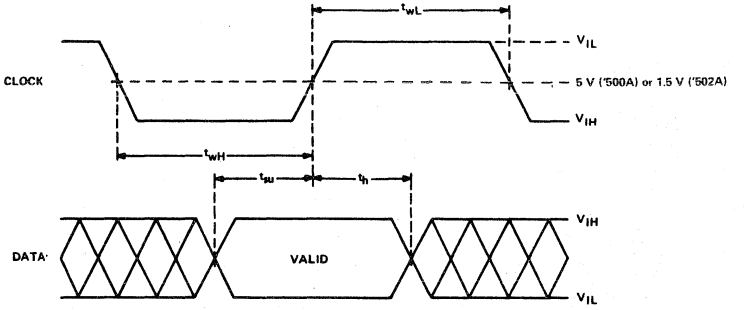


FIGURE 1–DATA INPUT TIMING

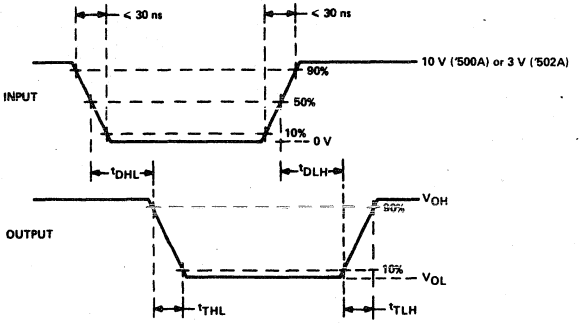
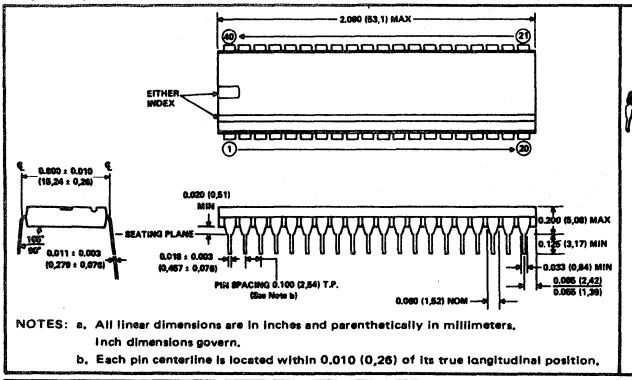
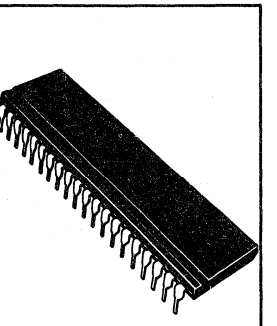


FIGURE 2–OUTPUT SWITCHING TIMES

MECHANICAL DATA

40-pin N plastic dual-in-line package





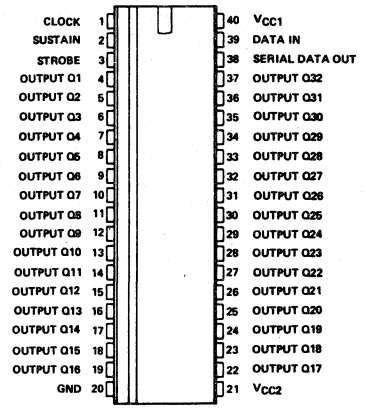
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TYPES SN75501A, SN75503A
AC PLASMA DISPLAY Y-AXIS DRIVERS

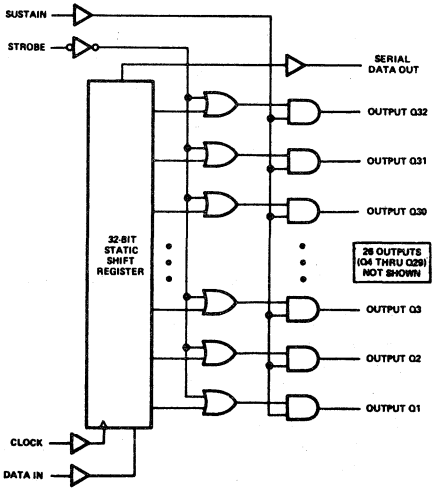
BULLETIN NO. DL-S 12621, APRIL 1980

- Each Device Drives 32 Axis Lines
- High-Speed Serially Shifted Data Input Operation (4 MHz Max)
- 100-V Output Voltage Swing Capability
- 20-mA Output Current Operation
- Low-Power Nonswitching Operation
- Fast Output Transitions
- Totem-Pole Outputs
- Sink and Source Clamp Diodes
- SN75501A Has CMOS-Compatible Inputs
- SN75503A Has TTL-Compatible Inputs
- Performs Y-Axis Sustaining Function
- Static Shift Register Can Retain Data on all Outputs Indefinitely

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram



description

The SN75501A and SN75503A are monolithic BIDFET integrated circuits (bipolar, double-diffused MOS, n-channel MOS, and p-channel MOS transistors on the same chip†) designed to perform the select operation and the sustain function along the Y-axis of a plasma display. The SN75501A is designed with CMOS-compatible inputs while the SN75503A is designed to be driven by TTL circuitry.

These devices each have a 32-bit shift register with indefinite latch capability when the clock input is either high or low. Information at the data input meeting the setup time requirements is transferred into the shift register on the positive-going edge of the clock signal. Each shift register output drives its respective Q output through two gates controlled by the strobe and sustain inputs, respectively. The strobe input controls the outputs for writing and erase functions, while the sustain input controls the output for system sustaining along the Y-axis. The serial-data output can be used to cascade shift registers.

The device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 5 volts for the SN75501A and 1.5 volts for the SN75503A. The device outputs are totem-pole structures formed by double-diffused MOS (DMOS) transistors with clamp diodes to both ground and V_{CC2}.

†Patent pending

FUNCTION TABLE

FUNCTION	INPUTS				OUTPUTS						
	DATA IN	CLOCK	STROBE	SUSTAIN	SHIFT REGISTERS R1	R2	R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n \ldots R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n \ldots R31_n$	$R32_n$	H	H	H . . . H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n \ldots R32_n$	$R32_n$	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n \ldots R32_n$	$R32_n$	R1	R2	R3 . . . R32
SUSTAIN	X	X	X†	L	$R1_n$	$R2_n$	$R3_n \ldots R32_n$	$R32_n$	L	L	L . . . L

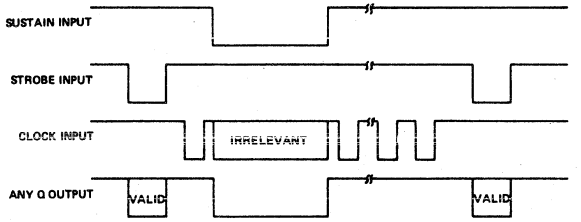
H = high level, L = low level, X = irrelevant, ↑ = low-to-high level transition.

R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.

$R1_n \ldots R32_n$ = levels at internal outputs of shift registers one through thirty-two, respectively, before the most recent low-level pulse at the clock input.

†To minimize delay time for the next output signals, it is recommended that Strobe remain high while Sustain is low. Delay time from Strobe to the Q outputs is typically longer than from Sustain.

typical operating sequence



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	V_{CC1}		100	V
Peak high-level output current			−20	mA
Peak low-level output current			20	mA
High-level output clamp current			20	mA
Low-level output clamp current			−20	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH}	125			ns
Width of low clock pulse, t_{wL}	125			ns
Data setup time before low-to-high transition of clock, t_{su}	125			ns
Data hold time after low-to-high transition of clock, t_h	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75501A			SN75503A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH} High-level input voltage				7			2			V
V_{IL} Low-level input voltage						3			0.8	V
V_{IK} Input clamp voltage		V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH} High-level output voltage	Outputs 1 through 32	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	95	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		92	94.5		
			I_{OH} = −15 mA	91	93.5		91	93.5		
	Serial data	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		9	10		
V_{OL} Low-level output voltage	Outputs 1 through 32	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
	Serial data	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1		0.1	1	
V_{OK} Output clamp voltage		V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH} High-level input current		V_{CC1} = 13.2 V,	$V_I = V_{IH}$ min		0.1	40		0.1	40	μA
I_{IL} Low-level input current		V_{CC1} = 13.2 V,	$V_I = V_{IL}$ max		−20	−150		−20	−150	μA
I_{CC1} Supply current		V_{CC1} = 13.2 V	$V_I = V_{IH}$ min		0.5	2		0.5	2	mA
			$V_I = V_{IL}$ max		6	12		6	12	mA
I_{CC2} Supply current		V_{CC2} = 100 V	All outputs high		1	3		1	3	mA
			All outputs low		1	3		1	3	mA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{DHL}	Delay time, high-to-low-level output from sustain input			250	ns
t_{DLH}	Delay time, low-to-high-level output from sustain input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION

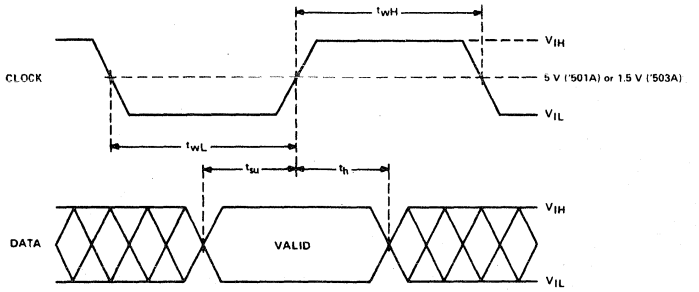

FIGURE 1–DATA INPUT TIMING

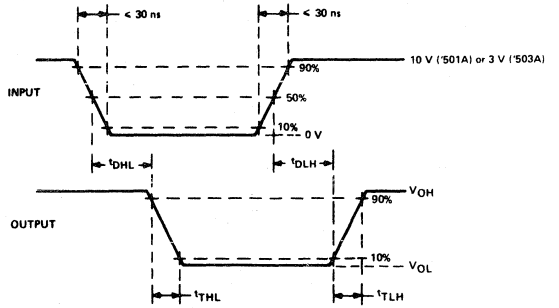

FIGURE 2–OUTPUT SWITCHING TIMES

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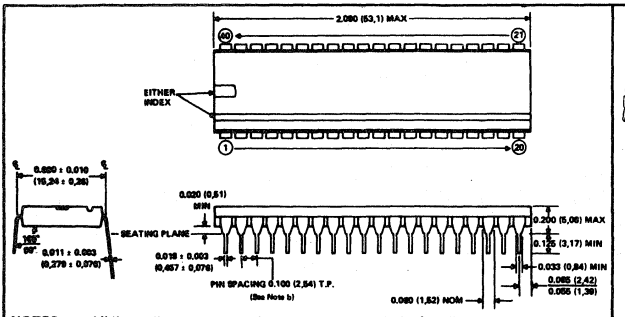
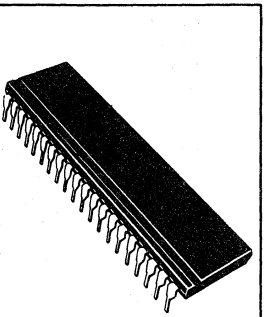
MECHANICAL DATA

40-pin N plastic dual-in-line package





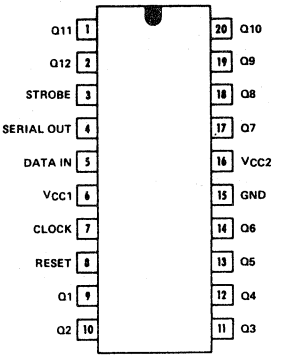
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TYPE SN75510
VACUUM FLUORESCENT DISPLAY DRIVER

BULLETIN NO. DL-S 12764, AUGUST 1980

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Reset Input

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

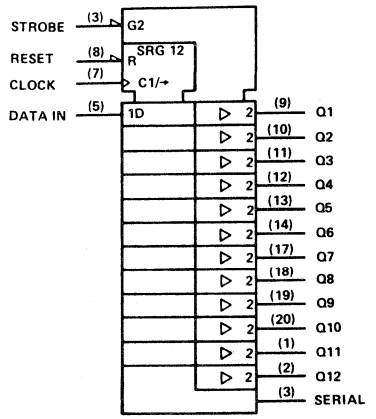
The SN75510 is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS, and P-channel MOS transistors on the same chip†), designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and diffused MOS (DMOS) transistors.

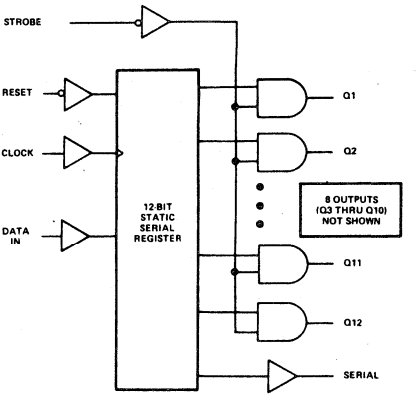
The device consists of a 12-bit shift register and 12 output AND gates. Data is entered into the shift register on the low-to-high transition of the clock. The active-low strobe input enables all Q outputs. The reset input sets the shift register contents to all lows. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input.

The SN75510 is characterized for operations from 0°C to 70°C.

logic symbol‡



functional block diagram



†Patent Pending.
‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

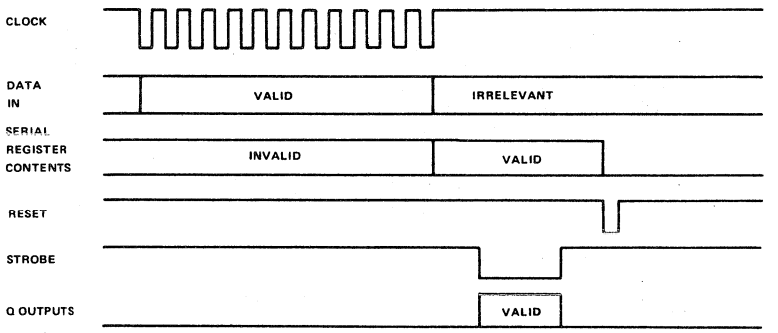
TEXAS INSTRUMENTS
INCORPORATED

FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	RESET	CLOCK	STROBE	R1 THRU R12	SERIAL	Q1 THRU Q12
LOAD	H	↑	X	Load and shift*	R12*	Determined by Strobe
STROBE	H	Not↑	H	No change	R12	All L
	H	Not↑	L	No change	R12	R1 thru R12, respectively
RESET	L	X	X	All L	L	All L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
*R12 and Serial output take on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



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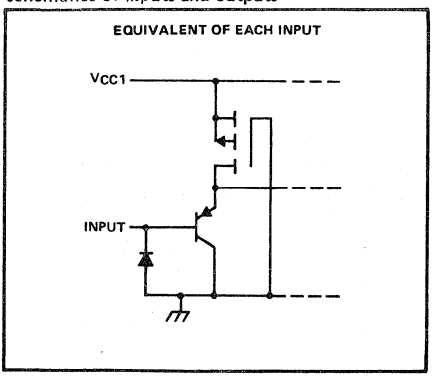
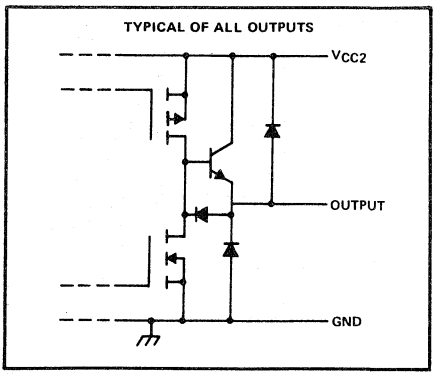
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 60 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}			60	V
Peak high-level output current			−25	mA
Peak low-level output current			5	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH} (see Figure 1)	125			ns
Width of low clock pulse, t_{wL} (see Figure 1)	125			ns
Data setup time before low-to-high transition of clock, t_{su} (see Figure 1)	125			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1)	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{IK}	Input clamp voltage		V_{CC1} = 12 V, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 10.8 V, V_{CC2} = 60 V, I_{OH} = −25 mA		55	57.5		V
		Serial data	V_{CC1} = 12 V, I_{OH} = −200 μA		11	11.3		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 12 V, I_{OL} = 5 mA			1.9	5	V
		Serial data	V_{CC1} = 12 V, I_{OL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_I = 7 V			0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_I = 3 V			−30	−150	μA
I_{CC1}	Supply current		V_{CC1} = 13.2 V	V_I = 7 V		150	800	μA
				V_I = 3 V		10	12	mA
I_{CC2}	Supply current		V_{CC1} = 13.2 V, V_{CC2} = 60 V	All outputs high		5	8	mA
				Strobe at 7 V		100	500	μA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF See Figure 2		500	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			500	ns
t_{THL}	Transition time, high-to-low-level output			300	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

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PARAMETER MEASUREMENT INFORMATION

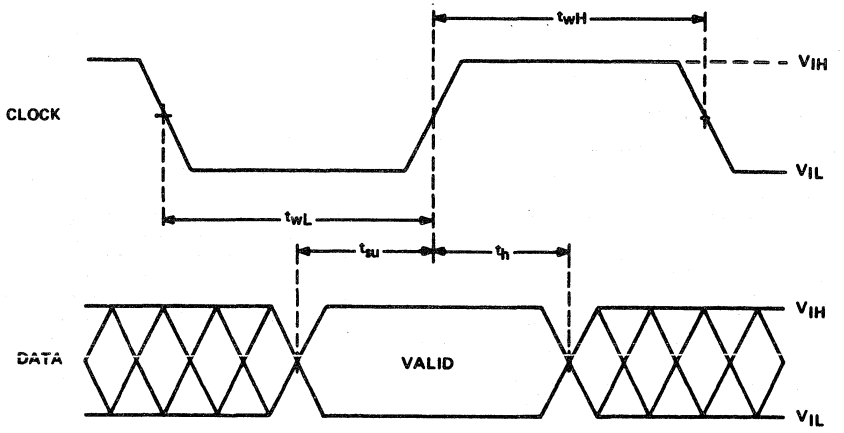


FIGURE 1 – INPUT TIMING

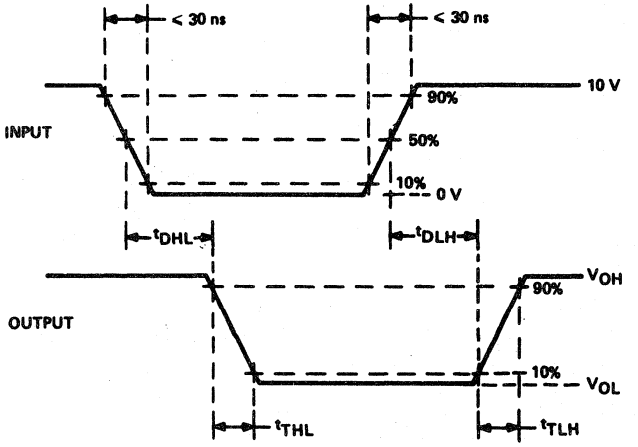


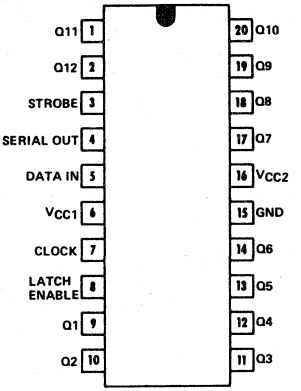
FIGURE 2 – SWITCHING TIMES

TYPE SN75511
VACUUM FLUORESCENT DISPLAY DRIVER

BULLETIN NO. DL-S 12765, AUGUST 1980

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

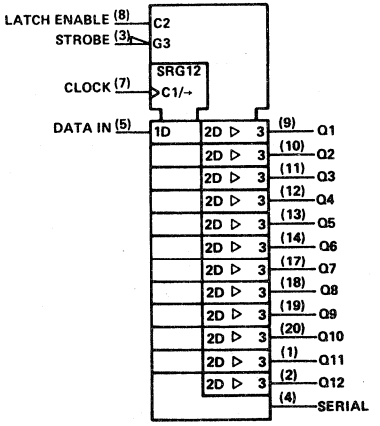
The SN75511 is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS and p-channel MOS transistors on same chip†) designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

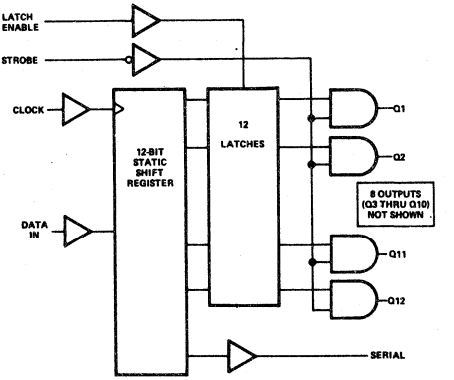
The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock. When high, the latch enable input transfers the shift register contents to the outputs of the 12 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the latch enable or strobe inputs.

The SN75511 is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram



†Patent Pending

‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

PRODUCT PREVIEW

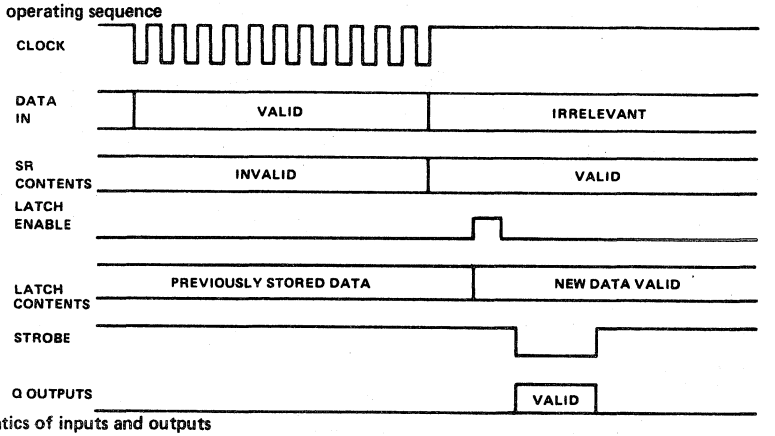
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R12	LATCHES LC1 THRU LC12†	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable†	R12*	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable†	R12	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R12	Determined by Strobe
	X	H	X	As determined above	New data	R12	Determined by Storbe
STROBE	X	X	H	As determined above	Determined by Latch Enable†	R12	All L
	X	X	L	As determined above	Determined by Latch Enable†	R12	LC1 thru LC12, respectively

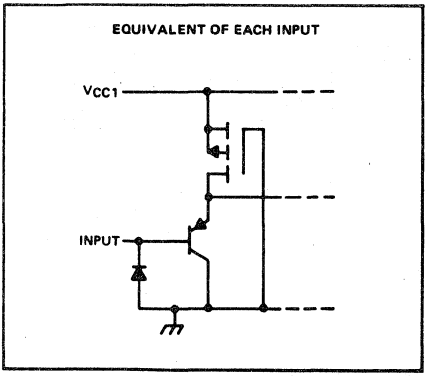
H = high level, L = Low level, X = Irrelevant, ↑ = low-to-high-level transition.
†New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
*R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

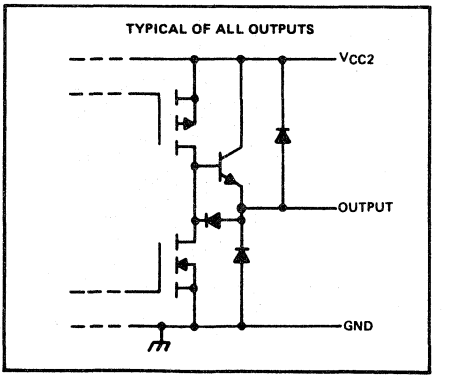
typical operating sequence



9

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 60 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}			60	V
Peak high-level output current			−25	mA
Peak low-level output current			5	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH} (see Figure 1)	125			ns
Width of low clock pulse, t_{wL} (see Figure 1)	125			ns
Data setup time before low-to-high transition of clock, t_{su} (see Figure 1)	125			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1)	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{IK}	Input clamp voltage		V_{CC1} = 12 V, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 10.8 V, V_{CC2} = 60 V, I_O = −25 mA		55	57.5		V
		Serial data	V_{CC1} = 12 V, I_{OH} = −200 μA		11	11.3		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 12 V, I_{OL} = 5 mA			1.9	5	V
		Serial data	V_{CC1} = 12 V, I_{OL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_I = 7 V			0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_I = 3 V			−30	−150	μA
I_{CC1}	Supply current		V_{CC1} = 13.2 V	V_I = 7 V		150	800	μA
				V_I = 3 V		10	12	mA
I_{CC2}	Supply current		V_{CC1} = 13.2 V, V_{CC2} = 60 V	All outputs high		5	8	mA
				Strobe at 7 V		100	500	μA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		500	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			500	ns
t_{THL}	Transition time, high-to-low-level output			300	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

9

PARAMETER MEASUREMENT INFORMATION

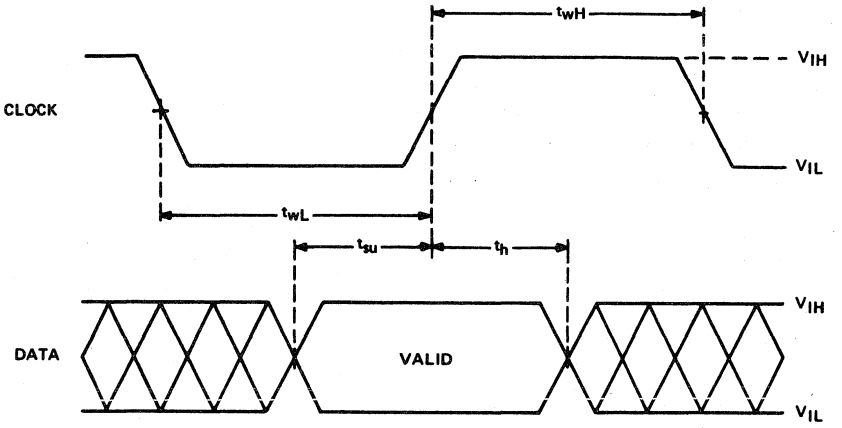


FIGURE 1–INPUT TIMING

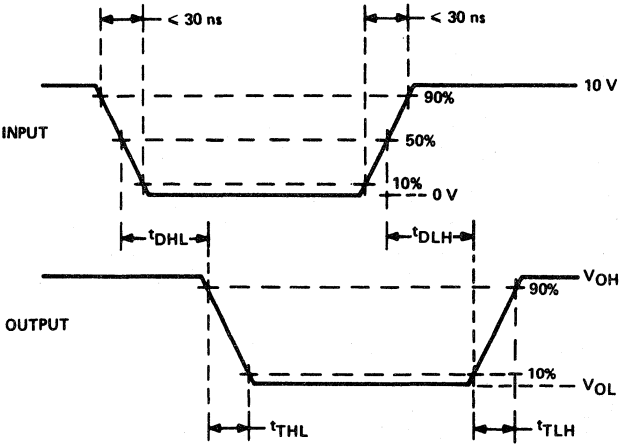


FIGURE 2–OUTPUT SWITCHING TIMES

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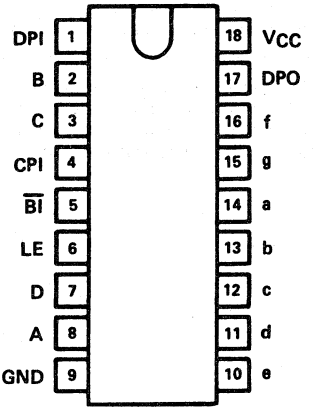
TYPE SN75580
HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

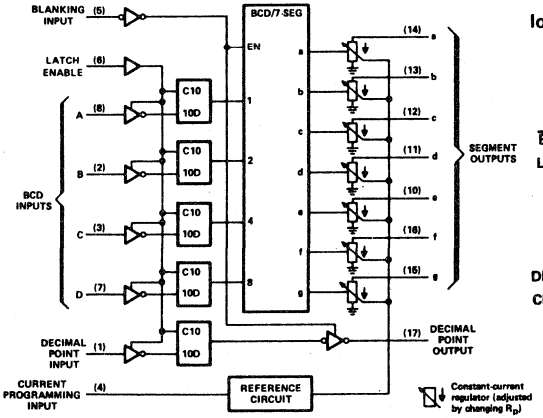
D2626, MAY 1981

- Output Current Adjustable From 0.1 mA to 1 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs . . . 100 V Min
  Decimal Point Output . . . 100 V Min
- Input Data Latches
- Blanking Input Provided
- Low Power Requirements
- Supply Voltage Variable over Wide Range . . . 5 V to 15 V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

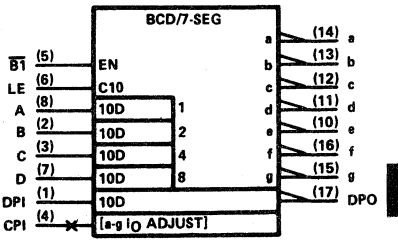
N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

description

The SN75580 is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

†Trademark of Burroughs Corporation.

description (continued)

Output currents may be varied from 0.1 mA to 1 mA for driving various displays. The output current is adjusted by connecting an external programming resistor (R_p) from the current programming input to ground.

The blanking input provides unconditional blanking of all segment outputs including the decimal point output.

The enable input allows data to be stored internally while input data is changing. When enable is at a high-level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs. A transition from a high-level voltage to a low-level voltage at enable will cause the input data set up prior to the transistion to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

FUNCTION TABLE

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUTPUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

†Table is valid for the indicated BCD and decimal point inputs while the latch enable is high. See description.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage	V_{CC}
Peak transient off-state voltage, segment outputs (See Note 2)	180 V
Continuous on-state segment output current	4 mA
Peak transient on-state segment output current (See Note 3)	50 mA
Continuous total dissipation	650 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In all applications, peak transient segment output voltage must be limited to 180 V. This is accomplished by limiting the anode voltage to 180 V maximum.
3. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10\ \mu s$, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (See Figure 4).

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	5	15	V
Segment output voltage	4	100	V
Decimal point output voltage	4	100	V
Segment-b output current	0.1	1	mA
Enable pulse width, t_w (see Figure 2)	500		ns
Data setup time before enable goes low (see Figure 2)	500		ns
Data hold time after enable goes low (see Figure 2)	500		ns
Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		V_{CC} = 10 V		7			V
V_{IL}	Low-level input voltage		V_{CC} = 10 V				3	V
V_{IK}	Input clamp voltage		V_{CC} = 15 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
$V_{O(on)}$	On-state output voltage	Decimal point	V_{CC} = 5 V, I_O = 25 mA				4	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI at 0 V, I_O = 3 μA		100			V
		Decimal point			100			
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 10 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18080 Ω	0.17	0.20	0.23	mA
				R_p = 7232 Ω	0.425	0.50	0.575	
				R_p = 3616 Ω	0.85	1.00	1.15	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 10 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
I_{IH}	High-level input current	All inputs except CPI	V_{CC} = 10 V, V_I = 10 V				1	μA
I_{IL}	Low-level input current	All inputs except CPI	V_{CC} = 10 V, V_{CC} = 0 V				1	μA
I_{CC}	Supply current		V_{CC} = 15 V, All inputs at 10 V, R_p open				4	mA
			V_{CC} = 15 V, All inputs at 0 V, R_p = 3.6 kΩ				6	

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switching characteristics, V_{CC} = 10 V, T_A = 25°C, see figures 1 and 2

PARAMETER		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.5	10	
t_{off}	Turn-off time of segment outputs from DP input		0.5	10	µs
t_{on}	Turn-on time of segment outputs from DP input		0.5	10	
t_{off}	Turn-off time of segment outputs from BI		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BI		0.5	10	

PARAMETER MEASUREMENT INFORMATION

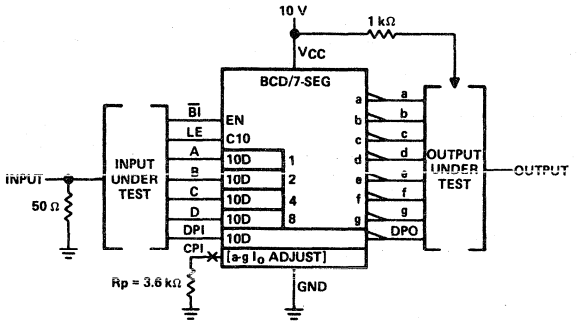


FIGURE 1–TEST CIRCUIT

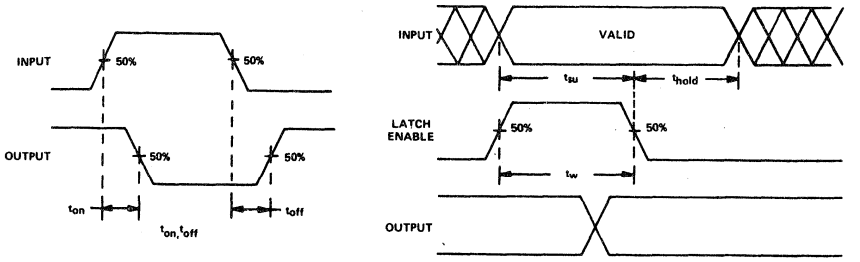
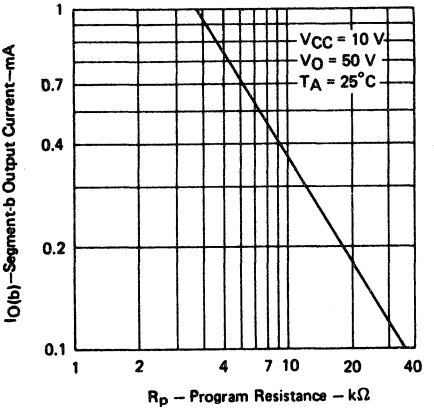


FIGURE 2–VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

SEGMENT-b OUTPUT CURRENT
vs
PROGRAM RESISTANCE



$$I_{O(b)} \text{ in mA} = \frac{3.616}{R_p \text{ in k}\Omega}$$

FIGURE 3

TYPICAL APPLICATION DATA

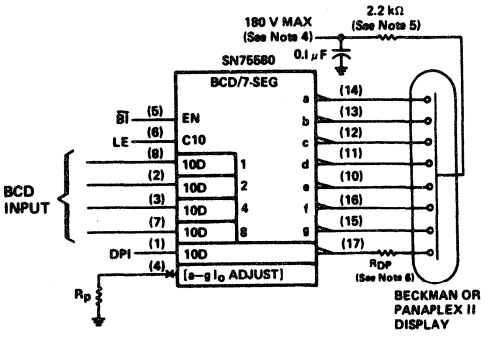


FIGURE 4—SINGLE-DIGIT 7-SEGMENT DISPLAY

NOTES: 4. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 100 V at the segment outputs of the SN75580.

5. In all applications, peak transient segment current must be limited to 50 mA (t_w ≤ 10 μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

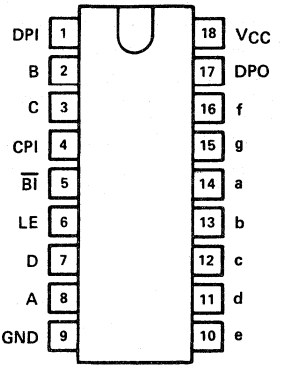
6. The value of R_{DP} is chosen for even illumination of the decimal point and the digit.

TYPE SN75584A HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

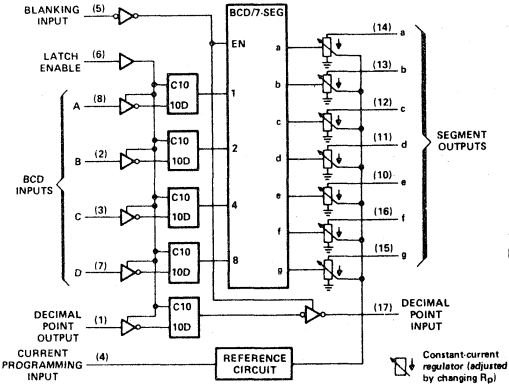
D2627, MAY 1981

- Output Current Adjustable From 0.1 mA to 4 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs . . . 100 V Min
  Decimal Point Output . . . 100 V Min
- Input Data Latches
- Blanking Input Provided
- P-N-P Inputs for Minimal Input Loading
- Low Power Requirements
- Thermal Protection Circuitry
- Supply Voltage Variable Over Wide Range . . . 4.75 V to 15 V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

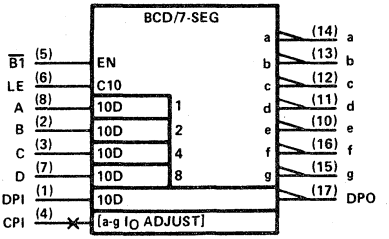
N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



logic symbol †



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

description

The SN75584A is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

† Trademark of Burroughs Corporation.

description (continued)

Output currents may be varied from 0.1 mA to 4 mA for driving various displays. The output current is adjusted by connecting an external programming resistor (R_P) from the current programming input to ground.

The blanking input provides unconditional blanking of all segment outputs including the decimal point output.

The enable input allows data to be stored internally while input data is changing. When enable is at a high-level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs. A transition from a high-level voltage to a low-level voltage at enable will cause the input data set up prior to the transition to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

Thermal protection circuitry will blank the display, regardless of input conditions, whenever junction temperature exceeds approximately 150°C.

FUNCTION TABLE

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUTPUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

†Table is valid for the indicated BCD and decimal point inputs while enable is high. See description.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage	V_{CC}
Peak transient off-state voltage, segment outputs (See Note 2)	180 V
Continuous on-state segment output current	4 mA
Peak transient on-state segment output current (See Note 3)	50 mA
Continuous total dissipation	650 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. In all applications, peak transient segment output voltage must be limited to 180 V. This is accomplished by limiting the anode voltage to 180 V maximum.

3. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (see Figure 4).

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	15	V
Segment output voltage	4	100	V
Decimal point output voltage	0	100	V
Segment-b output current	0.1	4	mA
Enable pulse width, t_w (see Figure 2)	500		ns
Data setup time before enable goes low (see Figure 2)	500		ns
Data hold time after enable goes low (see Figure 2)	500		ns
Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 15 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI at 0 V, I_O = 3 μA		100			V
		Decimal point			100			
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 10 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18080 Ω	0.18	0.20	0.22	mA
				R_p = 7232 Ω	0.45	0.50	0.55	
				R_p = 2411 Ω	1.35	1.5	1.65	
				R_p = 1808 Ω	1.8	2.0	2.2	
				R_p = 1205 Ω	2.7	3.0	3.3	
				R_p = 904 Ω	3.6	4.0	4.4	
			V_{CC} = 5 V to 15 V, $V_{O(b)}$ = 10 V to 100 V, T_A = 0°C to 70°C	R_p = 18080 Ω	0.16		0.24	
				R_p = 7232 Ω	0.4		0.6	
				R_p = 2411 Ω	1.2		1.8	
				R_p = 1808 Ω	1.6		2.4	
				R_p = 1205 Ω	2.4		3.6	
				R_p = 904 Ω	3.2		4.8	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 10 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
		Segments a, f, & g	V_{CC} = 5 V to 15 V, All outputs at 10 V to 100 V, T_A = 0°C to 70°C		0.74		1.12	
		Segment c			1		1.5	
		Segment d			0.8		1.2	
		Segment e			0.88		1.32	
I_{IH}	High-level input current	All inputs	V_{CC} = 15 V, V_I = 15 V	Enable at 15 V			15	μA
		A, B, C, D, & DP		Enable at 0 V			1	
I_{IL}	Low-level input current	All inputs	V_{CC} = 15 V, V_I = 0.4 V	Enable at 15 V			−50	μA
		Enable		Enable at 0.4 V			−50	
		A, B, C, D, & DP		Enable at 0 V			−1	
I_{CC}	Supply current		V_{CC} = 15 V, All inputs at 15 V, R_p open				4	mA
			V_{CC} = 15 V, All inputs at 0 V, R_p = 2.2 kΩ				6	

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figures 1 and 2

	PARAMETER	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.5	10	
t_{off}	Turn-off time of segment outputs from DP input		0.5	10	µs
t_{on}	Turn-on time of segment outputs from DP input		0.5	10	
t_{off}	Turn-off time of segment outputs from BI		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BI		0.5	10	

PARAMETER MEASUREMENT INFORMATION

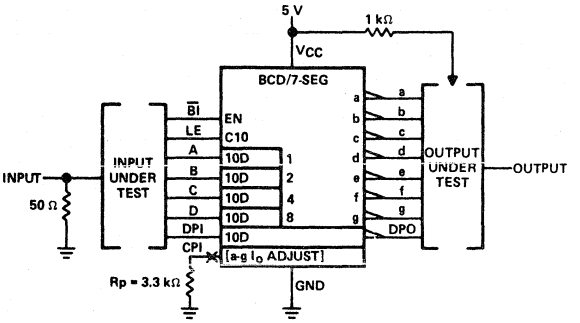


FIGURE 1 – TEST CIRCUIT

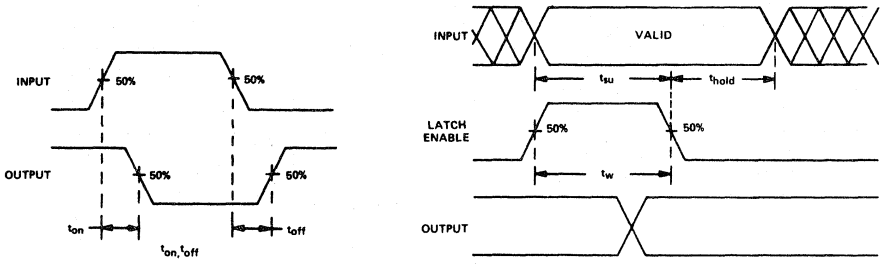
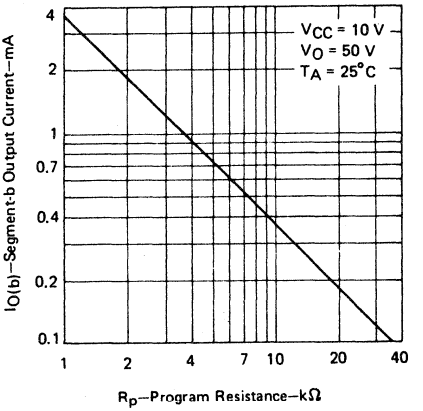


FIGURE 2–VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

SEGMENT-b OUTPUT CURRENT
vs
PROGRAM RESISTANCE



$$I_{O(b)} \text{ in mA} = \frac{3.616}{R_p \text{ in k}\Omega}$$

FIGURE 3

TYPICAL APPLICATION DATA

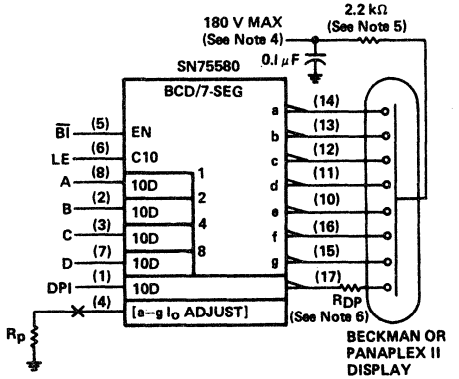


FIGURE 4—SINGLE-DIGIT 7-SEGMENT DISPLAY

NOTES: 4. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 100 V at the segment outputs of the SN75584A.

5. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

6. The value of R_{DP} is chosen as required for even illumination of the decimal point and the digit.

JAN MIL-M-38510
Integrated Circuits

10

MIL-M-38510 AND MIL-STD-883
Military High-Reliability Integrated Circuits

The Texas Instruments MIL-M-38510 and MIL-STD-883 programs offer several options designed to meet system cost, reliability, lead time, and contract requirements. The following are the key features of the options available for MIL-M-38510 and MIL-STD-883 Class B applications:

JAN-Processed TI SNJ

- Produced under MIL-M-38510 guidelines with all chips manufactured in a DESC-certified front end facility
- Fully tested per MIL-STD-883 method 5004 Class B
- Includes device types covered by MIL-M-38510 part numbers and circuits not yet covered by MIL numbers
- Electrical and mechanical characteristics per TI data sheets
- Marked with 38510 part numbers where applicable
- Each lot includes Certificate of Conformance and Group A Summary Report
- Approximately one-half the cost of JAN-Qualified IC's

SNC/MACH-IV (883B)

- Cost effective – approximately one-third the cost of JAN-Qualified IC's
- Produced under MIL-M-38510 guidelines with all chips manufactured in a DESC-certified front end facility
- Tested per MIL-STD-883 method 5004 Class B and TI 38510/MACH-IV specification, Section 9 of this catalog
- Tested per MIL-STD-883 method 5004 Class B and TI 38510/MACH-IV specification, Section 9 of this catalog
- Electrical and mechanical characteristics per TI data sheets
- Available in broad product spectrum including SSI, MSI, and LSI, both bipolar and MOS

JAN-Qualified

- Qualified per MIL-M-38510 Class B
- Produced per MIL-STD-883 and MIL-M-38510 Class B and appropriate slash sheets
- Produced in DESC-certified domestic production facility
- Applicable devices and packages

PRODUCT	A	C	D	E	F	G	I	J	L	T	V	W
SERIES 54 TTL		X	X	X	X			X	X			
SERIES 54H TTL		X	X	X	X							
SERIES 54L TTL *										X		
SERIES 54LS TTL		X	X	X	X			X	X			
SERIES 54S TTL		X	X	X	X			X	X			
LINEAR CONTROL		X				X	X					
SERIES 55 INTERFACE		X		X								
MOS LSI										X	X	X
LEAD FINISH B		X	X	X	X			X	X		X	X
LEAD FINISH C/D						X	X			X		

* PER MIL-M-00385108, Class S.

10

How to Order

See Tables I, II and III for device, package and lead-finish cross-reference.

- **JAN-Processed/TI SNJ**

Device type covered by 38510 part number:			Device type not covered by 38510 part number:		
Device	SN5400J	883 Class B	Device	SN54LS298J	883 Class B
Order	SNJ5400J			SNJ54LS298J	
Marking	SNJ5400J 38510/00104BCB		Marking	SNJ54LS298J 38510B	

- **SNC/MACH-IV**

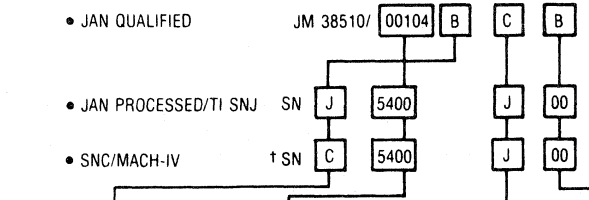
Device	SNC5400J	883 Class B
Order	SNC5400J	
Marking	SNC5400J	

- **JAN-Qualified**

Device	SN5400J	883 Class B
Order	JM38510/00104BCB	
Marking	JM38510/00104BCB	

Table I Part Numbers

EXAMPLE: 5400 TTL NAND gate in ceramic dual-in-line package to 883 Class B with standard tin-plated leads.



CASE OUTLINE

JAN	PACKAGE	SNJ SNC/MACH-IV
A	1/4" x 1/4" FLAT-14	U/FB
B/T*	1/4" x 1/8" FLAT-14	T
C	DIP-14	J
D	1/4" x 3/8" FLAT-14	W
E	DIP-16	J
F	1/4" x 3/8" FLAT-16	W/SB
G	TO-99	L
H	1/4" x 1/4" FLAT-10	U
I	TO-100	L
J	DIP-24	J
K	3/8" x 5/8" FLAT-24	W
L	3/8" x 1/2" FLAT-24	W
V	DIP-18	JR §
W	DIP-22	JR §
X	TO-5	—
Y	TO-3	—
Z	1/4" X 3/8" FLAT-24	—

LEAD FINISH

JAN	TYPE	SNJ SNC/MACH-IV
A	SOLDER DIP	10
B	TIN-PLATE	00
C/D*	GOLD-PLATE	00
X	OPTIONAL **	

*Per MIL-M-0038510B, Class S.
**Finish B or C at TI's option. Devices will be marked B or C as applicable.
†Prefix designation for MOS/LSI is "SMC."
§R denotes temperature range.

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Screening — Class B

	JAN QUALIFIED		SNJ JAN PROCESSED		SNC MACH-IV	
SCREEN	**METHOD**	**RQMT**	**METHOD**	**RQMT**	**METHOD**	**RQMT**
Internal Visual (Precap)	2010.2 Cond B and 38510	100%	2010.2 Cond B and 38510	100%	2010.2 Cond B and 38510	100%
Stabilization Bake	1008.1 24 hrs min test Cond C	100%	1008.1 24 hrs min test Cond C	100%	1008.1 24 hrs min test Cond C	100%
Temperature Cycling	1010.1 Cond C	100%	1010.1 Cond C	100%	1010.1 Cond C	100%
Constant Acceleration	2001.1 Cond E (min) in Y_1 plane	100%	2001.1 Cond E (min) in Y_1 plane	100%	2001.1 Cond E (min) in Y_1 plane	100%
Seal (a) Fine (b) Gross	1014.1	100%	1014.1	100%	1014.1 (cond C_1)	100%
Interim Electrical	JAN slash-sheet electrical specifications	As applicable	TI data sheet electrical specifications	As applicable	TI data sheet electrical specifications	As applicable
Burn-in test	1015.1 160 hrs @ 125°C min	100%	1015.1 160 hrs @ 125°C min	100%	1015.1 160 hrs @ 125°C min	100%
Final Electrical Tests (a) Static tests (1) 25°C (Subgroup 1, table 1, 5005.3)	JAN slash-sheet electrical specifications	100%	TI data sheet electrical specifications	100%	TI data sheet electrical specifications	100%
(2) Max and min rated op. temperature (subgroups 2 and 3 table 1, 5005.3)		100%		100%		100% Note 1
(b) Dynamic tests and switching tests 25°C (subgroup 4 and 9, table 1, 5005.3)		100%		100%		
(c) Functional test 25°C (subgroup 7, table 1, 5005.3)		100%		100%		100%
Qualification or quality conformance inspection	5005.3 Class B	per 38510	5005.3 Class B	per 38510 Note 2	5005.3 Class B	per 38510 Note 2
External Visual	2009.1	100%	2009.1	100%	2009.1	100%

NOTES: 1. Temperature guardband test may be used in lieu of 100% test for digital bipolar only.
2. Group A per 5005.3. Generic data available for groups B, C, and D.

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For MIL-M-38510/MIL-STD-883 Class A/S

For critical space and satellite applications, SAMSO Class S JAN-Qualified TTL flat pack devices are available per MIL-M-0038510B including:

CIRCUIT TYPE	JAN NO.
SN54L00T	JM38510/02004STD
SN54L01T	JM38510/02006STD
SN54L02T	JM38510/02701STD
SN54L04T	JM38510/02005STD
SN54L10T	JM38510/02003STD
SN54L20T	JM38510/02002STD
SN54L30T	JM38510/02001STD
SN54L51T	JM38510/04101STD
SN54L54T	JM38510/04104STD
SN54L71T	JM38510/02101STD
SN54L74T	JM38510/02105STD
SN54L78T	JM38510/02104STD
SN54L86T	JM38510/02601STD
SN54L91T	JM38510/02806STD
SN54L95T	JM38510/02801STD
SN54L121T	JM38510/04201STD
SN54L122T	JM38510/04202STD
SN54L164T	JM38510/02802STD
SN5400T	JM38510/00104STD
SN5401T	JM38510/00107STD
SN5402T	JM38510/00401STD
SN5404T	JM38510/00105STD
SN5410T	JM38510/00103STD
SN5420T	JM38510/00102STD
SN5440T	JM38510/00301STD
SN5472T	JM38510/00201STD
SN5473T	JM38510/00202STD
SN5474T	JM38510/00205STD
SN5493T	JM38510/01302STD
SN5495T	JM38510/00901STD
SN54121T	JM38510/01201STD
SN54H00T	JM38510/02304STD

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
00101	5430	01307	5490	03001	15930	06005	10507‡
00102	5420	01308	54192	03002	15935	06006	10509‡
00103	5410	01309	54193	03003	15936	06101	10531‡
00104	5400	01310†	54196	03004	15946	06102	10631‡
00105	5404	01311†	54197	03005	15962	06103	10576‡
00106	5412	01312†	54177	03101	15932	06104	10535‡
00107	5401	01401	54150	03102	15944	06201	10504
00108	5405	01402	9312‡	03103	15957	06202	10597
00109	5403	01403	54153	03104	15958	07001	54S00
00201	5472	01404	9309	03105	15933	07002	54S03
00202	5473	01405	54157	03201	15951	07003	54S04
00203	54107	01406	54151	03301	15945	07004	54S05
00204	5476	01501	5475	03302	15948	07005	54S10
00205	5474	01502	5477	03303	15950	07006	54S20
00206	5470	01503	54116	03304	9094	07007	54S22
00207	5479‡	01504	9314‡	03501	MH0026	07008	54S30
00301	5440	01601	5408	04001	54H50	07009	54S133
00302	5437	01602	5409	04002	54H51	07010	54S134
00303	5438	01701	54174	04003	54H53	07101	54S74
00401	5402	01702	54175	04004	54H54	07102	54S112
00402	5423	01703†	54173	04005	54H55	07103	54S113
00403	5425	01801	54170	04101	54L51	07104	54S114
00404	5427	01901	54180	04102	54L54	07105	54S174
00501	5450	02001	54L30	04103	54L55	07106	54S175
00502	5451	02002	54L20	04104♦	54L54	07201	54S40
00503	5453	02003	54L10	04201	54L121	07301	54S02
00504	5454	02004	54L00	04202	54L122	07401	54S51
00601	5482	02005	54L04	04301	93L18	07402	54S64
00602	5483	02006	54L01/54L03	04401	93L24	07403	54S65
00603	9304‡	02101	54L71	04501†	93L14	07501	54S86
00604	5480	02102	54L72	04502†	93L08	07502	54S135
00701	5486	02103	54L73	04601	93L09	07601†	54S194
00801	5406	02104	54L78	04602	93L12	07602†	54S195
00802	5416	02105	54L74	04603	93L22	07701†	54S138
00803	5407	02201	54H72	05001	4011A	07702†	54S139
00804	5417	02202	54H73	05002	4012A	07703†	54S280
00805	5426	02203	54H74	05003	4023A	07801	54S181
00901	5495	02204	54H76	05101	4013A	07802	54S182
00902	5496	02205	54H101	05102	4027A	07901	54S151
00903	54164	02206	54H103	05201	4000A	07902	54S153
00904	54165	02301	54H30	05202	4001A	07903	54S157
00905	54194	02302	54H20	05203	4002A	07904	54S158
00906	54195	02303	54H10	05204	4025A	07905	54S251
00907†	9300‡	02304	54H00	05301	4007A	07906	54S257
00908†	9328	02305	54H04	05302	4019A	07907	54S258
00909†	54198	02306	54H01	05303	4030A	08001	54S11
00910†	54166	02307	54H22	05401	4008A	08002	54S15
01001	5442	02401	54H40	05501	4009A	08003†	54S08
01002	5443	02501	54L90	05502	4010A	08004†	54S09
01003	5444	02502	54L93	05503	4049A	08101	54S140
01004	5445	02503	54L193	05504	4050A	08201	54S85
01005	54145	02504	93L10	05505	4041A	10101	uA741
01006	5446	02505	93L16	05601	4017A	10102	uA747
01007	5447	02601	54L86	05602	4018A	10103	LM101A
01008	5448	02701	54L02	05603	4020A	10104	LM108A
01009	5449	02801	54L95	05604	4022A	10105	LH2101A
01101	54181	02802	54L164	05605	4024A	10106	LH2108A
01102	54182	02803	93L28‡	05701	4006A	10107	LM118
01201	54121	02804	93L00	05702	4014A	10201	uA723
01202	54122	02805	76L70	05703	4015A	10202†	LM104
01203	54123	02806♦	54L91	05704	4021A	10203†	LM105
01204	9601	02901	54L42	05705	4031A	10301	uA710
01205	9602	02902	54L43	05706	4034A	10302	uA711
01301	5492	02903	54L44	05801†	4016A	10303	LM106
01302	5493	02904	54L46	06001	10501‡	10304	LM111
01303	54160	02905	54L47	06002	10502‡	10305†	LM2111
01304	54163	02906	76L42A	06003	10505‡	10401	55107
01305	54162	02907	93L01	06004	10506‡	10402	55108
01306	54161						

NOTE: Only the basic JAN and commercial numbers are shown.

† Slash sheets not released as of date of this publication.

‡ Not recommended for new designs.

♦ Class S only.

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TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN. /NO.	CKT TYPE	JAN. /NO.	CKT TYPE	JAN. /NO.	CKT TYPE	JAN. /NO.	CKT TYPE
10403	55114	15802	9317	30104	54LS113	31001	54LS11
10404	55115	15901	9300	30105	54LS114	31002	54LS15
10405	55113	15902	9328	30106	54LS174	31003	54LS21
10406	7831	16001	9334	30107	54LS175	31004	54LS08
10407	7832	16101	5432	30108	54LS107	31101	54LS85
10501†	uA733	16201	5428	30109	54LS109	31201†	54LS83A
10601	LM102‡	20101	54186 (PROM 512)	30110	54LS76	31202†	54LS283
10602	LM110	20102	MCM5304‡	30201	54LS40	31301	54LS13
10603†	LM2110	20103†	IM5603A	30202	54LS37	31302	54LS14
10701	LM109	20201†	IM5603 (PROM 1024)	30203	54LS38	31303	54LS132
10702†	LM140-12	20202†	IM5623	30204	54LS28	31401†	54LS123
10703†	LM140-15	20301†	AM27S10	30301	54LS02	31402†	54LS221
10704†	LM140-24	20302†	AM27S11	30302	54LS27	31403†	54LS122
10801	3018A	20401†	IM5604	30303	54LS266	31501†	54LS90
10802	3045	20402†	IM5624	30401	54LS51	31502†	54LS93
10901†	SE555	20501†	HHX7620-8	30402	54LS54	31503†	54LS160
10902†	SE556	20502†	HMX7621-8	30501	54LS32	31504†	54LS161
15001	5485	20601†	HMX7640-8	30502	54LS86	31505†	54LS168
15101	5413	20602†	HMX7641-8	30601†	54LS194	31506†	54LS169
15102	5414	23001†	93410 (256 RAM)	30602†	54LS195	31507†	54LS192
15103	54132	23002†	93411 (256 RAM)	30603†	54LS95	31508†	54LS193
15201	54154	23003†	93421	30604†	54LS96	31509†	54LS191
15202	54155	23501	TMS4060 (4K RAM)	30605†	54LS164	31510†	54LS92
15203	54156	23502	TMS4050 (4K RAM)	30606†	54LS295	31511†	54LS162
15204	8250	23503	TMS4060 (4K RAM)	30607†	54LS395	31512†	54LS163
15205	8251	23504	TMS4050 (4K RAM)	30701†	54LS138	31513†	54LS190
15206	8252	30001	54LS00	30702†	54LS139	31601†	54LS75
15301	54125	30002	54LS03	30703†	54LS42	31602†	54LS279
15302	54126	30003	54LS04	30704†	54LS47	31701†	54LS124
15401†	54120	30004	54LS05	30801	54LS181	31702†	54LS324
15501	54H08	30005	54LS10	30901†	54LS151	31801†	54LS261
15502	54H11	30006	54LS12	30902†	54LS153	31901†	54LS670
15503	54H21	30007	54LS20	30903†	54LS157	32001†	54LS196
15601	54147	30008	54LS22	30904†	54LS158	32002†	54LS197
15602	54148	30009	54LS30	30905†	54LS251	32003†	54LS290
15603	9318‡	30101	54LS73	30906†	54LS257	32004†	54LS293
15701	9338	30102	54LS74	30907†	54LS258	32102†	54LS26
15801	9321	30103	54LS112	30908†	54LS253		

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NOTE: Only the basic JAN and commercial numbers are shown.

† Slash sheets not released as of date of this publication.

‡ Not recommended for new designs.

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

TTL 54 SERIES

CKT TYPE	JAN /NO.
5400	00104
5401	00107
5402	00401
5403	00109
5404	00105
5405	00108
5406	00801
5407	00803
5408	01601
5409	01602
5410	00103
5412	00106
5413	15101
5414	15102
5416	00802
5417	00804
5420	00102
5423	00402
5425	00403
5426	00805
5427	00404
5428	16201
5430	00101
5432	16101
5437	00302
5438	00303
5440	00301
5442	01001
5443	01002
5444	01003
5445	01004
5446	01006
5447	01007
5448	01008
5449	01009
5450	00501
5451	00502
5453	00503
5454	00504
5470	00206
5472	00201
5473	00202
5474	00205
5475	01501
5476	00204
5477	01502
5480	00604
5482	00601
5483	00602
5485	15001
5486	00701
5490	01307
5492	01301
5493	01302
5495	00901
5496	00902
54107	00203
54116	01503
54120	15401†
54121	01201
54122	01202
54123	01203
54125	15301
54126	15302

CKT TYPE	JAN /NO.
54132	15103
54145	01005
54147	15601
54148	15602
54150	01401
54151	01406
54153	01403
54154	15201
54155	15202
54156	15203
54157	01405
54160	01303
54161	01306
54162	01305
54163	01304
54164	00903
54165	00904
54166	00910†
54173	01703†
54174	01701
54175	01702
54177	01312†
54180	01901
54181	01101
54182	01102
54186	20101
54192	01308
54193	01309
54194	00905
54195	00906
54196	01310†
54197	01311†
54198	00909†

TTL 54H SERIES

CKT TYPE	JAN /NO.
54H00	02304
54H01	02306
54H04	02305
54H08	15501
54H10	02303
54H11	15502
54H20	02302
54H21	15503
54H22	02307
54H30	02301
54H40	02401
54H50	04001
54H51	04002
54H53	04003
54H54	04004
54H55	04005
54H72	02201
54H73	02202
54H74	02203
54H76	02204
54H101	02205
54H103	02206

TTL 54L SERIES

CKT TYPE	JAN /NO.
54L00	02004
54L01	02006
54L02	02701
54L03	02006
54L04	02005
54L10	02003
54L20	02002
54L30	02001
54L42	02901
54L43	02902
54L44	02903
54L46	02904
54L47	02905
54L51	04101
54L54	04102
54L54	04104♦
54L55	04103
54L71	02101
54L72	02102
54L73	02103
54L74	02105
54L78	02104
54L86	02601
54L90	02501
54L91	02806♦
54L93	02502
54L95	02801
54L121	04201
54L122	04202
54L164	02802
54L193	02503

TTL 54LS SERIES

CKT TYPE	JAN /NO.
54LS00	30001
54LS02	30301
54LS03	30002
54LS04	30003
54LS05	30004
54LS08	31004
54LS10	30005
54LS11	31001
54LS12	30006
54LS13	30301
54LS14	31302
54LS15	31002
54LS20	30007
54LS21	31003
54LS22	30008
54LS26	32102†
54LS27	30302
54LS28	30204
54LS30	30009

CKT TYPE	JAN /NO.
54LS32	30501
54LS37	30202
54LS38	30203
54LS40	30201
54LS42	30703†
54LS47	30704†
54LS51	30401
54LS54	30402
54LS73	30101
54LS74	30102
54LS75	31601†
54LS76	30110
54LS83A	31201
54LS85	31101
54LS86	30502
54LS90	31501†
54LS92	31511†
54LS93	31502†
54LS95	30603†
54LS96	30604†
54LS107	30108
54LS109	30109
54LS112	30103
54LS113	30104
54LS114	30105
54LS122	31403†
54LS123	31401†
54LS132	31303
54LS138	30701†
54LS139	30702†
54LS151	30901†
54LS153	30902†
54LS157	30903†
54LS158	30904†
54LS160	31503†
54LS161	31504†
54LS162	31510†
54LS163	31512†
54LS164	30605†
54LS169	31506†
54LS174	30106
54LS175	30107
54LS181	30801
54LS190	31509†
54LS191	31513†
54LS192	31507†
54LS193	31508†
54LS194	30601†
54LS195	30602†
54LS196	32001†
54LS197	32002†
54LS221	31402†
54LS251	30905†
54LS253	30908†
54LS257	30906†
54LS258	30907†
54LS261	31801†
54SL266	30303
54LS279	31602†
54LS283	31202†
54LS290	32003†
54LS293	32004†
54LS295	30606†
54LS324	31702†
54LS395	30607†
54LS670	31901†

NOTE: Only the basic JAN and commercial numbers are shown.

†Slash sheets not released as of the date of this publication.

‡Not recommended for new designs.

♦Class S only.

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TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

TTL 54S SERIES CKT TYPE	JAN /NO.
54S00	07001
54S02	07301
54S03	07002
54S04	07003
54S05	07004
54S08	08003†
54S09	08004†
54S10	07005
54S11	08001
54S15	08002
54S20	07006
54S22	07007
54S30	07008
54S40	07201
54S51	07401
54S64	07402
54S65	07403
54S74	07101
54S85	08201
54S86	07501
54S112	07102
54S113	07103
54S114	07104
54S133	07009
54S134	07010
54S135	07502
54S138	07701†
54S139	07702†
54S140	08101
54S151	07901
54S153	07902
54S157	07903
54S158	07904
54S174	07105
54S175	07106
54S181	07801
54S182	07802
54S194	07601†
54S195	07602†
54S251	07905
54S257	07906
54S258	07907
54S280	07703†

MOS LSI CKT TYPE	JAN /NO.
TMS4050	23502 (4K RAM)
TMS4050	23504 (4K RAM)
TMS4060	23501 (4K RAM)
TMS4060	23503 (4K RAM)

LINEAR CONTROL SERIES CKT TYPE	JAN /NO.
LM101A	10103
LM104	10202†
LM105	10203†
LM106	10303
LM108A	10104
LM109	10701
LM111	10304
LM118	10107
LM140-12	10702†
LM140-15	10703†
LM140-21	10704†
SE555	10901†
SE556	10902†
uA710	10301
uA711	10302
uA723	10201
uA733	10501†
uA741	10101
uA747	10102

LINEAR INTERFACE SERIES CKT TYPE	JAN /NO.
55107	10401
55108	10402
55113	10405
55114	10403
55115	10404

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NOTE: Only the basic JAN and commercial numbers are shown.
†Slash sheets not released as of date of this publication.

38510/MACH IV

High-Reliability Microelectronics Procurement Specifications

MIL-STD-883

CONTENTS

REVISIONS

CLASSIFICATION (MAJOR/MINOR)	DATE CODE EFFECTIVITY	LTR	DESCRIPTION	DATE	APPROVED
Major	7040	A	Incorporate MIL-M-38510 and Revision Notice 2 of MIL-STD-883	8/15/70	
Major	7239	B	Incorporate Revision Notice 3 and 4 of MIL-STD-883 and Revision A of MIL-STD-38510	9/1/72	
Major	7401	C	Incorporate revised Level IV (SNH) processing with inclusion of recorded electrical data with delta requirements; incorporate technological criteria in Table III for precap of complex circuits.	1/1/74	
Minor	7518	D	Incorporate Revision A of MIL-STD-883 and provisions for MOS LSI and CMOS devices	4/15/75	
Minor	7628	E	Incorporate Revision C of MIL-M-38510 and MIL-STD-883 Revision A, Notice 2	6/15/76	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02
INTERPRET DWG. IN ACCORDANCE WITH STD. DESCRIBED IN MIL-STD-100
MATERIAL:

	DATE
DR	9/22/69
CHK	10/1/69
ENGR	10/2/69
QUALITY CONTROL	10/3/69
QRA MGR.	10/4/69
DESIGN ACTIVITY RELEASE DEPARTMENT MANAGER, TXL	
CIRCUITS DIVISION MANAGER	

TEXAS INSTRUMENTS INCORPORATED
SEMICONDUCTOR CIRCUITS DIVISION DALLAS, TEXAS

TITLE: MICROELECTRONICS, HIGH RELIABILITY PROCUREMENT SPECIFICATION (MIL-STD 38510/883)

SIZE	CODE IDENT NO	DRAWING NO.
A	01295	38510/MACH IV PROGRAM

SCALE | REV D | SHEET

38510/MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification, and processing of high-reliability monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits devices, general specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions

Detail Specifications

SNXXXX (Bipolar) TMSXXXX (MOS LSI) TFXXXX (CMOS)	Detail Specification for a Particular Part Type (e.g., Manufacturer's Data Sheet)

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extent specified herein.

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38510.
c)	MRN	Minimum reject number as defined by MIL-M-38510.
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
e)	Inspection Lot	An inspection lot shall be as defined in MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510.

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Process Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4

3.2 Process Conditioning, Testing and Screening

Three levels of screening and quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

SCREENING LEVEL	PART NUMBER PREFIX			APPLICABLE FLOW CHART
	BIPOLAR	CMOS	MOS LSI	
38510/883 Class A (Level IV)	SNH	Not Avail.	Not Avail.	Figure 4
38510/883 Class B (Level III)	SNC	TFC		Figure 3
			SMC	Figure 2
38510/883 Class C (Level I)	SNM	TFM	Not Avail.	Figure 1

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

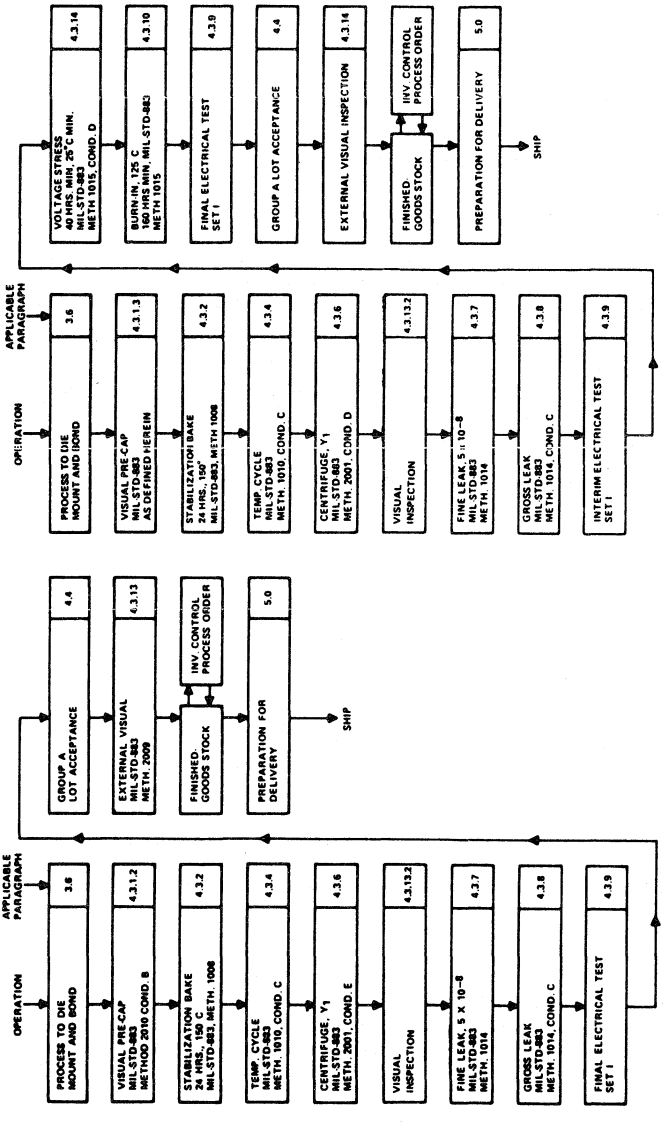

FIGURE 1–FLOW CHART FOR 38510 CLASS C LEVEL I

FIGURE 2–FLOW CHART FOR MOS LSI
38510 CLASS B (LEVEL III SMC)

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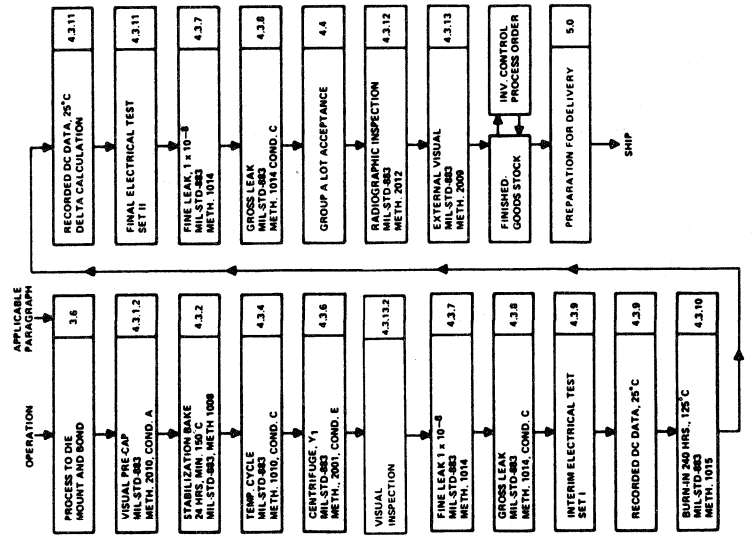

FIGURE 3–FLOW CHART FOR 38510 CLASS B LEVEL III

FIGURE 4–FLOW CHART FOR 38510 CLASS A LEVEL IV

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Selection

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 2003. (See note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) of 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose radius is less than 0.10 inch and no twist whose angle is greater than 30° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carriers shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable to Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-99, TO-100, and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual-in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) A lot date code indicating the week of initial submission for screening or inspection. The date code shall be as follows:

1) EIA four-digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) EIA three-digit date code (when limited by space available), the first number shall be the last digit of the year, the last two numbers shall indicate the calendar week.

d) Manufacturer's part number defining circuit type and applicable MIL-STD-883 screening level and MIL-M-38510 product assurance level as defined in paragraph 3.2.

e) Individual device serial number is required for Class A (SNH).

f) A dot to indicate acceptance by Radiographic inspection.

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

g) Country of origin shall be per U.S. Customs codes.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Controls

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The

procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satisfactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework provisions

3.7.3.1 Rework

All rework on micorcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 as defined herein.

3.7.3.2 Rebonding

Rebonding shall be in accordance with MIL-M-38510, as defined herein (see Note 6.5)

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Inspection and Testing Procedures Coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program established per paragraph 3.6 shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts excluding Groups B, C, and D destructive samples as defined by MIL-STD-883. All parts found to be defective, excluding devices exhibiting damage from use, may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, and testing of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

When specifically called out and funded on the purchase order or contract, the manufacturer's specific device qualification shall be based on compliance with the quality conformance test per Table III for MOS LSI devices. Qualification for other technologies shall be per Table I except that the testing will be to one LTPD level tighter than as defined in Table B-I of MIL-M-38510. For 38510 Class A (Level IV), qualification shall be per MIL-STD-883, Method 5005, Table IIa.

4.2.1.2 Procedures and Definitions

4.2.1.2.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1 shall be based on a random sampling technique and will be selected from a generic family.

4.2.1.2.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, TTL Schottky, DTL, CMOS, MOS metal-gate, or MOS silicon-gate, and differ only in the number or complexity of specified circuits that they contain. Generic family for linear circuits is defined by circuit function (e.g., op amp, comparator, etc.).

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housings (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection

Quality conformance inspections (Groups B, C, and D) are per Tables I and II. Table II shall apply to MOS LSI and Table I to other technologies.

a) When specifically called out and funded on the purchase order or contract, the manufacturer shall perform the quality conformance inspections (Groups B, C, and D) on a lot-by-lot basis.

b) The manufacturer shall, upon request, make available for review the following generic quality conformance inspection and data:

Group B – To be performed every six weeks on each package type (a different number of pins constitutes a different package) at each assembly location.

Group C – To be performed every three months on each generic family as defined in 4.2.1.2.2a and b.

Group D – To be performed every six months on each package type (a different number of pins constitutes a different package) at each assembly location.

4.2.2.1 Lot Acceptance Sampling

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Statistical sampling for quality conformance inspections shall be in accordance with MIL-M-38510 Table B-I.

Group B samples shall be selected from sublots that have successfully completed all of the 100% processing steps specified on the applicable process flow chart.

4.2.2.2 Resubmission of Failed Lots

When any lot (paragraph 4.2.2.a) submitted for quality conformance inspection fails any subgroup requirement, it may be resubmitted a maximum of one time for that particular subgroup. This additional submission is permitted, provided an analysis is performed to determine the failure mechanism for each reject device in the subgroup, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices

b) A defect that can effectively be removed by rescreening the lot

c) Random defects that do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When quality conformance inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Groups B, C, and D shall be stored and controlled by Quality Assurance. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Groups B, C, and D Test Data

All lot-by-lot data generated by Groups B, C, and D testing when specifically called out and funded on the purchase order, shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Attributes data for Groups C and D. Endpoints for each subgroup are electrical test parameters as defined in Tables I and II.

4.2.2.5 Precedure in Case of Test Equipment Failure or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 38510 Class C (Level I) and 38510 Class B (Level III) devices shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition B.

4.3.1.2 38510A Class A (Level IV) devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition A. (See notes 6.1.1.1 and 6.1.1.2.) (See notes under 6.1.2 for MOS LSI devices.)

4.3.1.3 Complex MSI and LSI circuits as defined in MIL-STD-883, Method 5004, paragraph 3.3 may be precap inspected per MIL-STD-883, Method 5004, paragraph 3.3.1 for 38510 Class B (Level III) and paragraph 3.3.2 for 38510 Class C (Level I).

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, for a minimum of 10 cycles. For MSI and LSI comples devices as defined in MIL-STD-883, Method 5004, paragraph 3.3, 50 cycles may be used in lieu of alternate pre-cap visual inspection criteria.

4.3.5 (Deleted)

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4.3.6 Centrifuge (Constant Acceleration)

The centrifuge test is used to determine the effects on microelectronics devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition E for devices having 20 or less pins and Condition D for those having more than 20 pins.

4.3.7 Fine Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B (Level III), and 38510 Class A (Level IV) screens shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross-Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B, (Level III) and 38510 Class A (Level IV) screens shall be subjected to the appropriate gross-leak test of paragraph 4.3.8.1 or 4.3.8.2, or an approved equivalent. The manufacturer may, at his option, perform gross-leak testing after the Set I Electrical Tests of paragraph 4.3.9.

4.3.8.1 When specifically called out and funded on the purchase order or contract, units will be bombed 2 hours minimum at 30 psig in FC-78, or equivalent. Units will then be immersed in FC-40 or equivalent at +125°C ±5°C for 30 seconds minimum and observed for for a definite stream of bubbles, more than two large bubbles, or an attached bubble that grows in size, per MIL-STD-883, Method 1014, Condition C2.

4.3.8.2 Units will be immersed in FC-40 or equivalent at +125°C ± 5°C for 30 seconds minimum and observed for a definite stream of bubbles, or more than two large bubbles per MIL-STD-883, Method 1014, Condition C1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of the data sheet. The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits. MOS LSI memory devices will be 100% tested both at 25°C and at high temperature. Linear circuits will be 100% dc tested at high and low temperatures and 25°C.

When specifically called out and funded on the purchase order or contract, the manufacturer shall perform subgroups 2, 3, and 4 of paragraph 4.4 in accordance with Method 5004 of MIL-STD-883.

4.3.10 Burn-In

The burn-in screen is performed for the purpose of eliminating marginal devices and early-life failures. Device biasing shall be in accordance with MIL-STD-883 Method 1015, Conditions A, D, or E for Digital Circuits and Conditions B, C, or D for Linear Circuits. For 38510 Class B (Level III) devices, equivalent test conditions using the time/temperature acceleration factor of Condition F between the temperature range of 125°C to 150°C may be used. For 38510 Class B (Level III) MSI and LSI complex devices as defined in MIL-STD-883 paragraph 3.3.1, a 240 hour burn-in in lieu of alternate pre-cap visual inspection criteria per MIL-STD-883, Method 5004, paragraph 3.3.1 may be used.

4.3.11 Final Electrical Test (Set II)

Each 38510 Class A (Level IV) integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: dc parameters at maximum and minimum rated temperatures, and switching parameters at 25°C. In addition, each bipolar device shall have critical 25°C dc electrical parameters read and recorded by serial number and shall pass the following delta requirements:

PARAMETER	DELTA LIMIT
V_{OL}	±10% of detail specification limit
V_{OH}	±10% of detail specification limit
I_{IL}	±10% of detail specification limit
I_{IH}	±10% of detail specification limit

CMOS recorded parameters and delta limits will be defined by the manufacturer as required.

One copy of the pre-burn-in and post-burn-in recorded data with delta calculations shall be shipped with each lot. Data will not be available for the metal flat pack (T). See MIL-M-0038510, Class S. The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-Ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. X-ray may be performed at any point after serialization at the manufacturer's option (see note 6.3).

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4.3.13 External Visual Inspection

4.3.13.1 The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.3.13.2 Visual inspection will be performed for catastrophic failures. Catastrophic failures are defined as missing leads, broken packages, and damaged lids.

4.3.14 Voltage Stress

Selected n-channel MOS LSI devices will be voltage stressed for 40 hours minimum at 25°C min per MIL-STD-883 Method 1015, Condition D.

4.4 Group A Conformance

Group A conformance shall consist of the electrical parameters in the manufacturer's data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to Group A, as specified.

SUBGROUP	LTPD (%) LEVEL I 38510C	LEVEL II	LEVEL III 38510B	LEVEL IV 38510A
Subgroup 1 25°C, dc	5	7	5	5
Subgroup 2 High Temperature, dc	10	10	7	5
Subgroup 3 Low Temperature, dc	10	10	7	5
Subgroup 4 Dynamic and Switching Tests @ 25°C	10	10	7	5

NOTES: Functional tests included in dc tests.
MOS LSI devices will be lot accepted at 25°C and high temperature.
The LTPD's of subgroups 1 and 2 will apply.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria.

TABLE 1
QUALITY CONFORMANCE TEST (GROUPS B, C, D)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B, C LTPD
GROUP B 1/			
Subgroup 1 Physical dimensions	2016		2 devices (no failures)
Subgroup 2 a. Resistance to solvents	2015		3 devices (no failures)
b. Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (no failures)
c. Bond strength 2/	2011		15
(1) Thermocompression		(1) Test condition D	
(2) Ultrasonic or wedge		(2) Test condition D	
Subgroup 3 Solderability 3/	2003	Soldering temperature of 260 ± 10°C.	15
GROUP C (Die Related Tests)			
Subgroup 1 Operating life test End point electrical parameters	1005	Test condition to be specified (1000 hours) As specified in the applicable device specification	5
Subgroup 2 Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E min. (see 3) Y_1 axis followed by one other axis X or Z.	
Seal (a) Fine	1014	As applicable	
(b) Gross 2/			
Visual examination	1/		
End-point electrical parameters		As specified in the applicable device specification	

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified, be randomly selected following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross-leak testing is utilized, test condition C_2 shall apply as minimum.

TABLE 1
QUALITY CONFORMANCE TEST (GROUPS B, C, D)
(continued)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B, C LTPD
GROUP D (Package Related Test)			
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2/			
Lead integrity	2004	Test condition B2 (lead fatigue)	15
Seal	1014	As applicable	
(a) Fine 2/			
(b) Gross 3/			
Subgroup 3/			
Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum.	15
Temperature cycling	1010	Test condition C, 100 cycles minimum.	
Moisture resistance	1004		
Seal	1014	As applicable	
(a) Fine 2/			
(b) Gross 3/			
Visual examination	5/		
End point electrical parameters		As specified in the applicable device specification.	
Subgroup 4/			
Mechanical shock	2002	Test condition B	15
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E (see 3)	
Seal	1014	As applicable	
(a) Fine 2/			
(b) Gross 3/			
Visual examination	6/		
End point electrical parameters	5005	Subgroups 1, 2, 3, and 7.	
Subgroup 5/			
Salt atmosphere	1009	Test condition A. Omit initial conditioning	15
Visual examination	7/		

1. Electrical reject devices from the same production lot may be used for samples.
2. Condition A or B per paragraph 3.7 herein.
3. When fluorocarbon gross leak testing is utilized; test condition C2 shall apply as minimum.
4. Devices used in subgroup 3, "Thermal and Moisture Resistance", may be used in subgroup 4, "Mechanical".
5. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
6. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
7. Visual examination shall be in accordance with paragraph 3.3.1 of method 1009.

TABLE II
QUALITY CONFORMANCE TEST
MOS LSI CIRCUIT

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Temperature Cycle	1010	Condition C	
Constant Acceleration	2001	Condition D[1], Y_1 Plane	
Electrical End Points	5005	Subgroup 1	15
Subgroup 2			
Operating Life	1005	Condition D, 500 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	10

1. Condition D for packages with more than 20 pins. Condition E for packages with 20 pins or less.

TABLE III
MANUFACTURER'S QUALIFICATION PROCEDURE
MOS LSI CIRCUITS

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B, C LTPD
GROUP B			
Subgroup 1			
Physical dimensions	2016		2 devices (no failures)
Subgroup 2			
a. Resistance to solvents	2015		3 devices (no failures)
b. Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (no failures)
c. Bond strength 2/	2011		15
(1) Thermocompression		(1) Test condition D	
(2) Ultrasonic or wedge		(2) Test condition D	
Subgroup 3			
Solderability 3/	2003	Soldering temperature of 260 ±10°C.	15

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified, be randomly selected following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

GROUP C (Die Related Tests)

Subgroup 1			
Operating life test	1005	T_A = 85°C, 1000 hours minimum	5
End point electrical parameters Subgroups 1, 2, 3, and 7	5005		
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E for package with $<$20 pins Test condition D for packages with $\geq$ 20 pins Y_1 axis followed by one other axis X or Z.	
Seal	1014	As applicable	
(a) Fine			
(b) Gross 2/			
Visual examination	1/		
End-point electrical parameters		As specified in the applicable device specification	

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross-leak testing is utilized, test condition C_2 shall apply as minimum.

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TABLE III
MANUFACTURER'S QUALIFICATION PROCEDURE
MOS LSI CIRCUITS
(continued)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B, C LTPD
GROUP D (Package Related Test)			
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2[1]			
Lead integrity	2004	Test condition B2 (lead fatigue)	15
Seal	1014	As applicable	
(a) Fine[2]			
(b) Gross[3]			
Subgroup 3[4]			
Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
Temperature cycling	1010	Test condition C, 100 cycles minimum.	
Moisture resistance	1004		
Seal	1014	As applicable	
(a) Fine[2]			
(b) Gross[3]			
Visual examination	2/ 5/		
End point electrical parameters		As specified in the applicable device specifications.	
Subgroup 4[4]			
Mechanical shock	2002	Test condition B	15
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E (see 3)	
Seal	1014	As applicable	
(a) Fine[2]			
(b) Gross[3]			
Visual examination	3/ 6/		
End point electrical parameters	5005	Subgroups 1, 2, 3, and 7.	
Subgroup 5[1]			
Salt atmosphere	1009	Test condition A. Omit initial conditioning	15
Visual examination	5/ 7/		

1. Electrical reject devices from the same production lot may be used for samples.
2. Condition A or B per paragraph 3.7 herein.
3. When fluorocarbon gross leak testing is utilized; test condition C2 shall apply as minimum.
4. Devices used in subgroup 3, "Thermal and Moisture Resistance", may be used in subgroup 4, "Mechanical".
5. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
6. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
7. Visual examination shall be in accordance with paragraph 3.3.1 of method 1009.

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads

b) Damaged header (packages)

c) All test data specified in section 4.0

d) Certificate of Compliance as specified in section 4.0

e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C, bulk pack. The containers shall be clearly marked with manufacturer's name or symbol.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other than U.S.A.

Procuring activity parts number

Purchase order number

Material nomenclature

Quantity

Lot number

Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010

The following criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010).

6.1.1 Preseal Visual Inspection, Test Condition B [38510 Class B (Level III) and 38510 Class C (Level I)].

6.1.1.1 Paragraph 3.2: a 20-PSI minimum blow-off prior to seal will be performed to meet the intent of a controlled environment.

6.1.1.2 For titanium-tungsten, gold, titanium-tungsten multilayered systems, the underlying metal is defined as the bottom titanium tungsten and the top layer is defined as gold.

6.1.2 Preseal Visual Inspection for MOS LSI devices (38510 Class B, level III SMC). When the alternate screening option of paragraph 3.3 of Method 5004 is applied, the following additional items are applicable:

6.1.2.1 Internal visual, Method 2010, Condition B: In addition to the changes indicated by paragraph 3.3.1 of Method 5004, the following additional clarifications and deletions are applicable as reflected in MIL-M-38510/235:

a) Metallization inspection shall be applicable to the top layer metal conductor (i.e., Al) and need not include "underlying conductors" such as poly-silicon.

b) Omit paragraphs 3.2.1.1 (b) through 3.2.1.1 (e), 3.2.1.2 (b) through 3.2.1.2 (e) and 3.2.3 (e) (Items 3.2.1.1 (f) and 3.2.3 (g) do not apply).

6.2 Interconnections

Circuit interconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm^2, including allowances for worst-case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 X-Ray Method 2012

Paragraph 3.9.2.2a(2) and (3) delete and replace with: "Cause for rejection shall be a single void in the bar attachment material opening two adjacent sides and exceeding 50% of the length of one side and 100% of the length of the other side."

6.4 Salt Atmosphere Test, Method 1009

Where package design considerations necessitate (such as 0.75-inch tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

6.5 Rebonding

Attempts to bond where only impressions have been made in the metal and where the bond did not make a physical attachment to the pad or post shall not be considered evidence of rebonding.

Supplement S–1

SUPPLEMENT S–1

* The 'B' revision devices are improved direct replacements.

ERRATA

Since initial publication of this Data Book, Texas Instruments has discontinued production of the following devices. Their Data Sheets are included in this edition for information only, and their inclusion represents no obligation on Texas Instruments to supply these devices.

SN55/7520
SN55/7522
SN55/7524
SN55/7528
SN75156
SN55180
SN75186
SN75187
SN55/75232
SN55/75234
SN55/75238
SN75270
SN75320
SN75321
SN75322
SN75328
SN75330
SN75350
SN75355
SN75364
SN75366
SN75370
SN75375
SN75401
SN75402
SN75403
SN75404
SN75411
SN75412
SN75413
SN75414
SN75416
SN75417
SN75418
SN75419
SN75441
SN75493
SN75496
SN75496A
SN75502A
SN75503A
SN75510
SN75511
SN75580

AMMENDED DATA SHEETS

The following Data Sheets have been amended. The latest Data Sheets are included in this Section.

SN55/75109A
SN55/75110A
SN75112
*SN75160B
*SN75161B
*SN75162B
*SN75163B
*SN75176B
*SN75177B
*SN75178B
SN75500
SN75501

*The 'B' revision devices are improved direct replacements.

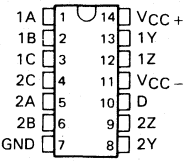
SN55109A, SN55110A, SN75109A, SN75110A, SN75112 DUAL LINE DRIVERS

D2106, DECEMBER 1975 – REVISED SEPTEMBER 1984

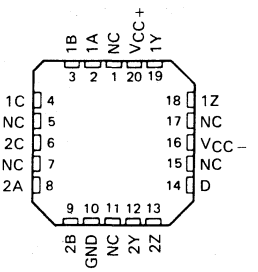
- Improved Stability over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range (−3 V to 10 V)
- TTL Input Compatibility
- Inhibitor Available for Driver Selection

−55°C to 125°C J or FK PACKAGE	0°C to 70°C J or N PACKAGE	OUTPUT FUNCTION
SN55109A	SN75109A	6-mA Current Switch
SN55110A	SN75110A	12-mA Current Switch
	SN75112	27-mA Current Switch

SN55109A, SN55110A . . . J DUAL-IN-LINE PACKAGE
SN75109A, SN75110A, SN75112 . . .
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN55109A, SN55110A . . . FK PACKAGE
(TOP VIEW)

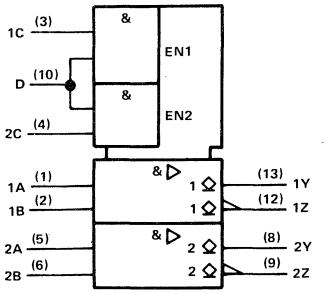


NC – No internal connection

description

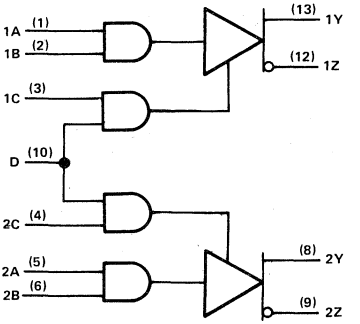
The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

description (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current is nominally 6 milliamperes for the '109A, 12 milliamperes for the '110A, and 27 milliamperes for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to 10 volts, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2.0 volts for high-logic-level input conditions and 0.8 volt for low-logic-level input conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

The SN55109A and SN55110A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75109A, SN75110A, and SN75112 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS†	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level, X = irrelevant

†When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

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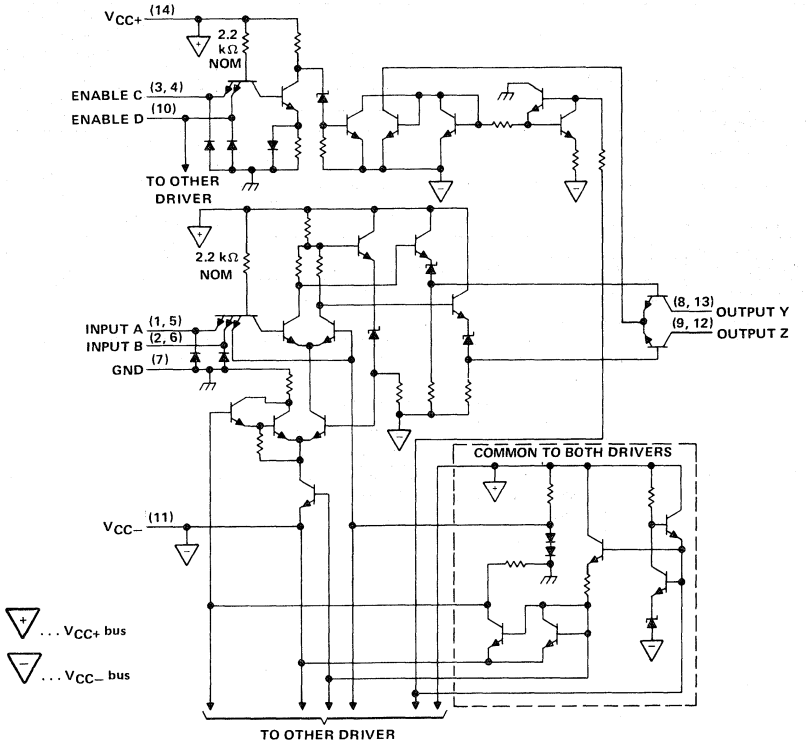
schematic (each driver)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55109A SN55110A	SN75109A SN75110A SN75112A	UNIT
Supply voltage, V_{CC+} (see Note 1)		7	7	V
Supply voltage, V_{CC-}		−7	−7	V
Input voltage, any input		5.5	5.5	V
Output voltage, any output		−5 to 12	−5 to 12	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	FK package	1375		mW
	J package	1375	1025	
	N package		875	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package			260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package, SN55109A and SN55110A chips are alloy mounted; SN75109A, SN75110A, and SN75112 chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
FK	1375 mW	11.0 mW/°C	25°C
J (Alloy-Mounted Chip)	1375 mW	11.0 mW/°C	25°C
J (Glass-Mounted Chip)	1025 mW	8.2 mW/°C	25°C
N	875 mW	7.0 mW/°C	25°C

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recommended operating conditions (see Note 3)

		SN55109A, SN55110A			SN75109A, SN75110A SN75112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC+}	$T_A \geq 0°C$	4.5	5	5.5	4.75	5	5.25	V
	$T_A < 0°C$	4.75	5	5.5				
Supply voltage V_{CC-}	$T_A \geq 0°C$	−4.5	−5	−5.5	−4.75	−5	−5.25	V
	$T_A < 0°C$	−4.75	−5	−5.5				
Positive common-mode output voltage		0		10	0		10	V
Negative common-mode output voltage		0		−3	0		−3	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A, SN75109A			SN55110A, SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_I = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	μA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				−10			−17			−32		

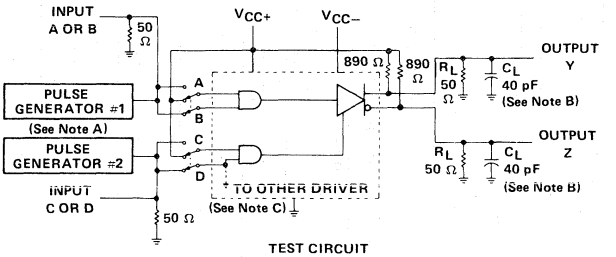
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

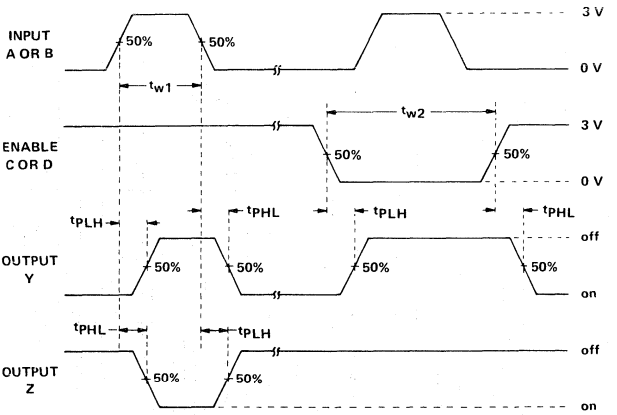
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

†t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = t_f = 10 ±5 ns, t_{w1} = 500 ns, PRR ≤ 1 MHz, t_{w2} = 1 μs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the enable connections are shown.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

SN55109A, SN75109A

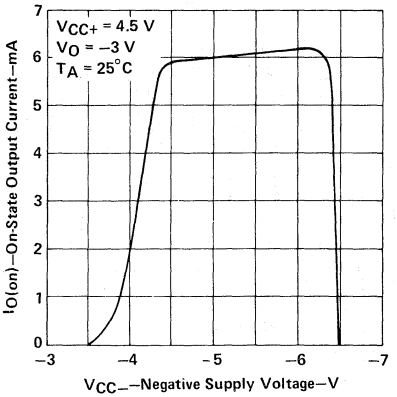


FIGURE 2

SN55110A, SN75110A

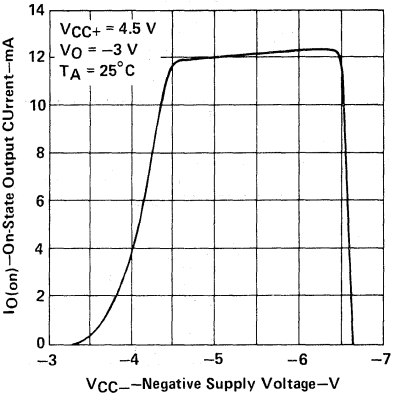


FIGURE 3

SN75112

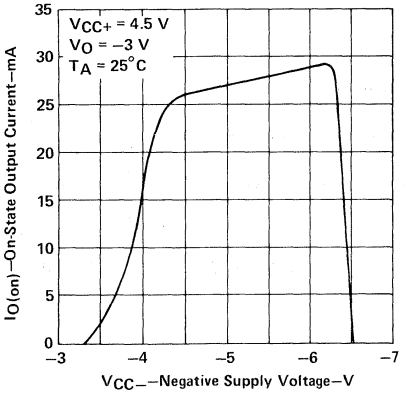


FIGURE 4

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TYPICAL APPLICATION DATA

special pulse-control circuit

Figure 5 shows a circuit that may be used as a pulse generator output or in many other testing applications.

INPUT	OUTPUTS	
A	Y	Z
HIGH	OFF	ON
LOW	ON	OFF

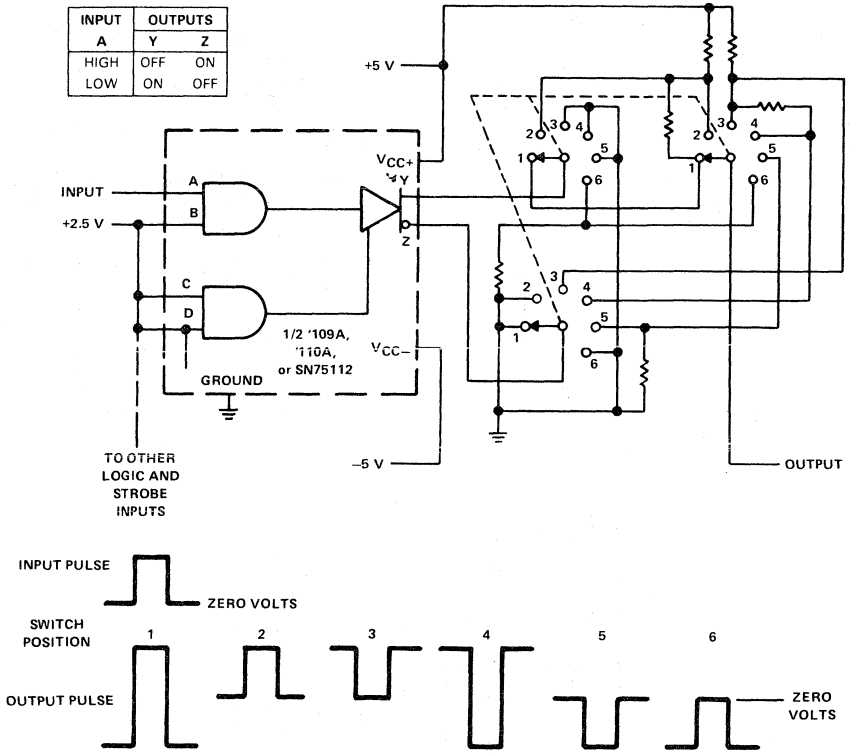

FIGURE 5. PULSE CONTROL CIRCUIT

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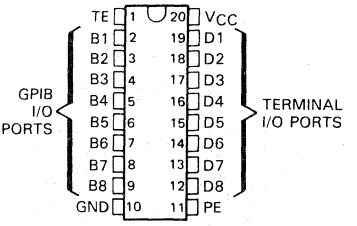
TEXAS INSTRUMENTS

D2525, OCTOBER 1985

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

DW, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0 volts. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

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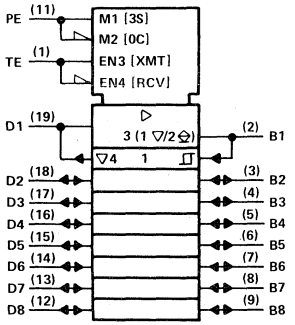
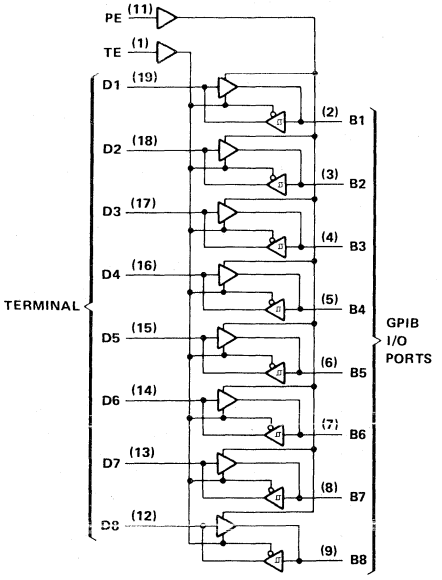
logic symbol†



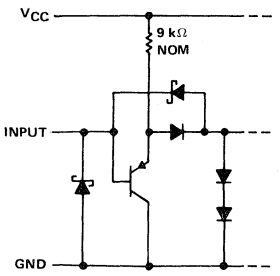
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽Designates 3-state outputs.
◇Designates passive-pullup outputs.

logic diagram (positive logic)

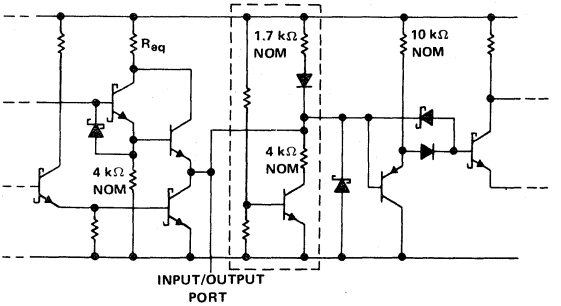


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 9.0 mW/°C, the N package at the rate of 9.2 mW/°C, and the J package at the rate of 11.0 mW/°C. In the J package, SN75160B chips are alloy mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

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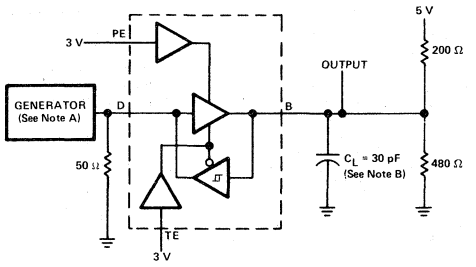
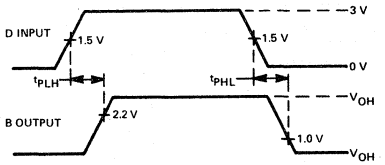
PARAMETER MEASUREMENT INFORMATION

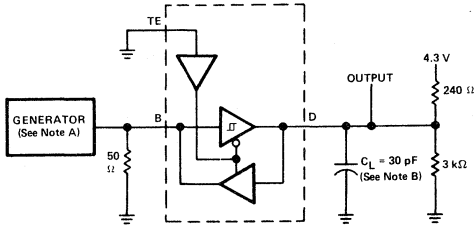


TEST CIRCUIT

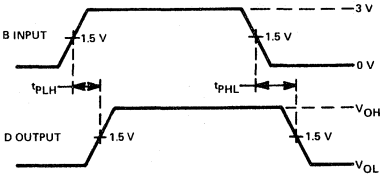


VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

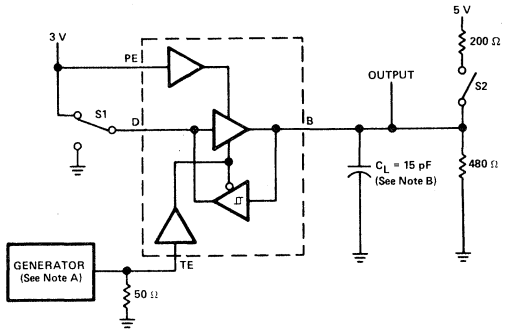


TEST CIRCUIT

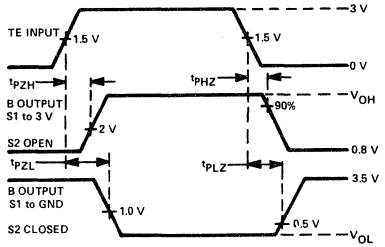


VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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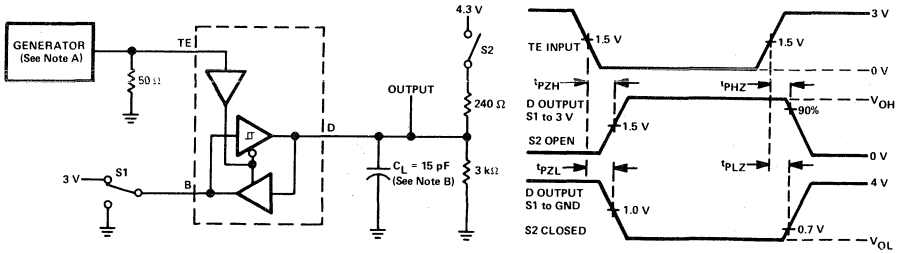
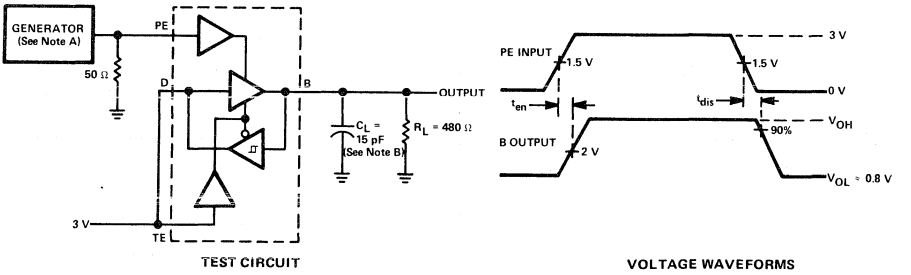
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

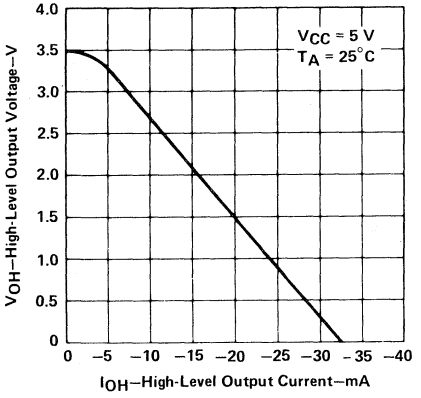

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

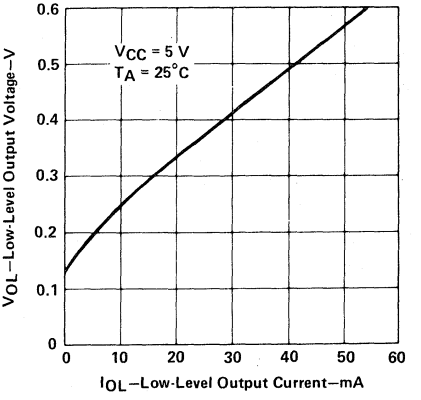

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

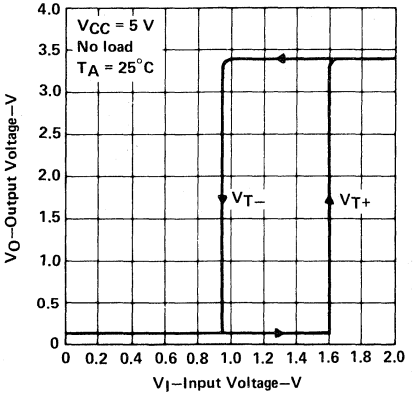

FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

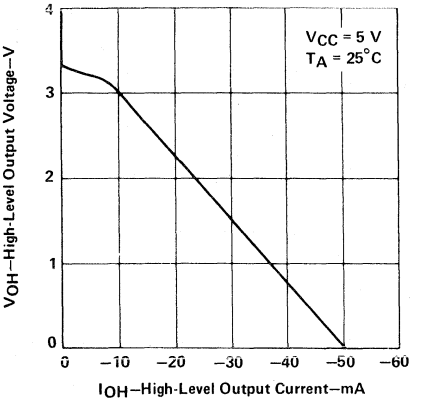


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

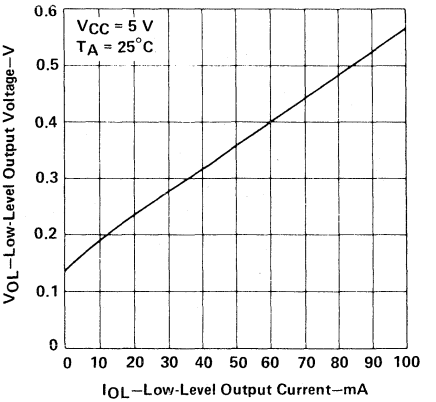


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

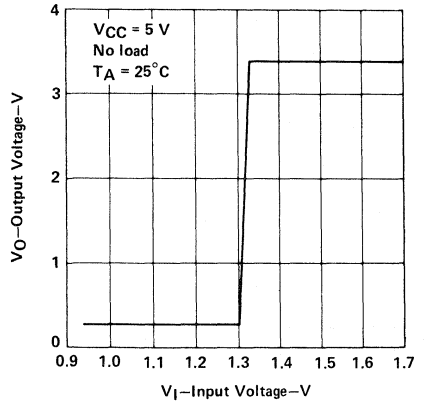


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

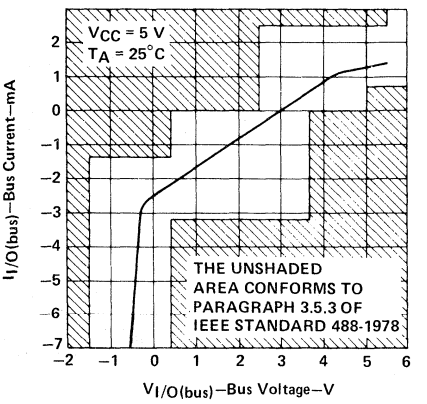


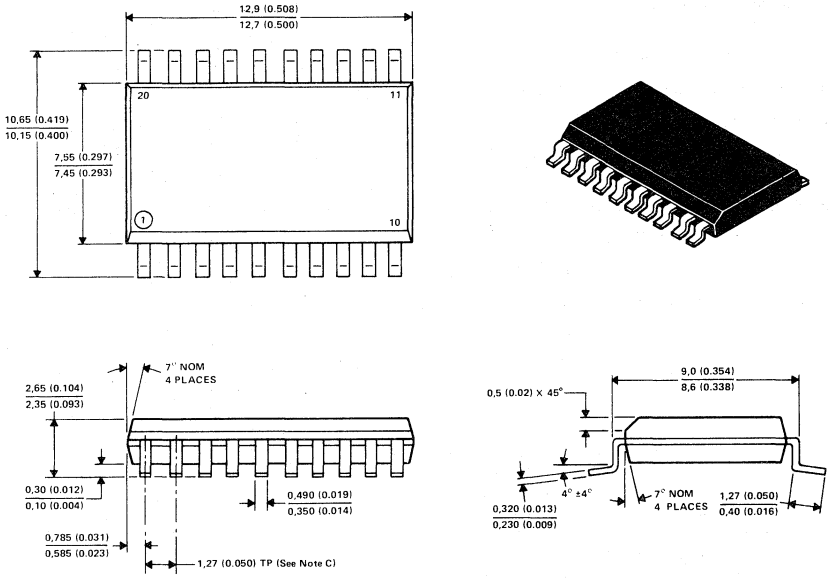
FIGURE 12

12

MECHANICAL DATA

DW plastic dual-in-line package

20-PIN DW PLASTIC



NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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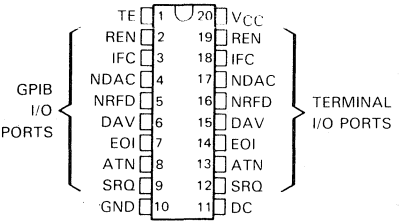
D2618, OCTOBER 1980 REVISED OCTOBER 1985

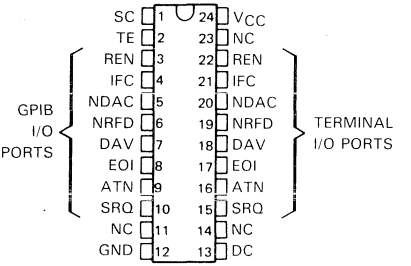
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multi-Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

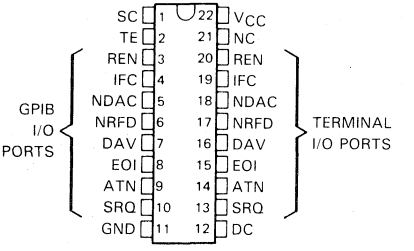
SN75161B . . . DW, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75162B . . . DW DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75162B . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC – No internal connection.

description

The SN75161B and SN75162B eight-channel general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75161B and SN75162B each features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power up/down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power-up and power-down. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

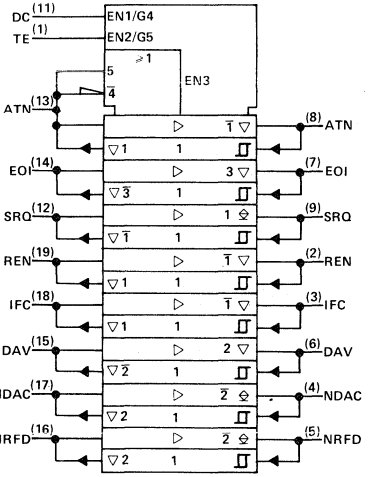
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

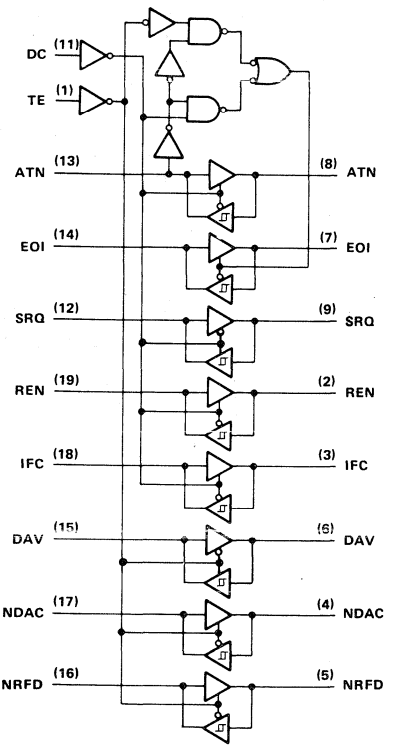
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162B only)	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

SN75161B logic symbol†



† This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.
▽designates 3-state output, ⏀designates passive-pullup outputs.

SN75161B logic diagram (positive logic)



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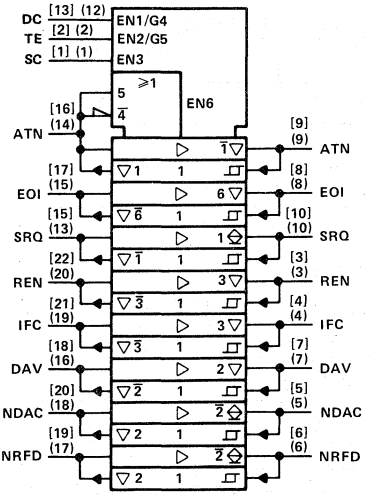
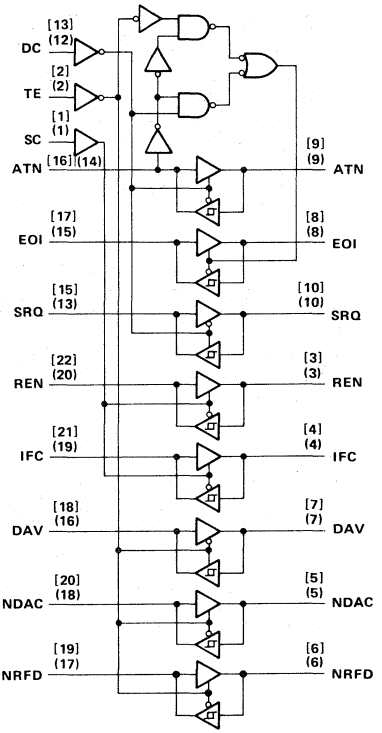
SN75162B logic symbol†



† This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.
▽designates 3-state output, ⏀designates passive-pullup outputs.

SN75162B logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

SN75161B
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162B
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

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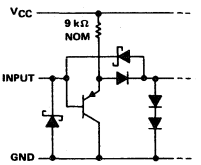
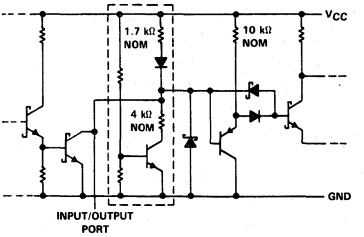
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

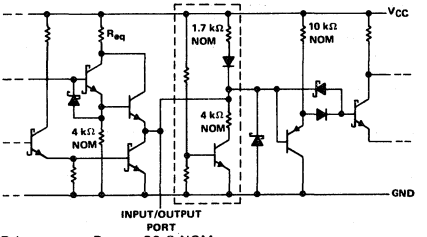


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
- DW package (20 pin) . . . . . 1125 mW
- DW package (24 pin) . . . . . 1350 mW
- J package . . . . . 1375 mW
- N package (20 pin) . . . . . 1150 mW
- N package (22 pin) . . . . . 1700 mW

Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the 20-pin DW package at the rate of 9.0 mW/°C, the 24-pin DW package at the rate of 10.8 mW/°C, the 20-pin N package at the rate of 9.2 mW/°C, the 22-pin N package at the rate of 13.6 mW/°C, and the J package at the rate of 11.0 mW/°C. In the J package, SN75161B chips are alloy mounted.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load, TE, DC, and SC low				110	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡V_{OH} applies for three-state outputs only.

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switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

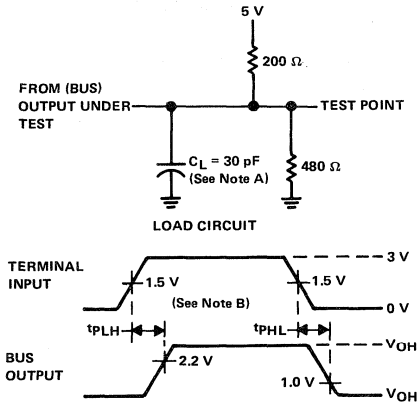


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

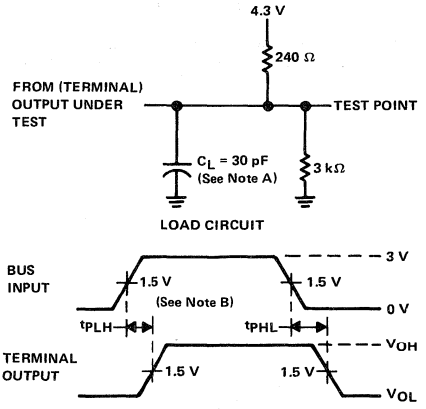
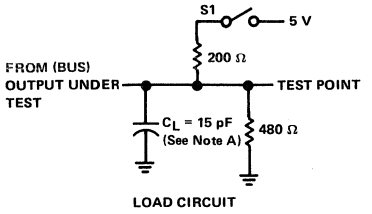


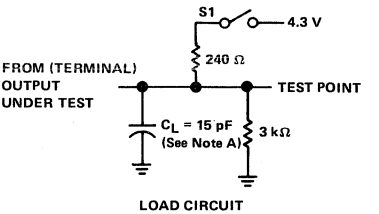
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

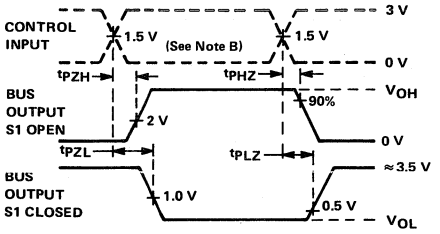
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

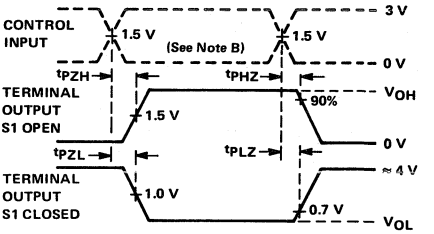


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

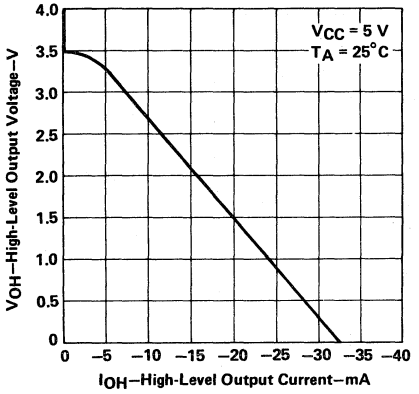

FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

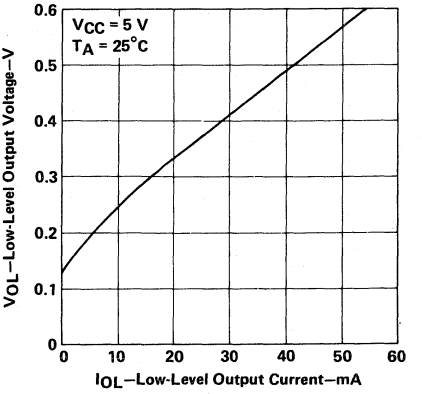

FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

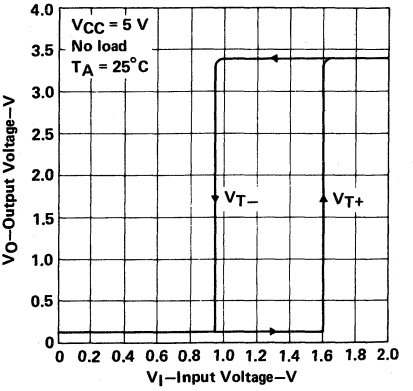

FIGURE 7

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

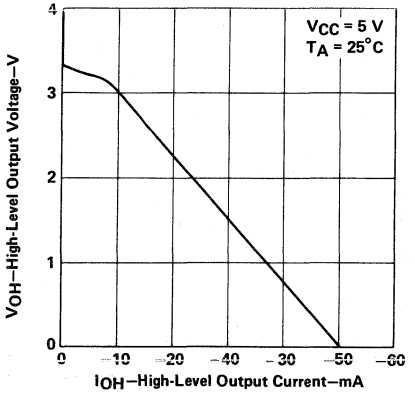


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

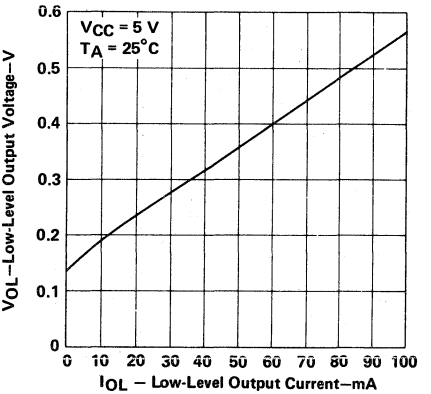


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

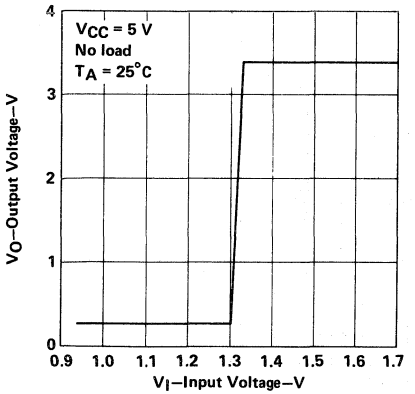


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

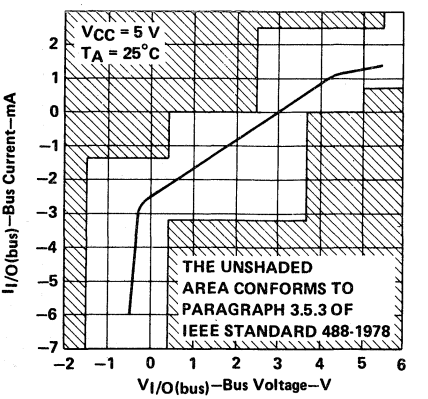


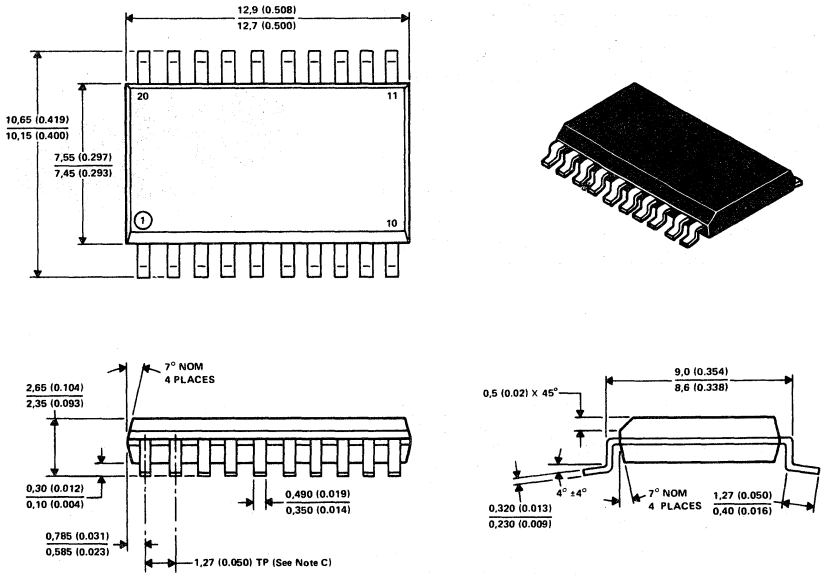
FIGURE 11

12

MECHANICAL DATA

DW plastic dual-in-line package

20-PIN DW PLASTIC



NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are with 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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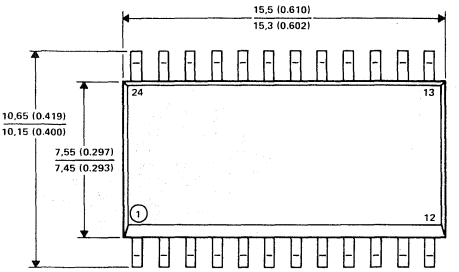
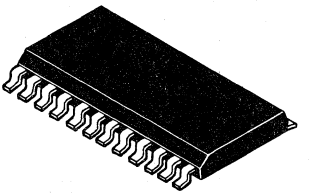
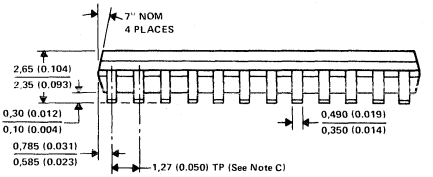
MECHANICAL DATA

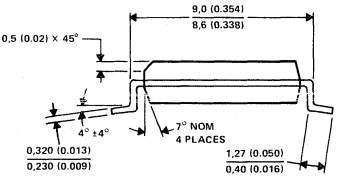
DW plastic dual-in-line package

24-PIN DW PLASTIC









NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not excees 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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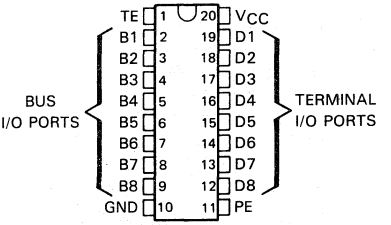
TEXAS INSTRUMENTS

D2611, OCTOBER 1985

- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed Low-Power Schottky Circuitry
- Low Power Dissipation . . . 66 mW Max per Channel
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

DW, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or three-state modes. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 millivolts of guaranteed hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0 volts.

The SN75163B is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high-impedance state.

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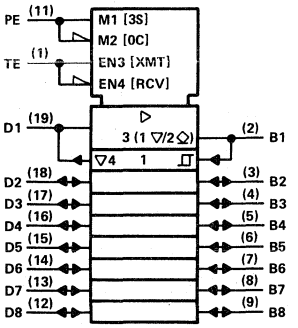
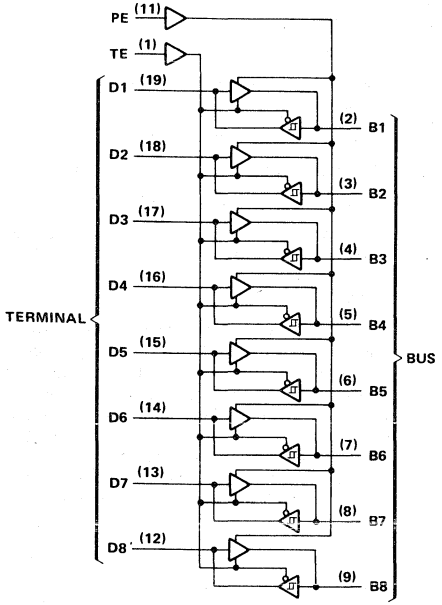
logic symbol†



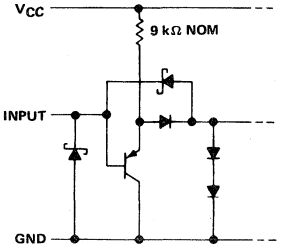
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
◇ Designates open-collector outputs.

logic diagram (positive logic)

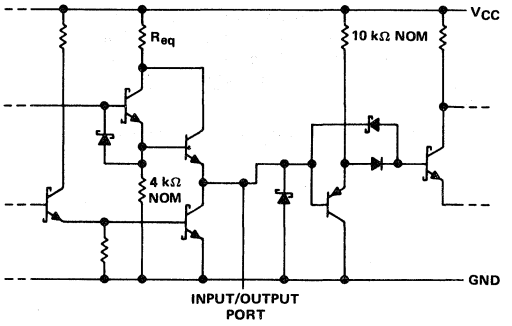


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 9.0 mW/°C, the N package at the rate of 9.2 mW/°C, and the J package at the rate of 11.0 mW/°C. In the J package, SN75163B chips are alloy mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−10	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature range, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled			80	mA
				Drivers low and enabled			100	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5, T_A = 25°C.

‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Terminal	See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

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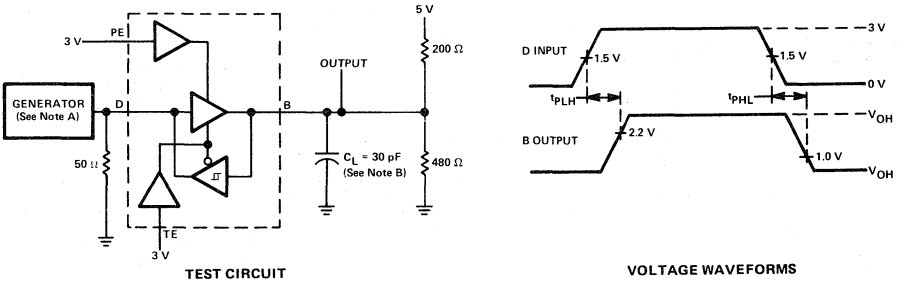
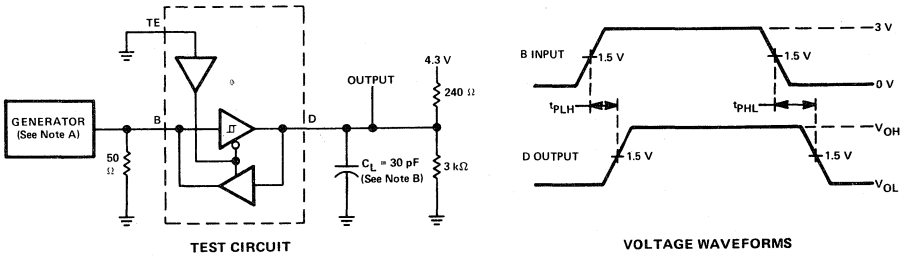
PARAMETER MEASUREMENT INFORMATION



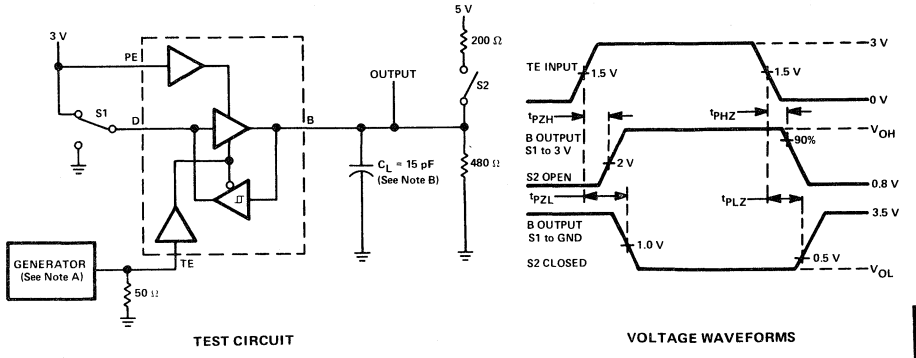
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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PARAMETER MEASUREMENT INFORMATION

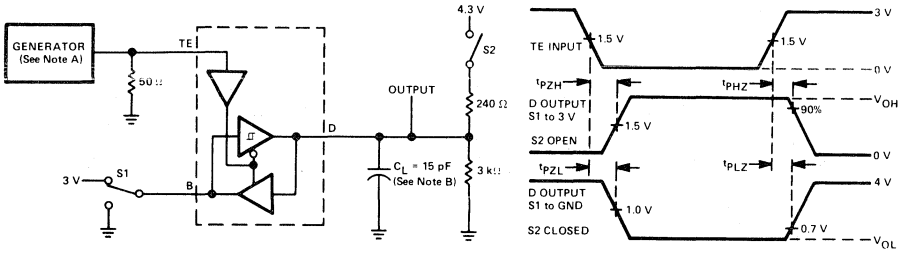

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

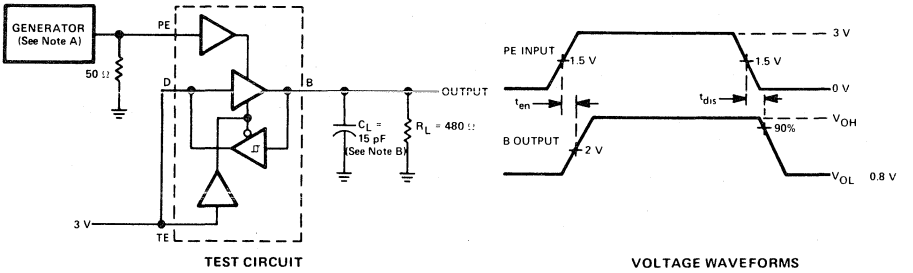

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

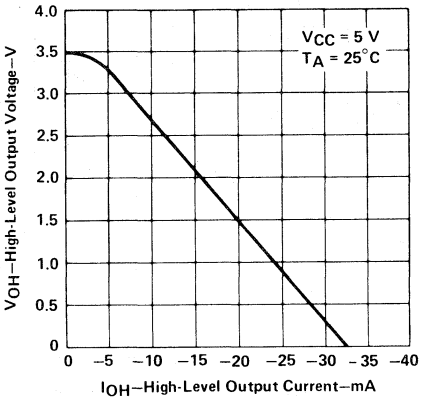

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

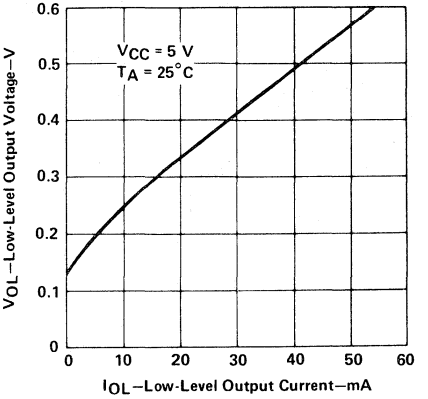

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

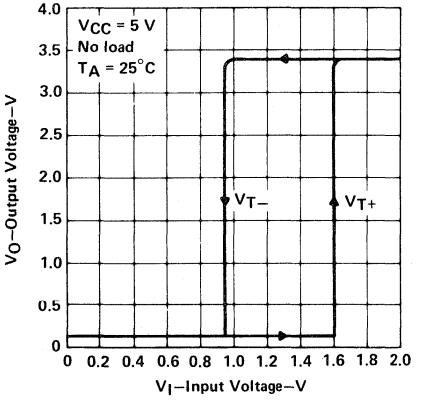

FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

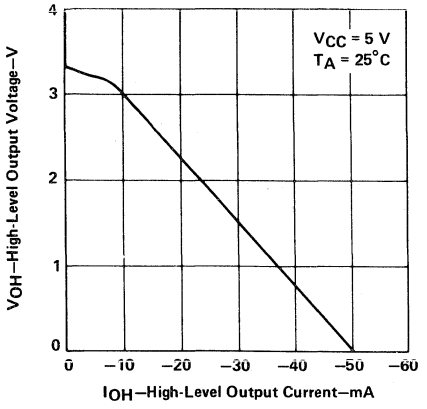


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

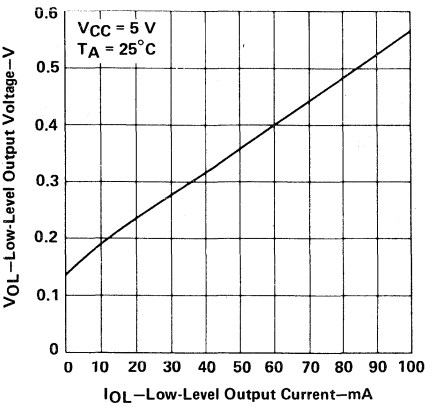


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

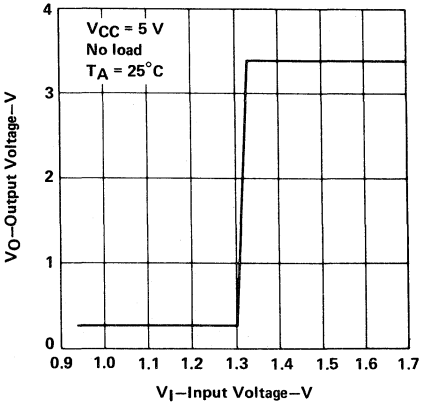


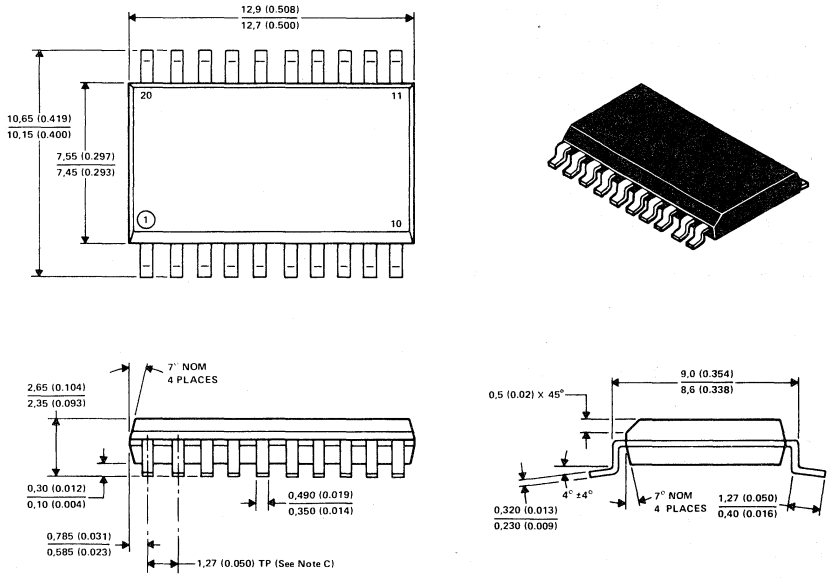
FIGURE 11

12

MECHANICAL DATA

DW plastic dual-in-line package

20-PIN DW PLASTIC



NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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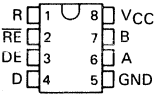
SN75176B DIFFERENTIAL BUS TRANSCEIVER

D2619, JULY 1985

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

D, JG, OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

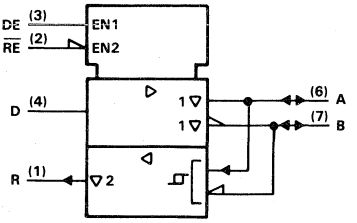
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN75176B differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27.

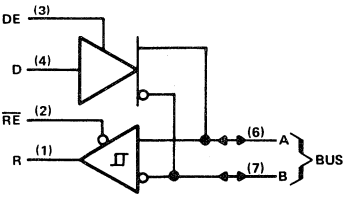
The SN75176B combines a three-state differential line driver and a differential input line receiver both of which operate from a single 5-volt power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0 volts. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617-12.

logic diagram (positive logic)



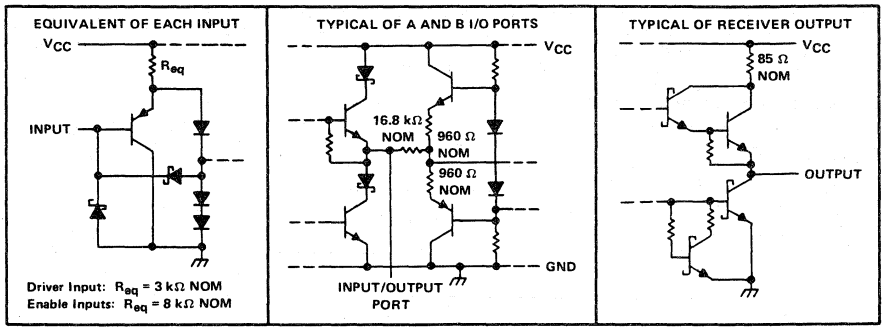
12

TEXAS INSTRUMENTS

The driver is designed to handle loads up to 60 milliamperes of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 millivolts, and a typical input hysteresis of 50 millivolts.

The SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D Package . . . . . 725 mW
JG Package . . . . . 825 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, and derate the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75176B chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7†		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

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DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			
				2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Ouputs enabled		57	70	mA
			Outputs disabled		26	35	

†The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 4. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
5. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3		15	22	ns
t_{TD}	Differential-output transition time			20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 6	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 6: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

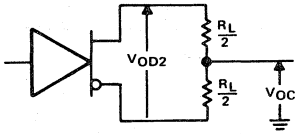

FIGURE 1. DRIVER V_{OD} AND V_{OC}

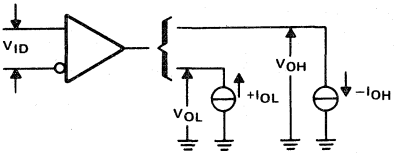

FIGURE 2. RECEIVER V_{OH} AND V_{OL}

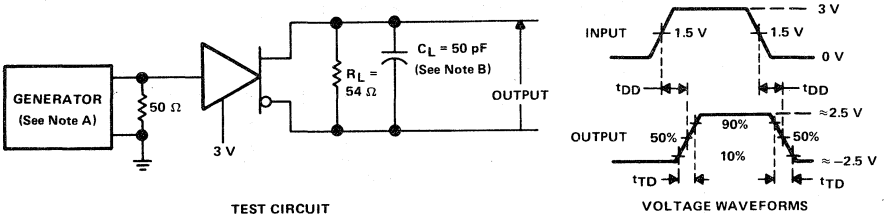

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

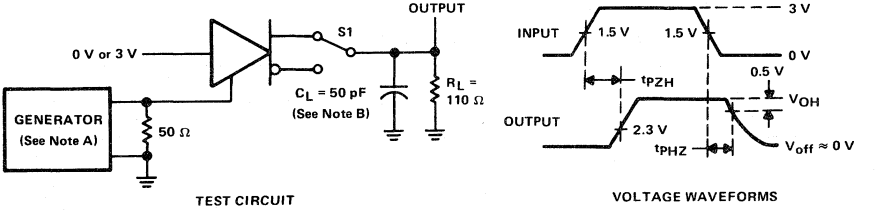

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

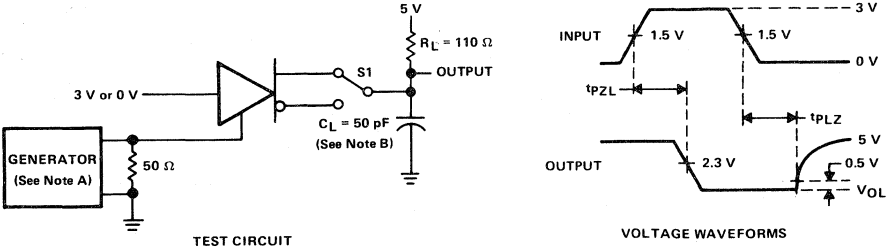

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_F ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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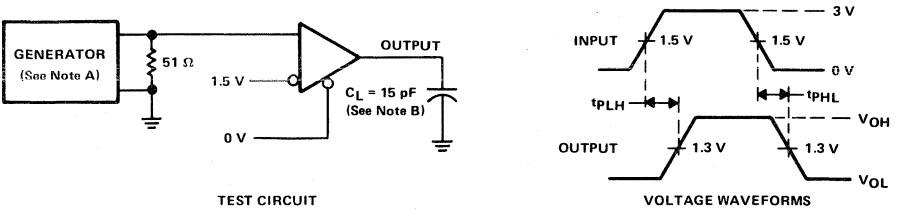
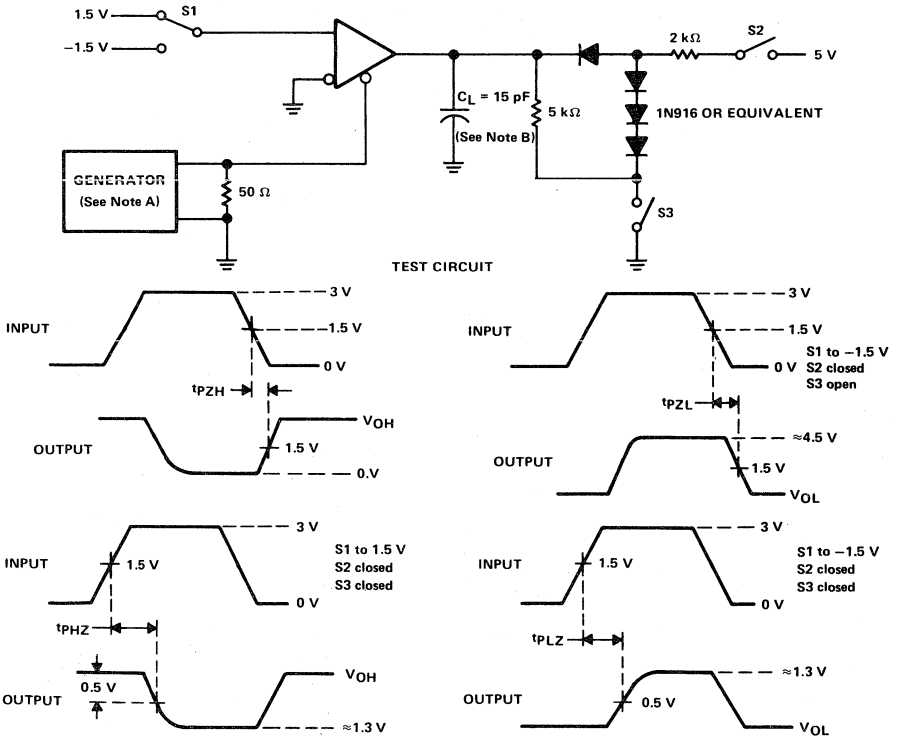
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 6. RECEIVER PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_F ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

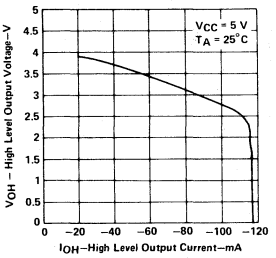


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

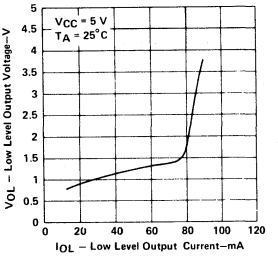


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

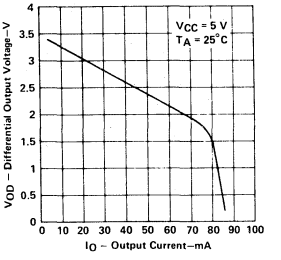


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

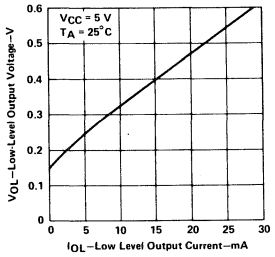


FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

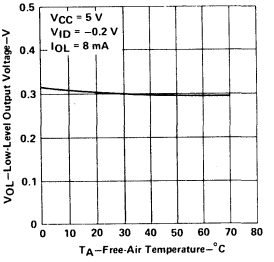


FIGURE 12

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

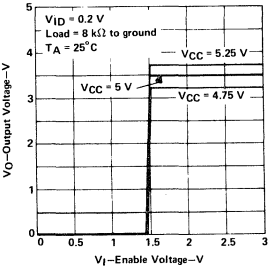


FIGURE 13

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

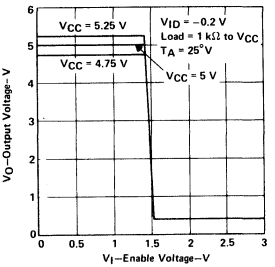


FIGURE 14

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TYPICAL APPLICATION

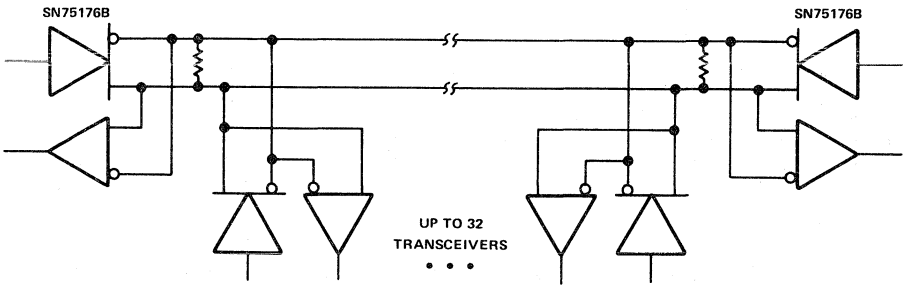


FIGURE 15. TYPICAL APPLICATION CIRCUIT

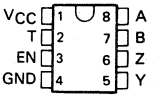
NOTE 7: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

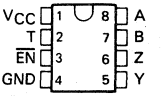
D2606, JULY 1985

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

SN75177B . . . D, JG, OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75178B . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75177B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE EN	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

SN75178B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE $\overline{EN}$	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = impedance (off)

description

The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

The SN75177B and SN75178B feature positive- and negative-current limiting three-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −7 volts to 12 volts. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The driver is designed to drive current loads up to 60 milliamperes maximum.

The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceivers.

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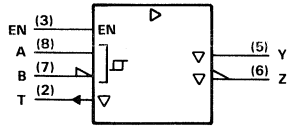
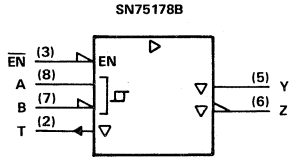
logic symbols†

SN75177B



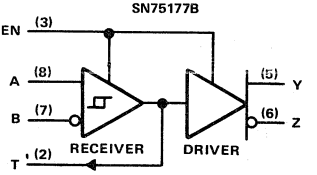
SN75178B



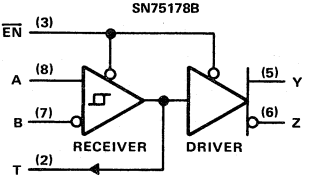
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

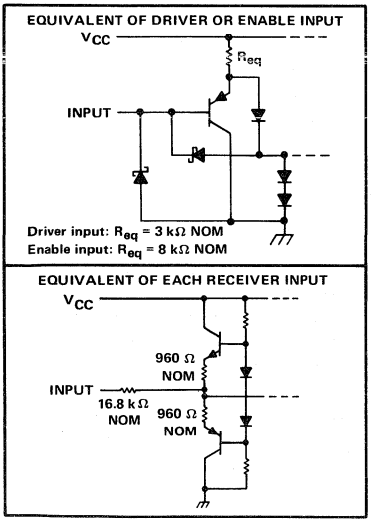
SN75177B

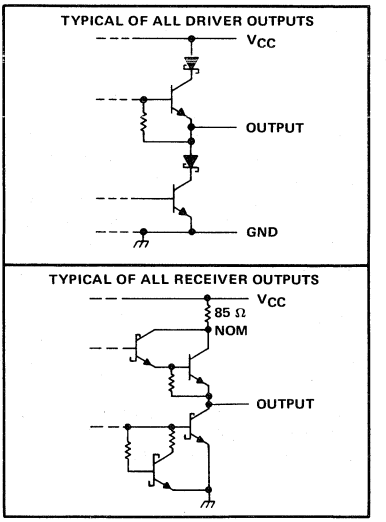


SN75178B



schematics of inputs and outputs





12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75177B and SN75178B chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	EN or $\overline{EN}$	2			V
Low-level input voltage, V_{IL}	EN or $\overline{EN}$			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½V_{OD1}			V
				2			
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.4 V,				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V,				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\ \|V_t\| - \|\overline{V}_t\|\ \|$	$\|\ \|V_t\| - \|\overline{V}_t\|\ \|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|\ V_{os} - \overline{V}_{os}\ \|$	$\|\ V_{os} - \overline{V}_{os}\ \|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				20	μA
						−400	
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 12.
NOTE 5: Refer to EIA Standard RS-422 A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		30	40	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		25	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

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PARAMETER MEASUREMENT INFORMATION

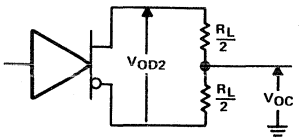


FIGURE 1. DRIVER V_{OD} AND V_{OC}

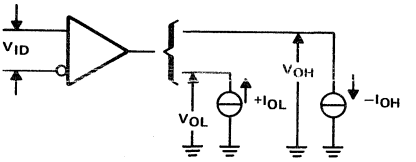
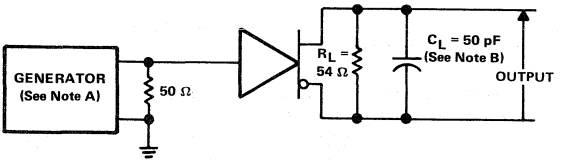
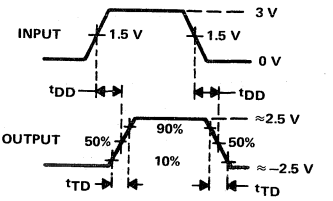


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

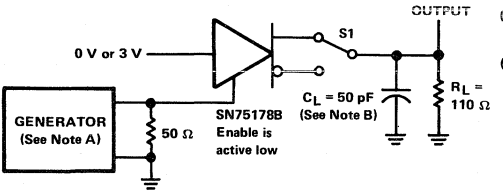


TEST CIRCUIT

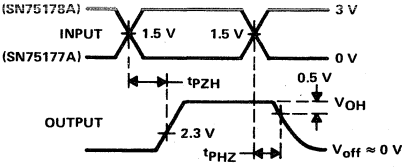


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES (t_{PZH}, t_{PHZ})

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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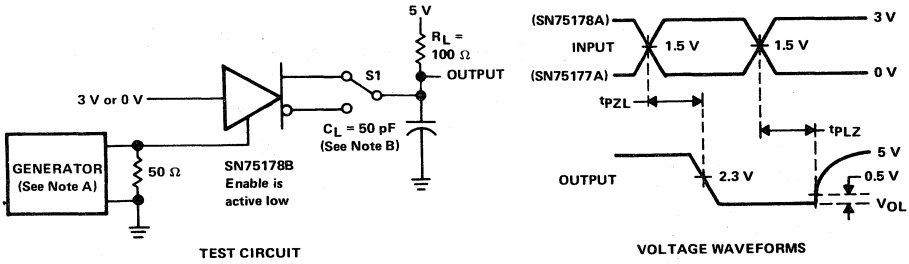
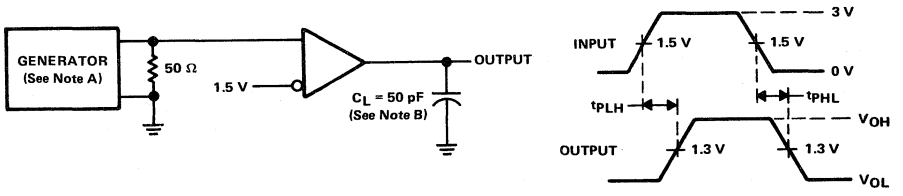
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES (t_{PZL}, t_{PLZ})



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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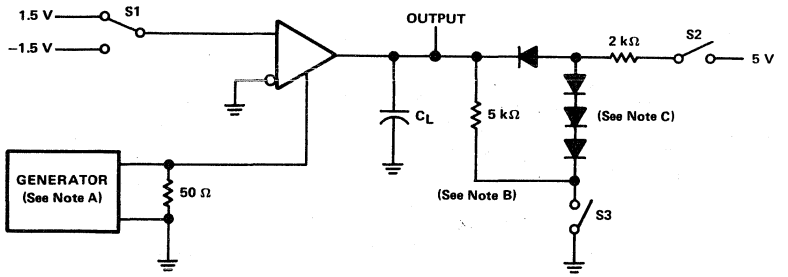
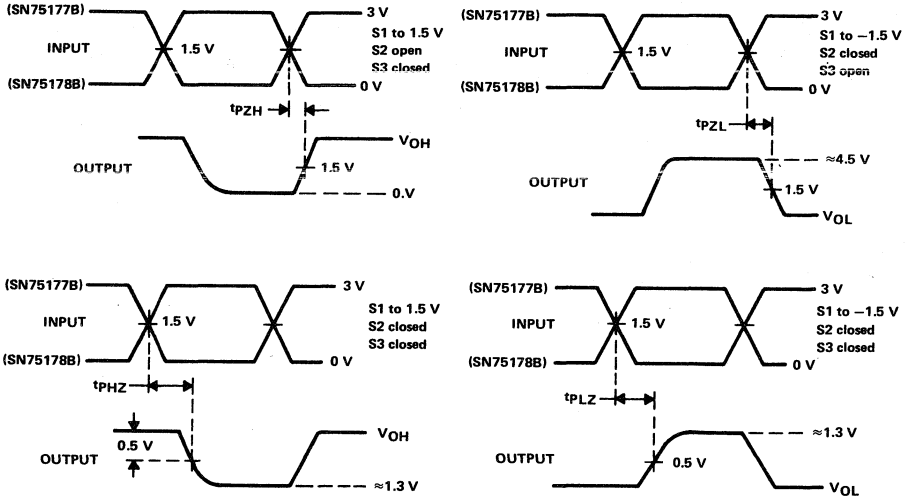
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 7. RECEIVER ENABLE AND DISABLE TIMES

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TYPICAL CHARACTERISTICS

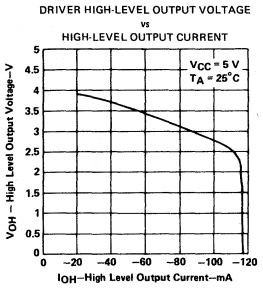

FIGURE 8

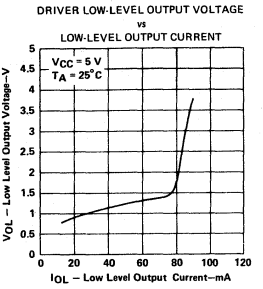

FIGURE 9

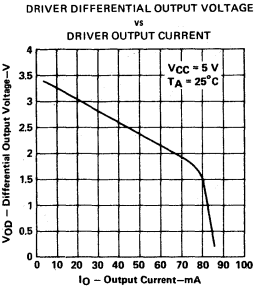

FIGURE 10

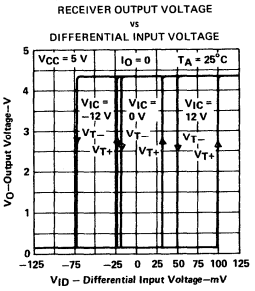

FIGURE 11

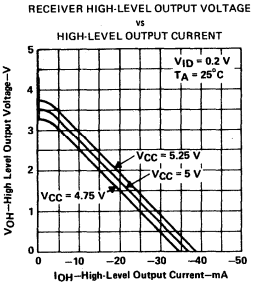

FIGURE 12

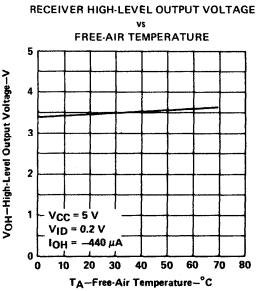

FIGURE 13

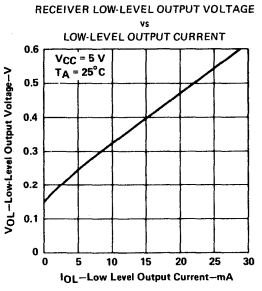

FIGURE 14

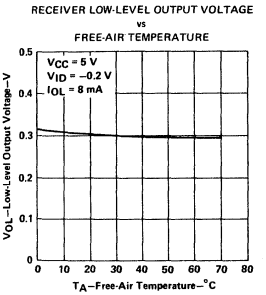

FIGURE 15

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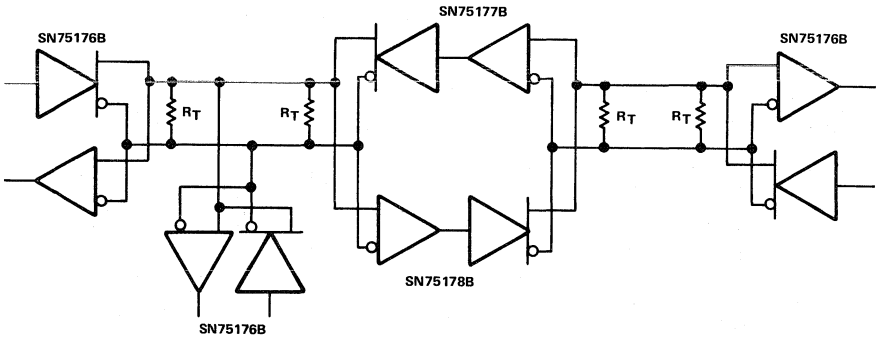
TYPICAL APPLICATION



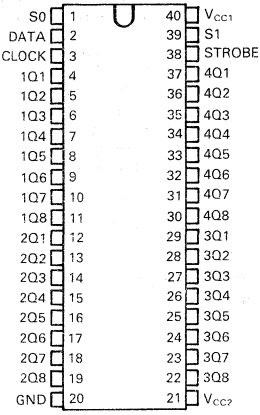
NOTE 6: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 16. TYPICAL APPLICATION CIRCUIT

TYPES SN55500 , SN75500
AC PLASMA DISPLAY DRIVERS

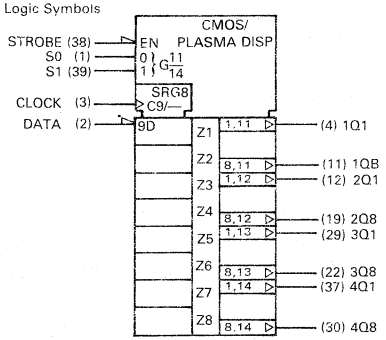
- Controls 32 Electrodes
- 100V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Dependable Texas Instruments Quality and Reliability
- Direct Replacement for SN75500

SN55500 . . . J PACKAGE
SN75500 . . . J OR N PACKAGE
(TOP VIEW)

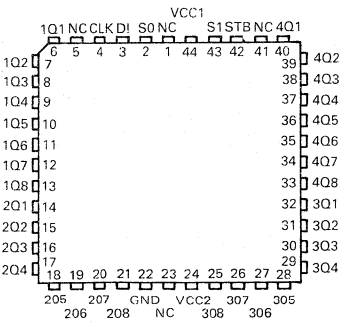


SN55500 , SN75500

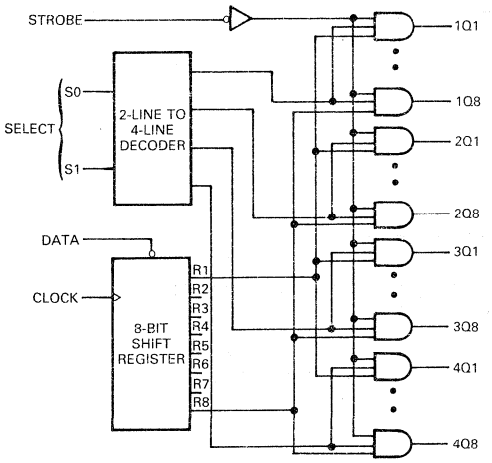
Logic Symbols



SN55500 . . . FC PACKAGE
SN75500 . . . FC OR FN PACKAGE



functional block diagram (positive logic)



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description

The SN55500 and SN75500 are monolithic BIDFET* integrated circuits designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the ouputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output selections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55500 is characterized for operation over the full military temperature range of −55°C to 125°C.
The SN75500 is characterized for operation over the commercial operating temperature range of 0°C to 70°C.

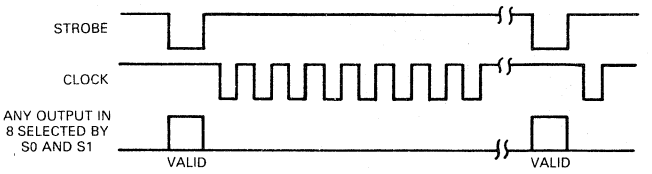
*BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS						
	DATA	CLOCK	SELECT S1	SELECT S0	STROBE	SHIFT REGISTER R1	R2	R3 . . . R8	1Q1 . . . 1Q8	2Q1 . . . 2Q8	3Q1 . . . 3Q8	4Q1 . . . 4Q8
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	L . . . L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	R1 . . . R8	L . . . L	L . . . L	L . . . L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	R1 . . . R8	L . . . L	L . . . L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	R1 . . . R8	L . . . L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	R1 . . . R8

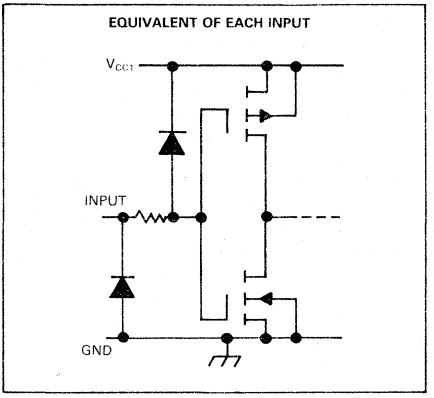
H = high level, L = low level, X = irrelevant, ↑ = low-to-high level transition.
R1 . . . R32 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R32_n$ = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

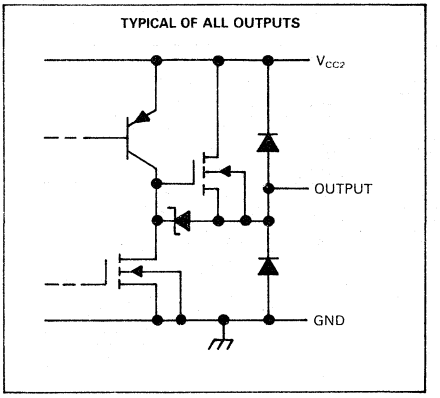
typical operating sequence



12

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (See Note 1) 13.8V
Supply voltage, V_{CC2} 100V
Input voltage ..... V_{CC1} +0.3V
Continuous total dissipation at (or below) 25°C J Package (See Note 2) 1650mW
N Package (See Note 2) 1285mW
FN Package (See Note 2) 1785mW
FC Package (See Note 2) ..... TBD
Operating free-air temperature range: SN75500 ..... 0°C to 70°C
SN55500 ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6mm (1/16 inch) from case for 60 seconds: J Package ..... 300°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: N Package ..... 260°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see dissipation derating table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE TA
J (alloy mount)	1650mW	22 mW/°C	75°C
N	1285mW	10.3mW/°C	25°C
FC (alloy mount)		TBD	75°C
FN	1785mW	14.3mW/°C	25°C

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	SN75500	10.8	12	13.2	V
		SN55500	10.8	12	12.8	
V_{CC2}	Supply voltage		0		100	V
VIH	High-level input voltage (See Fig, 1, 4)		(.75)V_{CC1}			V
VIL	Low-level input voltage (See Fig. 1, 4)				(.25)V_{CC1}	V
IOH	Peak high-level Q output current				−20	mA
IOL	Peak low-level Q output current				20	mA
IOKH	High-level Q output clamp current				20	mA
IOKL	Low-level Q output clamp current				−20	mA
f_{clock}	Clock frequency (See Note 3)		0		8	MHz
tw	Pulse duration, clock high or low (See Fig. 1)		62			ns
tsu	Data setup time before clock high (See Fig. 1)		20			ns
tsu	Select setup time before strobe low (See Fig. 1)		50			ns
th	Data hold time after clock high (See Fig. 1)		50			ns
th	Strobe high hold time after clock high (See Fig. 1)		50			ns
th	Select hold time after strobe high (See Fig. 1)		50			ns
T_A	Operating free-air temperature	SN55500	−55		125	C
		SN75500	0		70	C

NOTE: 3. For operation above 25°C junction temperature see Figure 3.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55500 MIN	SN55500 TYP	SN55500 MAX	SN75500 MIN	SN75500 TYP	SN75500 MAX	UNIT
V_{IK}	Input clamp voltage	V_{cc1}=12V, Ii=−12mA			−1	−1.5		−1	−1.5	V
V_{OH}	High level Q output voltage	SN75500 : V_{cc1}=13.2V SN55500 : V_{cc1}=12.8V V_{cc2}=100V	IOH=−1mA	94	97.5		95	97.5		V
			IOH=−10mA	92	94.5		93	94.5		
			IOH=−15mA	90	93.5		91	93.5		
V_{OL}	Low level Q output voltage		IOL=1mA		0.85	2		0.85	2	V
			IOL=10mA		2	4		2	4	
			IOL=15mA		2.75	5		2.75	5	
V_{OK}	Q Output clamp voltage	V_{cc2}=100V	IO=20mA		101	102.5		101	102.5	V
			IO=−20mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High level input current	SN75500 : V_{cc1}=13.2V SN55500 : V_{cc1}=12.8V	VIH=VIH min			1			1	μA
I_{IL}	Low-level input current		VIL=VIL max			−1			−1	μA
I_{cc1}	Low voltage supply current		VI=V_{cc1}		0.05	1		0.05	1	mA
			VI=GND		0.05	1		0.05	1	mA
I_{cc2}	High voltage supply current	V_{cc2}=100V Eight outputs high			1	5		1	3	mA
		V_{cc2}=100V All outputs low			1	3		1	2	mA

Typical values are at V_{cc1}=12V, T_A=25°C.

switching characteristics, V_{CC1}=12V, V_{CC2}=100V, T_A=25°C

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time high to low level Q output from strobe input	C_L=30pF		250	ns
t_{DLH}	Delay time low to high level Q output from strobe input			450	ns
t_{THL}	Transition time high-to-low level Q output	See Figs. 1 & 2		200	ns
t_{TLH}	Transition time low-to-high level Q output			300	ns

parameter measurement information

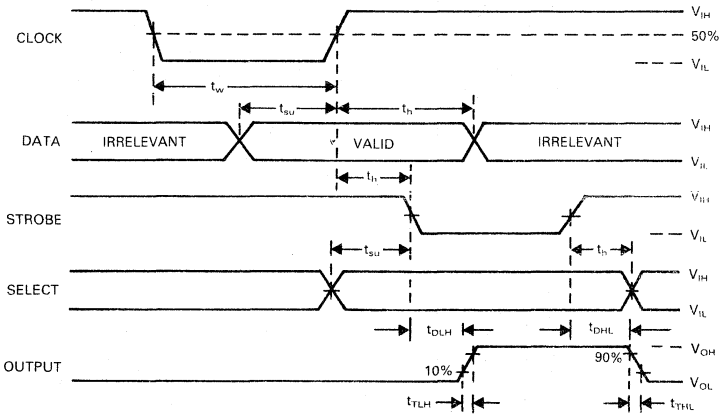
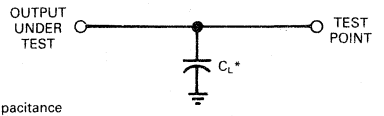


FIGURE 1. VOLTAGE WAVEFORMS



*Includes probe and jig capacitance

FIGURE 2. LOAD CIRCUIT

TEXAS INSTRUMENTS

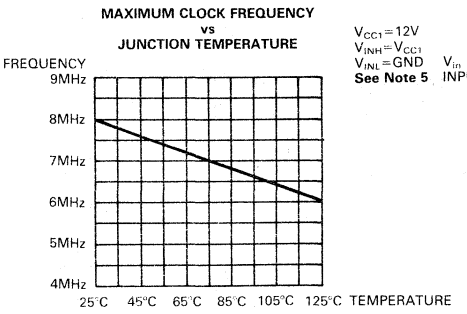


FIGURE 3

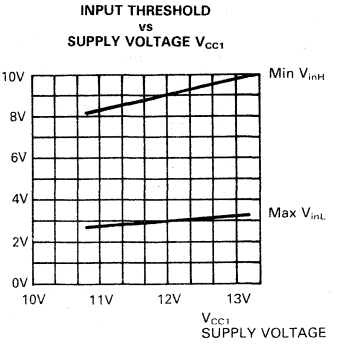


FIGURE 4

NOTE 5: This curve assumes a symmetrical clock pulse.

thermal information

junction temperature formula

$T_J = T_A + P_D R_\theta$

where
T_J = virtual junction temperature
T_A = free air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$ or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
N 40-pin plastic	97°C/W	27°/W
J 40-pin ceramic	45°C/W	12°C/W
FN 44-pin-plastic	70°C/W	
FC 44-pin ceramic	TBD	TBD

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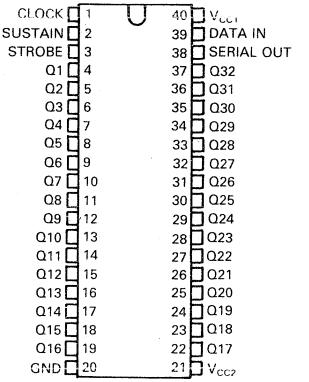
TYPES SN55501 , SN75501
AC PLASMA DISPLAY DRIVERS

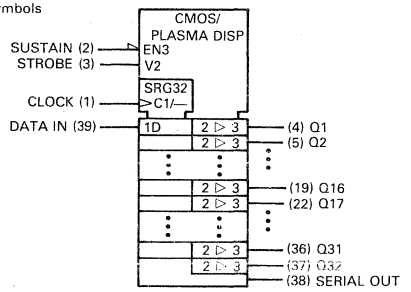
- Controls 32 Electrodes
- 100V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Dependable Texas Instruments Quality and Reliability
- Direct Replacement for SN75501

SN55501 . . . J PACKAGE
SN75501 . . . J OR N PACKAGE
(TOP VIEW)

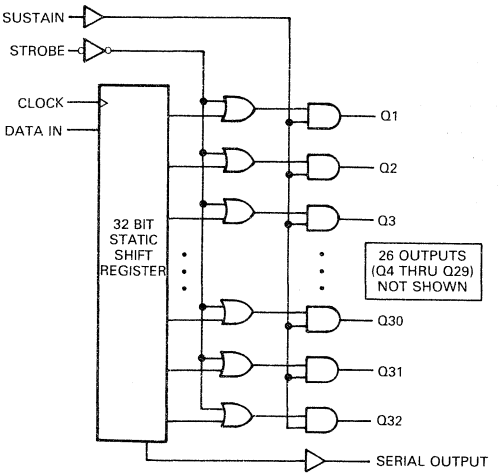


SN55501D, SN75501D

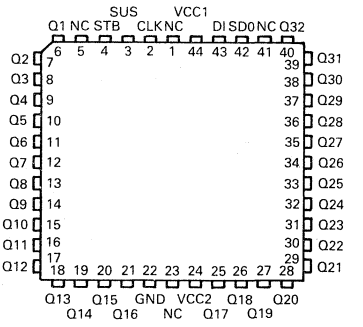
Logic Symbols



functional block diagram (positive logic)



SN55501 . . . FC PACKAGE
SN75501 . . . FC OR FN PACKAGE



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TEXAS INSTRUMENTS

description

The SN55501 and SN75501 are monolithic BIDFET* integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register (in the internal 32-bit serial register) contains a low level will switch low selectively when the Strobe input is switched low if the Sustain input is high. All other outputs remain high. When the Sustain input is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the sustain pulse required in the operation of an AC plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low standby pwer consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501 is characterized for operation over the full military temperature range of −55°C to 125°C.
The SN75501 is characterized for operation over the commercial operating temperature range of 0°C to 70°C.

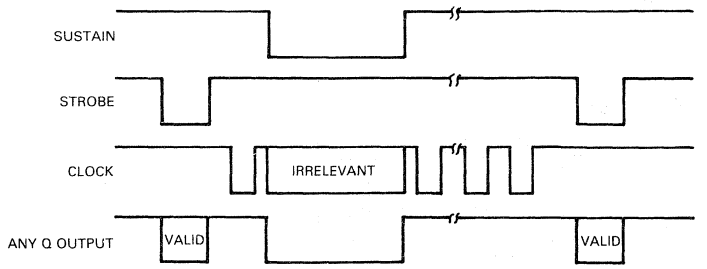
*BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

FUNCTION TABLE

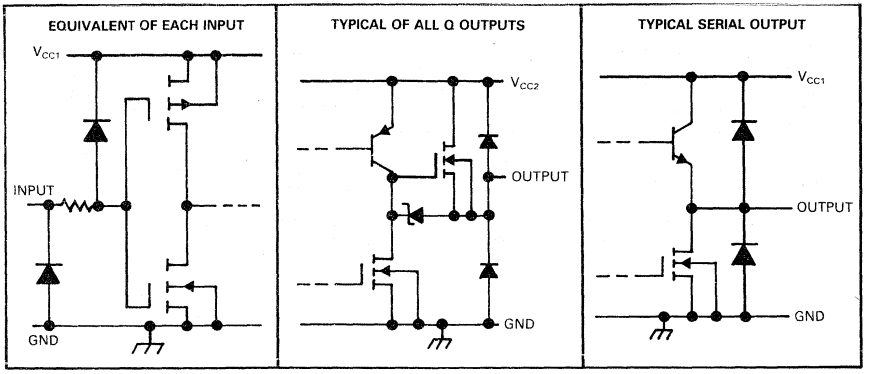
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	R1	R2	R3 . . . R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L . . . L

H=high level, L=low level, X=irrelevant, ↑ =low-to-high level transition.
R1 . . . R32=levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ . . . $R32_n$=levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the Clock input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (See Note 1)		13.8V
Supply voltage, V_{CC2}		100V
Input voltage		V_{CC1} +0.3V
Continuous total dissipation at (or below) 25°C	J Package (See Note 2)	1650mW
	N Package (See Note 2)	1285mW
	FN Package (See Note 2)	1785mW
	FC Package (See Note 2)	TBD
Operating free-air temperature range:	SN75501	0°C to 70°C
	SN55501	−55°C to 125°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6mm (1/16 inch) from case for 60 seconds: J Package		300°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: N Package		260°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see dissipation derating table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE TA
J (alloy mount)	1650mW	22 mW/°C	75°C
N	1285mW	10.3mW/°C	25°C
FC (alloy mount)		TBD	75°C
FN	1785mW	14.3mW/°C	25°C

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	SN75501	10.8	12	13.2	V
		SN55501	10.8	12	12.8	
V_{CC2}	Supply voltage		0		100	V
VIH	High-level input voltage (See Fig. 1, 4)		(.75)V_{CC1}			V
VIL	Low-level input voltage (See Fig. 1, 4)				(.25)V_{CC1}	V
IOH	Peak high-level Q output current				−20	mA
IOL	Peak low-level Q output current				20	mA
IOKH	High-level Q output clamp current				20	mA
IOKL	Low-level Q output clamp current				−20	mA
f_{clock}	Clock frequency (See Notes 3 and 4)		0		8	MHz
tw	Pulse duration, clock high or low (See Fig. 1)		62			ns
tsu	Data setup time before clock high (See Fig. 1)		20			ns
th	Data hold time after clock high (See Fig. 1)		50			ns
th	Strobe high hold time after clock high (See Fig. 1)		150			ns
th	Strobe high hold time after sustain high (See Fig. 1)		250			ns
T_A	Operating free-air temperature	SN55501	−55		125	C
		SN75501	0		70	C

NOTE: 3. See Figure 3 for maximimum clock frequency when devices are operated in cascade.
4. For operation above 25°C junction temperature see Figure 3.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

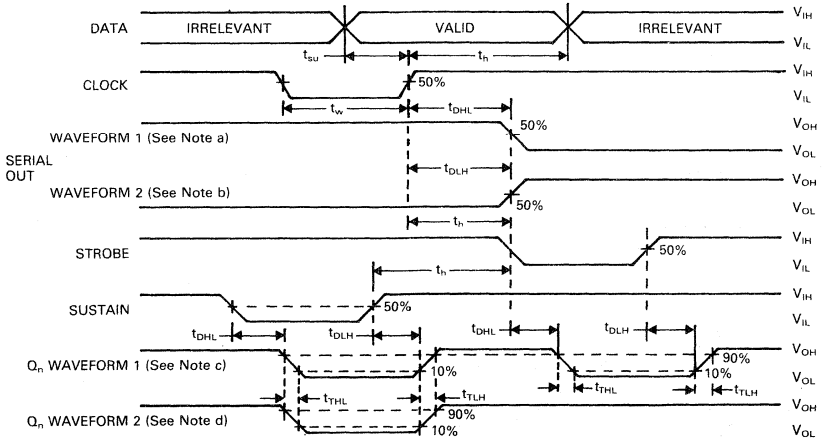
PARAMETER			TEST CONDITIONS		SN55501			SN75501			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	Input clamp voltage		V_{cc1}=12V, II=−12mA			−1	−1.5		−1	−1.5	V
V_{OH}	High level output voltage	Q Outputs	SN75501 : V_{cc1}=13.2V	IOH=−1mA	94	97.5		95	97.5		V
			SN55501 : V_{cc1}=12.8V	IOH=−10mA	92	94.5		93	94.5		
			V_{cc2}=100V	IOH=−15mA	90	93.5		91	93.5		
		Serial data	V_{cc1}=10.8V	IOH=−100μA	9	10		9	10		
V_{OL}	Low level output voltage	Q Outputs	SN75501 : V_{cc1}=13.2V	IOL=1mA		0.85	2		0.85	2	V
			SN55501 : V_{cc1}=12.8V	IOL=10mA		2	4		2	4	
			V_{cc2}=100V	IOL=15mA		2.75	5		2.75	5	
		Serial data	V_{cc1}=10.8V	IOL=100μA		0.1	1		0.1	1	
V_{OK}	Q Output clamp voltage		V_{cc2}=100V	IO=20mA		101	102.5		101	102.5	V
				IO=−20mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High level input current			VIH=VIH min			1			1	μA
I_{IL}	Low-level input current		SN75501 : V_{cc1}=13.2V	VIL=VIL max			−1			−1	μA
I_{cc1}	Low voltage supply current		SN55501 : V_{cc1}=12.8V	VI=V_{cc1}		0.05	1		0.05	1	mA
			V_{cc2}=100V	VI=GND		0.05	1		0.05	1	mA
I_{cc2}	High voltage supply current		V_{cc2}=100V	outputs low		0.1	1		0.1	3	mA
			V_{cc2}=100V	outputs high		1	5		1	3	mA

Typical values are at V_{cc1}=12V, T_A=25°C.

switching characteristics, V_{CC1}=12V, V_{CC2}=100V, T_A=25°C

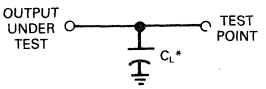
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time to high-to-low transition	From strobe to Q outputs	CL=30pF		250	ns
		From sustain to Q outputs			250	
		From clock to serial data output	CL=20pF		147	
t_{DLH}	Delay time to low-to-high transition	From strobe to Q outputs	CL=30pF		450	ns
		From sustain to Q outputs			450	
		From clock to serial data output	CL=20pF		147	
t_{THL}	Transition time high-to-low level Q output		CL=30pF		200	ns
t_{TLH}	Transition time low-to-high level Q output				300	ns

parameter measurement information



NOTES: a. Serial data out waveform for internal conditions such that a logic low is registered in R32.
b. Serial data out waveform for internal conditions such that a logic high is registered in R32.
c. Q_n output with a logic low stored in associated register R_n.
d. Q_n output with a logic high stored in associated register R_n.

FIGURE 1. VOLTAGE WAVEFORMS



*Includes probe and jig capacitance

FIGURE 2. LOAD CIRCUIT

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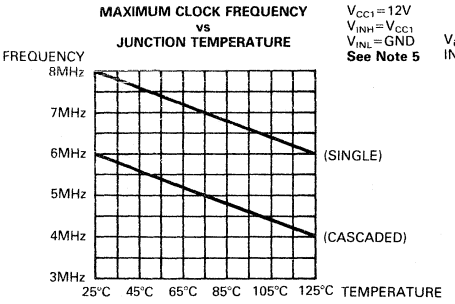

SN55/75501D FIGURE 3

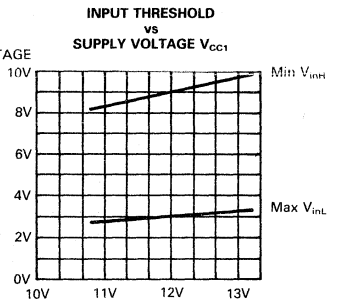

FIGURE 4

NOTE 5: This curve assumes a symmetrical clock pulse.

thermal information

junction temperature formula

$T_J = T_A + P_D R_\theta$

where
T_J=virtual junction temperature
T_A=free air temperature
P_D=average device power dissipation
R_θ=thermal resistance (junction-to-air, $R_{\theta JA}$ or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
N 40-pin plastic	97°C/W	27°/W
J 40-pin ceramic	45°C/W	12°C/W
FN 44-pin-plastic	70°C/W	
FC 44-pin ceramic	TBD	TBD

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NEW PRODUCTS DATA SHEETS

The following data sheets are for new devices introduced recently.

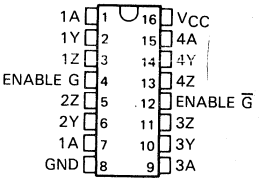
SN75ALS192
SN75ALS194
SN75164B
SN75179B
SN75407
SN75408
SN75423
SN75424
SN75435
SN75436
SN75437A
SN75438
SN75440
SN75512A
SN75513A
SN75514
SN75518
SN75551
SN75552
SN75553
SN75554
SN75555
SN75556
SN75603
SN75604
SN75605
TL4810B
TL5812
UCN4810A
ULN2803A
ULN2804A

SN75ALS192
QUADRUPLE DIFFERENTIAL LINE DRIVERS

D2904, JULY 1985

- Meets EIA Standard RS-422-A
- High-Speed, Low-Power ALS Design
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output Enable Inputs
- Improved Replacement for the AM26LS31

SN75ALS192 . . . D, J, N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

This quadruple complementary-output line driver is designed for data transmission over twisted-pair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds.

FUNCTION TABLE (EACH DRIVER)

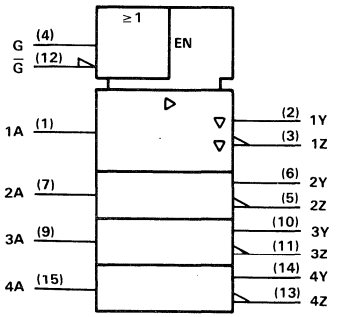
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
Z = high impedance (off),
X = irrelevant

High-impedance inputs maintain input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. Complementary control inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver.

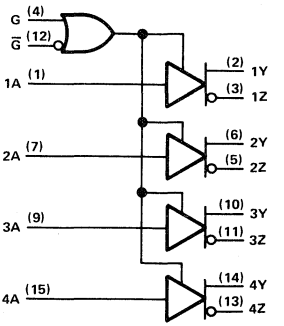
The SN75ALS192 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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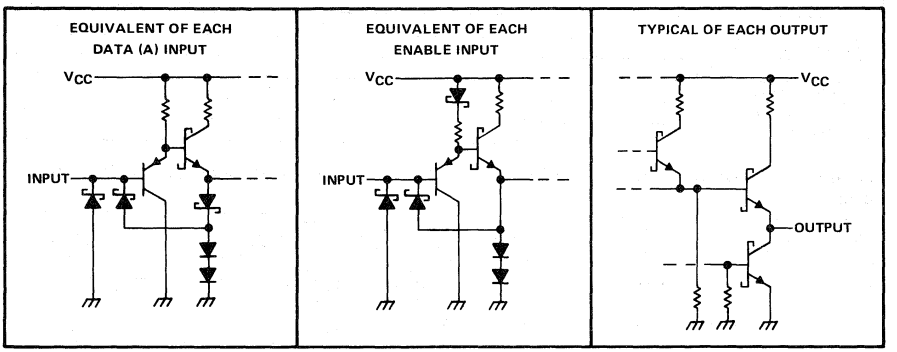
TEXAS INSTRUMENTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1000 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, SN75ALS192 chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70° POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1000 mW	8.2 mW/°C	28°C	656 mW
N	875 mW	7.0 mW/°C	25°C	560 mW

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 20 mA				0.5	V
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				0.2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		−30		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, All outputs disabled			26	45	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDTIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, S1 and S2 open		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	ns
	Output-to-output skew			3	6	ns
t_{PZH}	Output enable time to high level	R_L = 75 Ω		11	15	ns
t_{PZL}	Output enable time to low level	R_L = 180 Ω		16	20	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed		8	15	ns
t_{PLZ}	Output disable time from low level			18	20	ns

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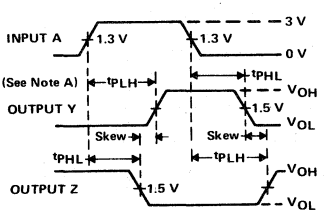
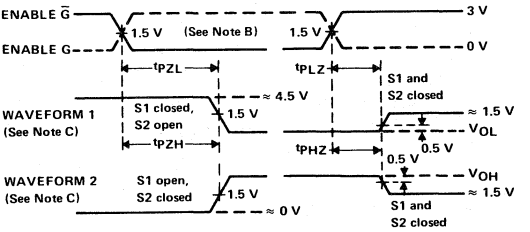
PARAMETER MEASUREMENT INFORMATION

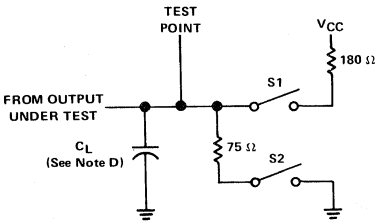


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the enable inputs. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the enable inputs.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, and $t_f \leq 6$ ns.

FIGURE 1. SWITCHING TIMES

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TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

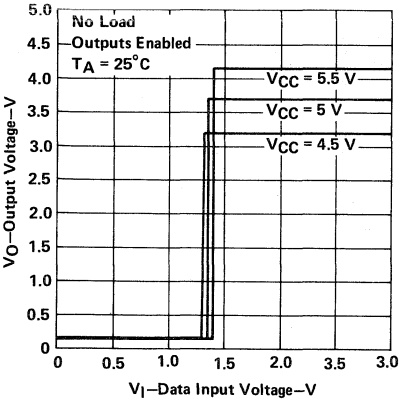

FIGURE 2

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

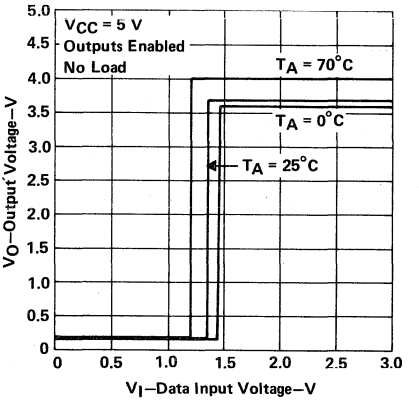

FIGURE 3

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

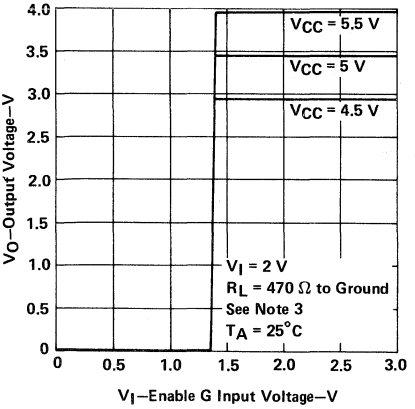

FIGURE 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

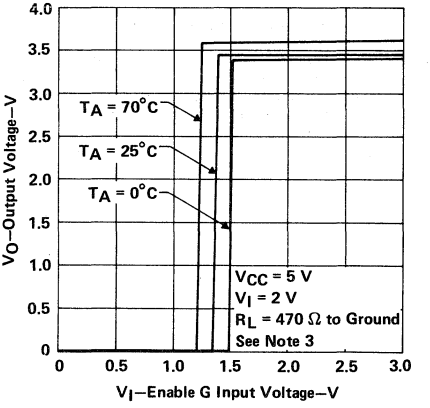

FIGURE 5

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

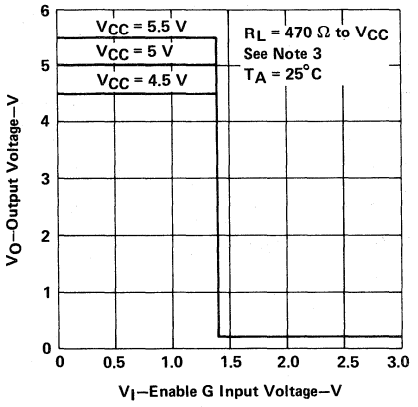

FIGURE 6

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

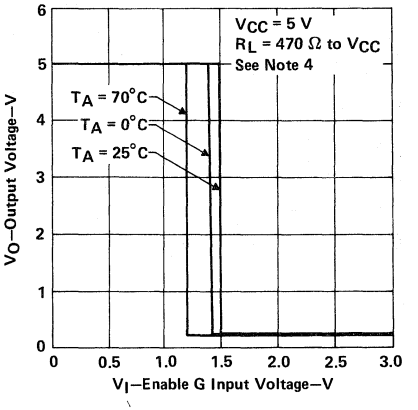

FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

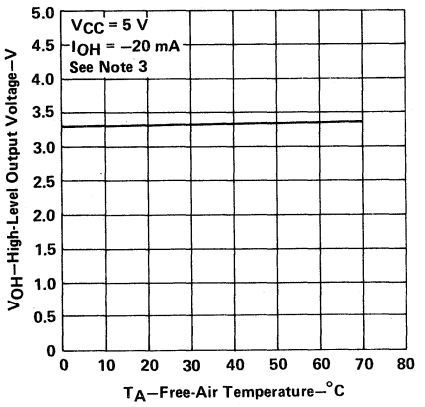

FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

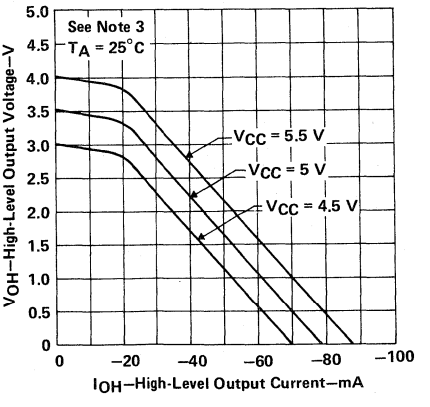

FIGURE 9

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

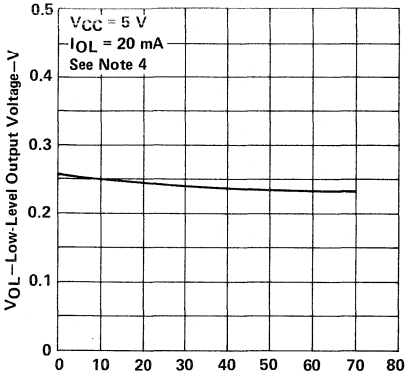

FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

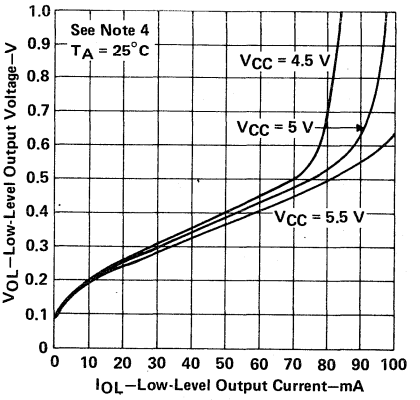

FIGURE 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

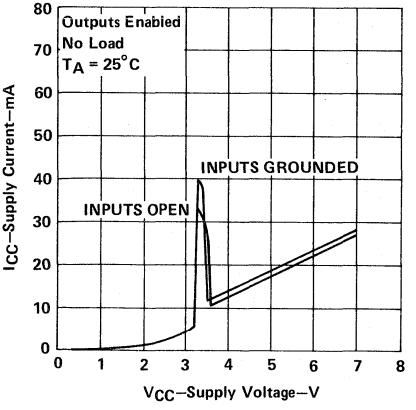

FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

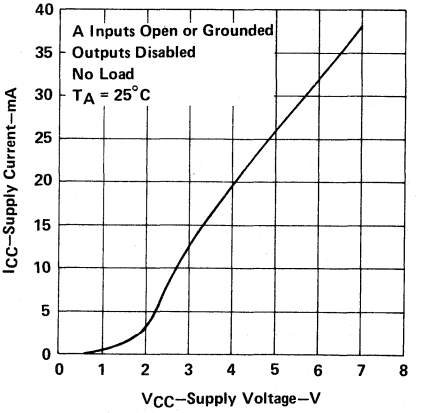

FIGURE 13

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

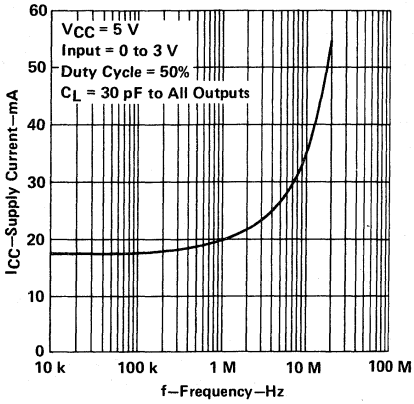
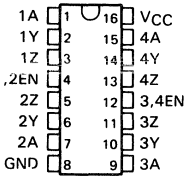


FIGURE 14

- Meets EIA Standard RS-422-A
- High-Speed ALS Design
- 3-State TTL-Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Two Pairs of Drivers Independently Enabled
- Designed as a Replacement for the MC3487 with Improvements: I_{CC} 50% Lower, Switching Speed 30% Faster

D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

H = TTL high level, L = TTL low level, X = irrelevant

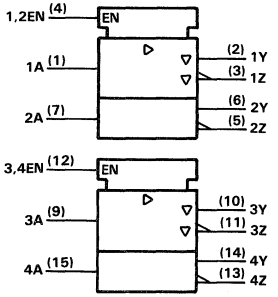
description

This quadruple complementary-output line driver is designed for data transmission over twisted-pair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds and enable/disable times are typically less than 16 nanoseconds.

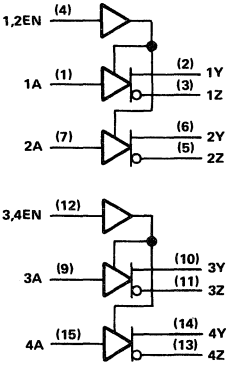
High-impedance inputs keep input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN75ALS194 is capable of data rates in excess of 10 megabits per second and is designed to operate with the SN75ALS195 quadruple line receiver.

The SN75ALS194 is characterized for operation from 0°C to 70°C.

logic symbol



logic diagram (positive logic)



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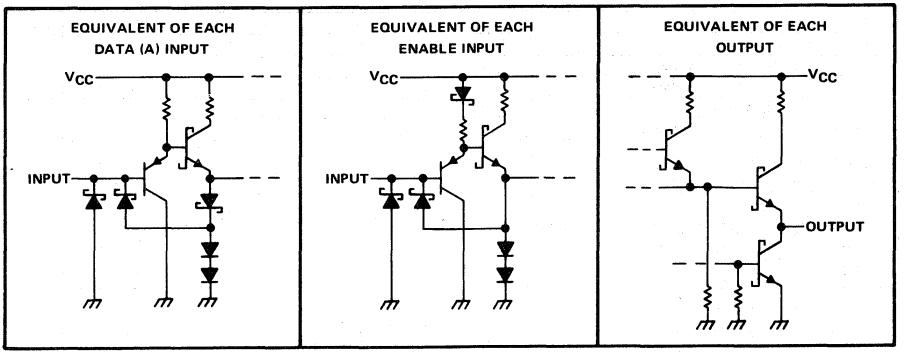
TEXAS INSTRUMENTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70°C POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1025 mW	8.2 mW/°C	25°C	656 mW
N	875 mW	7.0 mW/°C	25°C	560 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			48	mA
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA				0.5	V
VO	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		2		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			V
				2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance state output current	Output enables at 0.8 V	V_O = 2.7 V			100	μA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current§	V_I = 2 V		−40		−140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, All outputs disabled			26	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDTIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1			6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output				9	14	ns
	Output-to-output skew				3.5	6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 2			8	14	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 3			9	12	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level				9	14	ns
t_{PLZ}	Output disable time from low level				12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

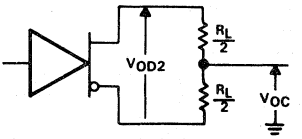


FIGURE 1. DRIVER V_{OD} AND V_{OC}

12

PARAMETER MEASUREMENT INFORMATION

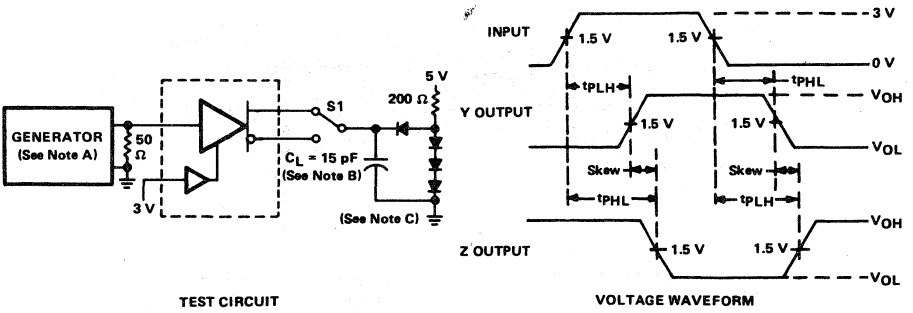


FIGURE 2. PROPAGATION DELAY TIMES

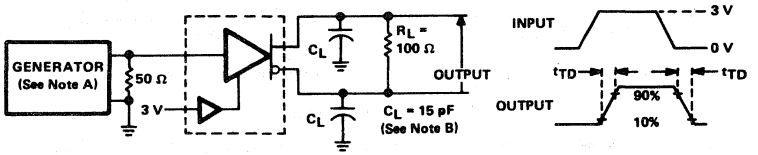
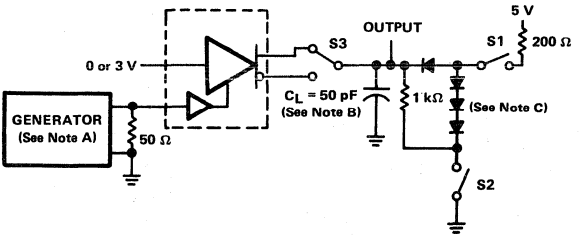


FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

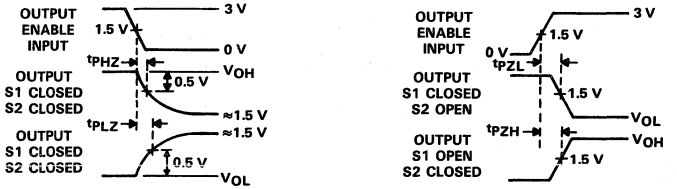
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR $\leq$ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

12

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

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TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

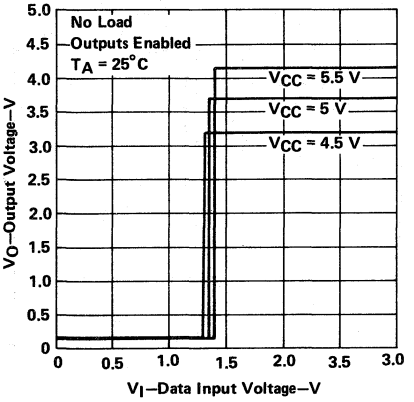

FIGURE 5

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

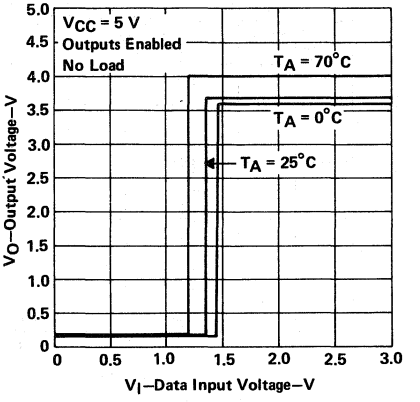

FIGURE 6

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

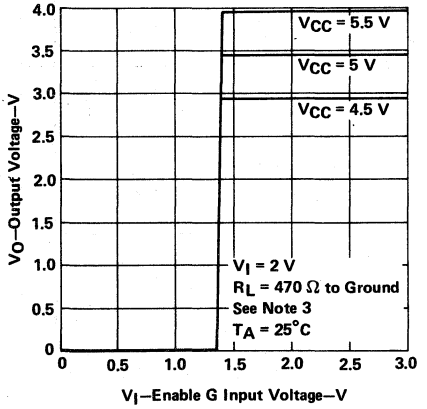

FIGURE 7

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

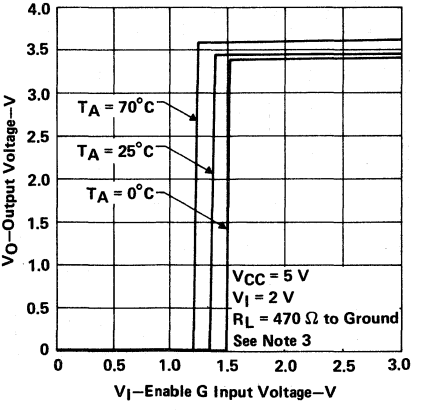

FIGURE 8

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

12

TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

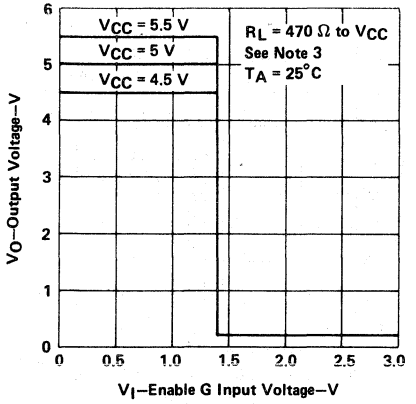

FIGURE 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

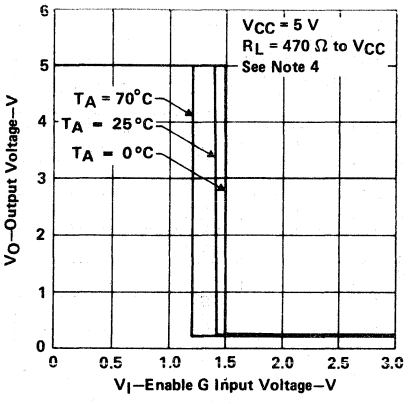

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

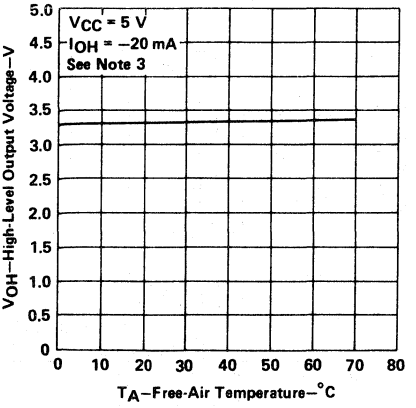

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

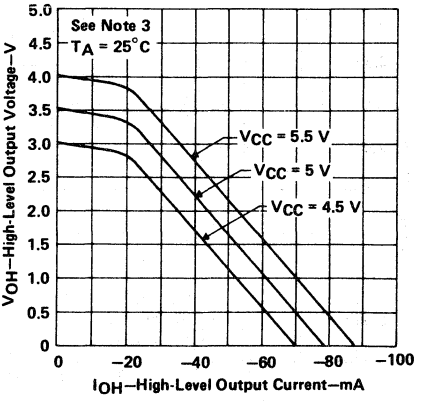

FIGURE 12

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

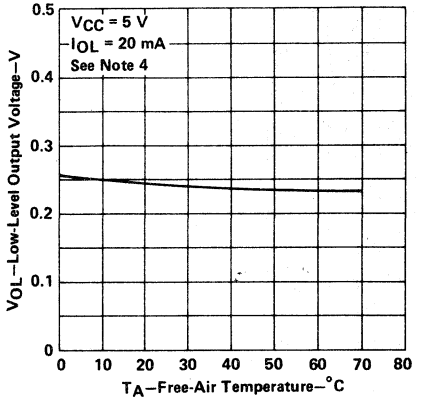


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

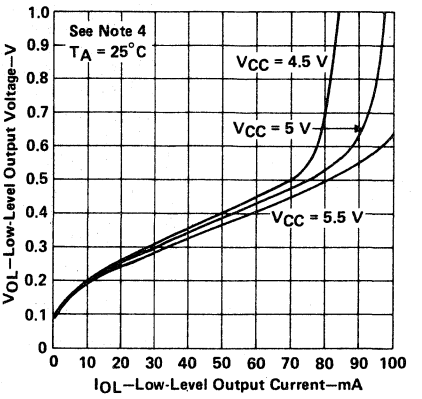


FIGURE 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

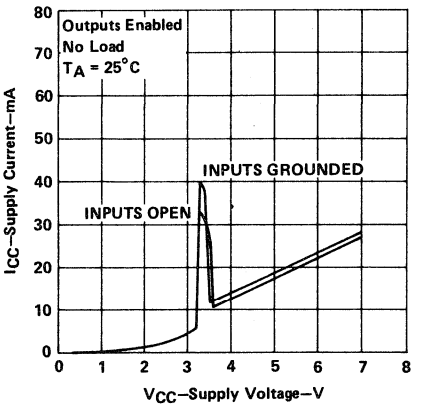


FIGURE 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

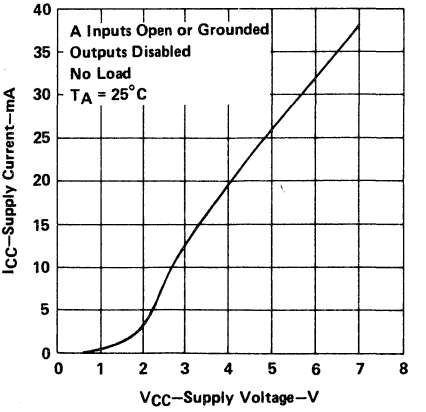


FIGURE 16

NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

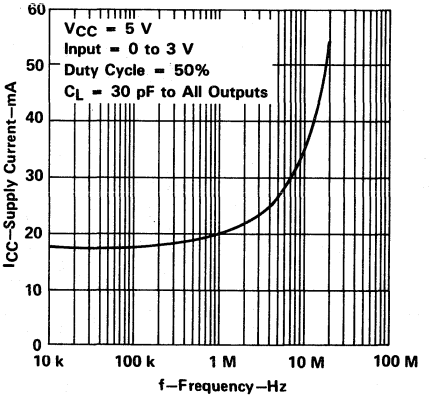


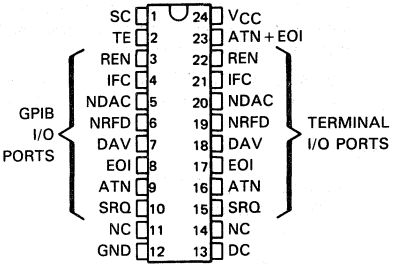
FIGURE 17

TEXAS INSTRUMENTS

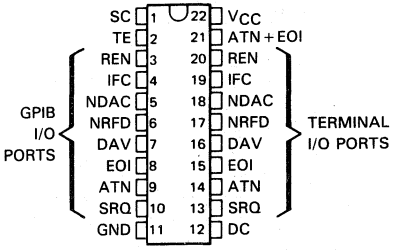
D2908, OCTOBER 1985

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- ATN + EOI (OR Function) Output to Simplify Board Layout
- Designed to Implement Control Bus Interface for Multi-Controllers
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

DW SMALL OUTLINE PACKAGE
(TOP VIEW)



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN75164B eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75164B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75164B features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75164B is identical to the SN75162B with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
ATN + EOI	ATN logical OR EOI	Logic
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

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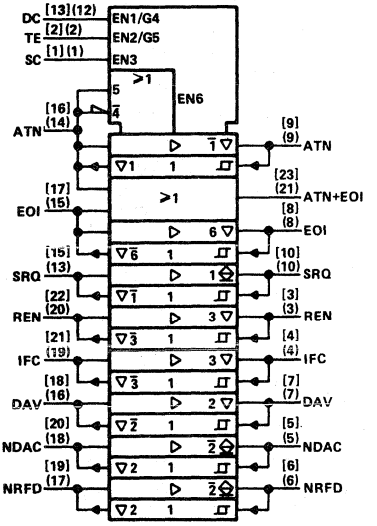
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

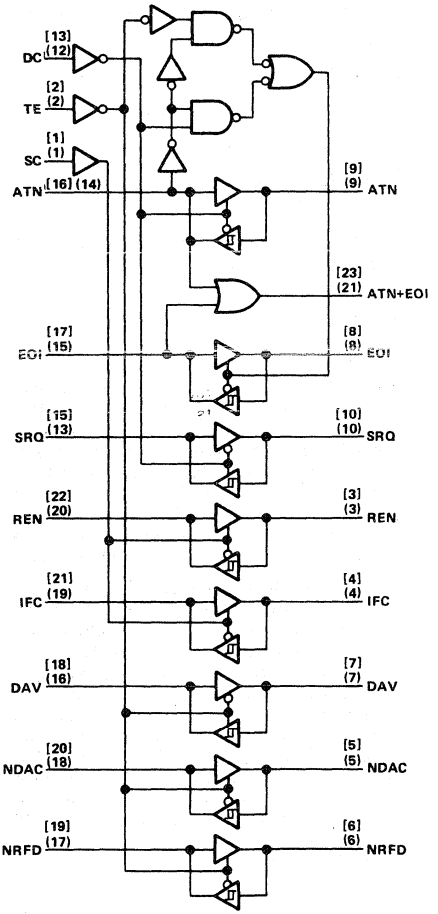
The SN75164B is manufactured in a 22-pin dual-in-line and 24-pin Small Outline package. The SN75164B is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

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RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

INPUTS		OUTPUT
ATN	EOI	ATN + EOI
H	X	H
X	H	H
L	L	L

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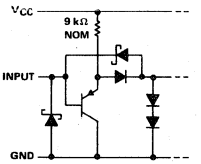
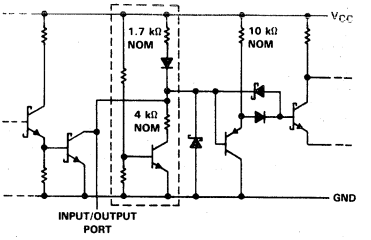
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

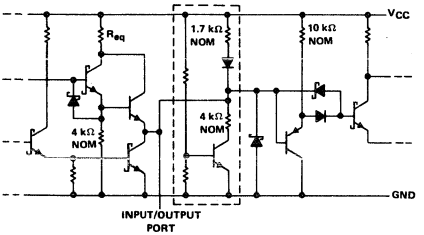


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



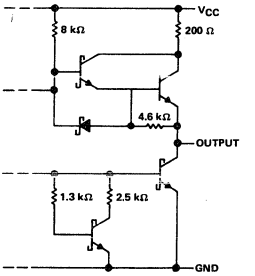
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 10.8 mW/°C, the N package at the rate of 13.6 mW/°C.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
	ATN + EOI			−400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN + EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA				−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4			V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7			V
		Bus	I_{OH} = −5.2 mA		2.5			
		ATN + EOI	I_{OH} = −400 μA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA				0.5	V
		Bus	I_{OL} = 48 mA				0.5	
		ATN + EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V				100	μA
		ATN, EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal, control	V_I = 2.7 V				20	μA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal, control	V_I = 0.5 V				−100	μA
		ATN, EOI	V_I = 0.5 V				−500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5		3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15		−75	mA
		Bus			−25		−125	
		ATN + EOI			−10		−100	
I_{CC}	Supply current		No load, TE, DC, and SC low				120	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.
§ Except ATN and EOI terminal pins.

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switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PHL}	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	See Figure 4			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	See Figure 5			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

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PARAMETER MEASUREMENT INFORMATION

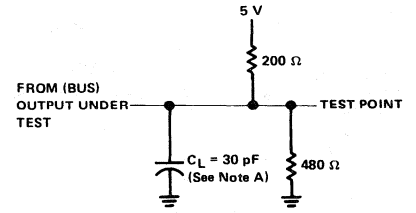


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

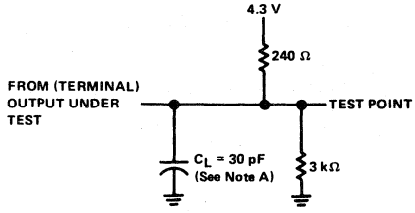
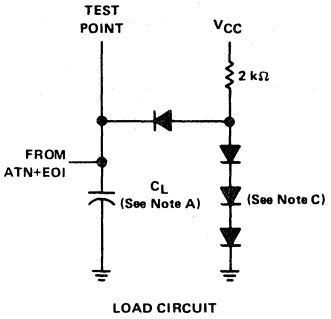


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



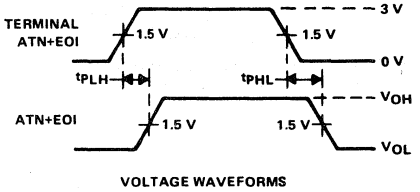


FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
C. All diodes are 1N916 or 1N3064.

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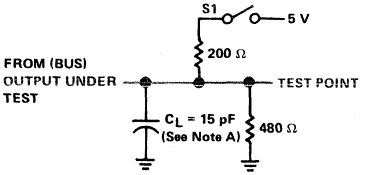
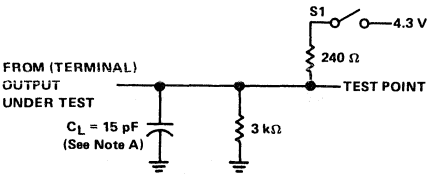
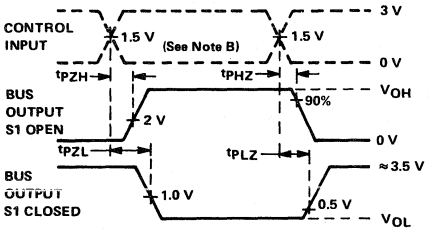
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

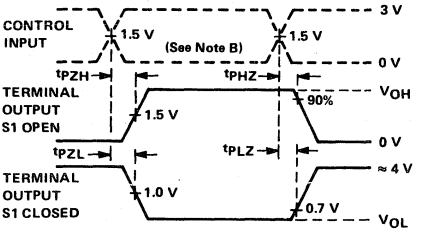


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

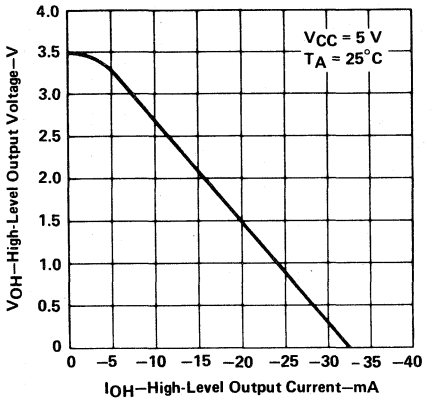

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

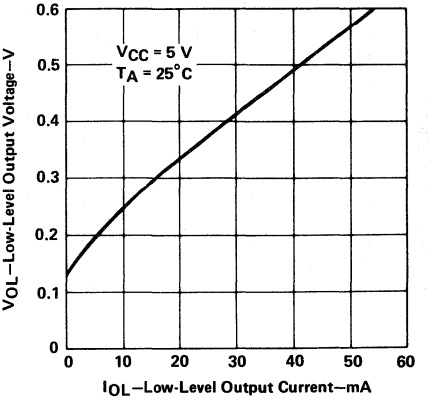

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

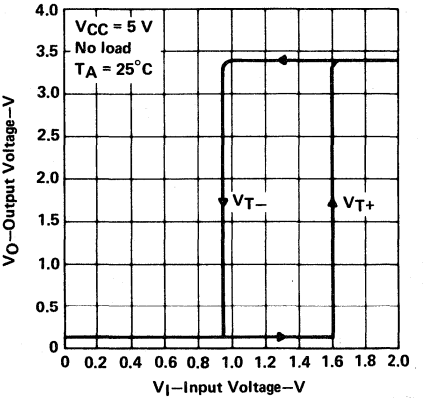

FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

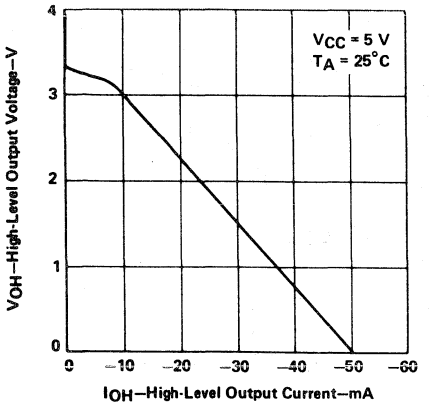

FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

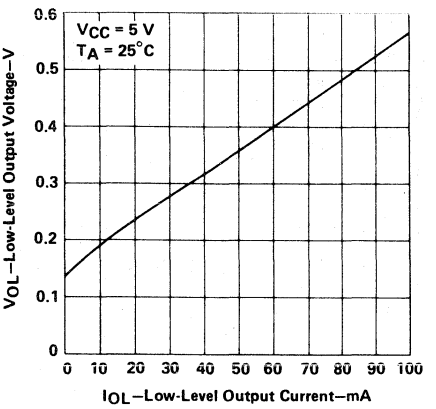

FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

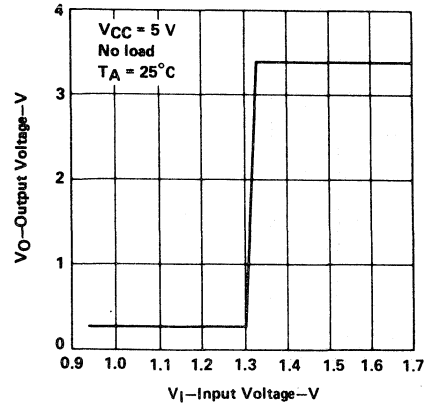

FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

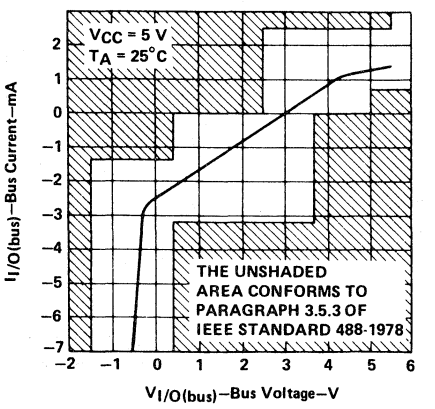

FIGURE 12

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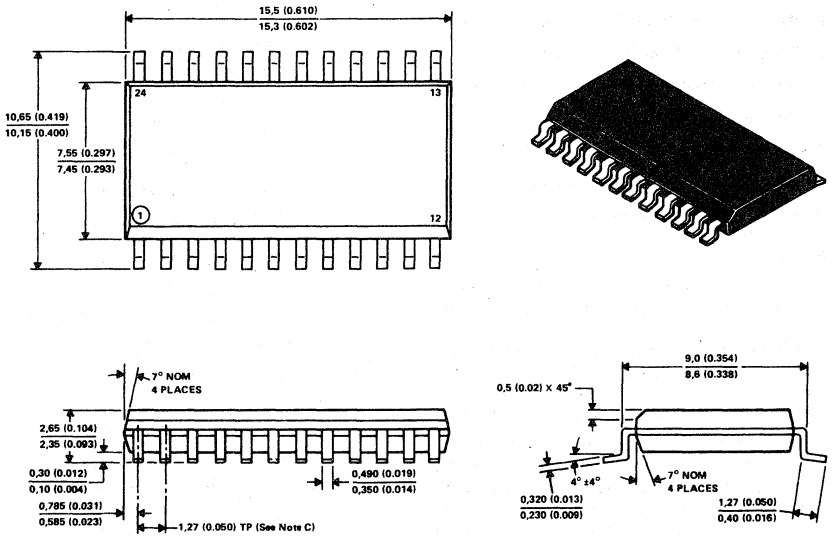
MECHANICAL DATA

DW plastic dual-in-line package

24-PIN DW PLASTIC



NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are with 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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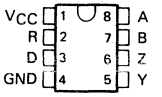
SN75179B
DIFFERENTIAL DRIVER AND RECEIVER PAIR

D2845, JULY 1985

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	OUTPUTS
D	Y Z
H	H L
L	L H

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	OUTPUT
A − B	R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

H = high level, L = low level, ? = indeterminate

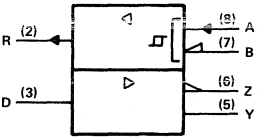
description

The SN75179B driver and bus receiver circuit is a monolithic integrated device designed for balanced transmission line applications and meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver outputs provide limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The device is designed to drive current loads of up to 60 milliamperes maximum.

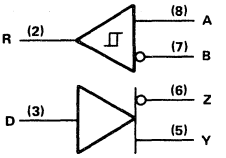
The SN75179B is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



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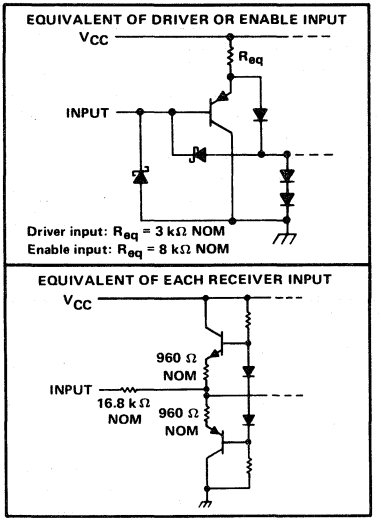
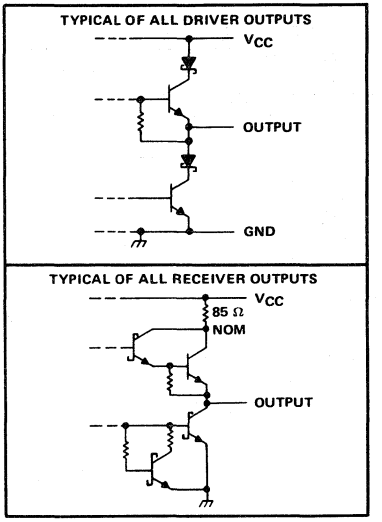
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D Package . . . . . 725 mW
JG Package . . . . . 825 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package SN75179B, chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	$\frac{½V_{OD1}}{2}$			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
$\lvert V_{OD3}\rvert$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡					±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC} or 12 V				250	
I_{CC}	Supply current (total package)	No load			57	75	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485, Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load			57	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 9.
NOTE 5: Refer to EIA Standard RS-422-A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,		19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, See Figure 4		30	40	ns

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PARAMETER MESUREMENT INFORMATION

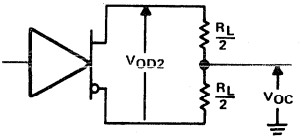

FIGURE 1. DRIVER V_{OD} AND V_{OC}

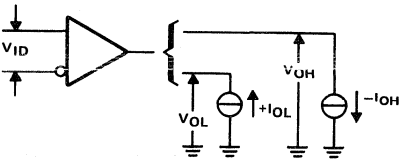

FIGURE 2. RECEIVER V_{OH} AND V_{OL}

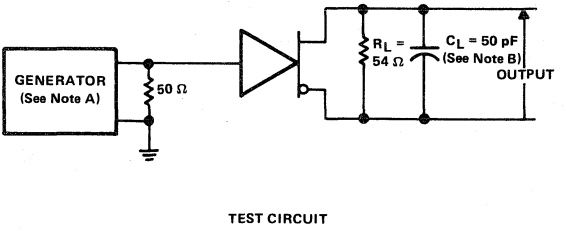

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

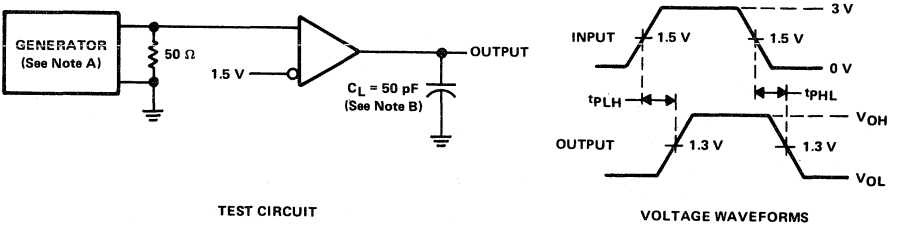

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

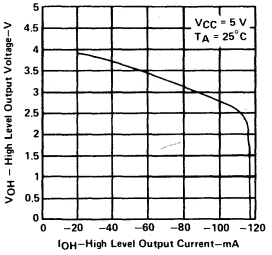

FIGURE 5

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

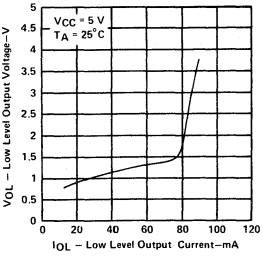

FIGURE 6

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

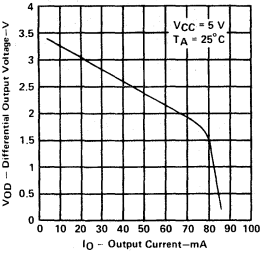

FIGURE 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

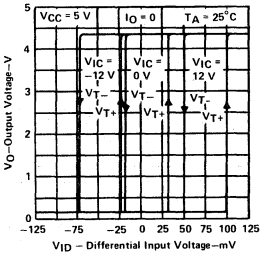

FIGURE 8

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

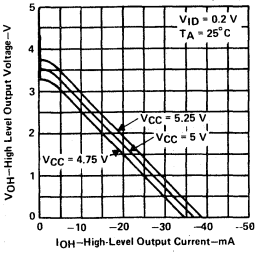

FIGURE 9

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

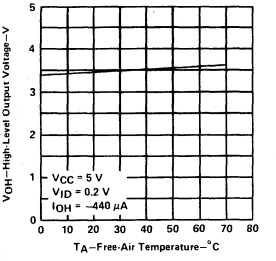

FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

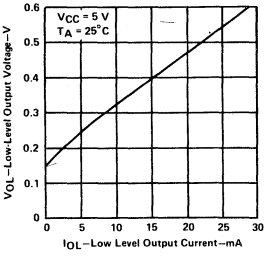

FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

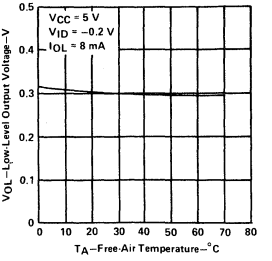

FIGURE 12

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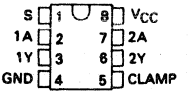
TYPES SN75407, SN75408
DUAL HIGH CURRENT PERIPHERAL DRIVERS

D..... DECEMBER 1982

- **Characterized for Use to 500 mA**
- **No Output Latch-Up at 50 V**
- **Very Low Quiescent Power . . . 100 mW Typical**
- **Very Low Input Current . . . 1 μA Typical**
- **Output Clamp Diodes**
- **TTL OR MOS Compatible-Diode Clamped Inputs**
- **Standard 5-V Supply Voltage**

SN75407
DUAL-IN-LINE PACKAGE
(TOP VIEW)



postive logic: Y = A + S

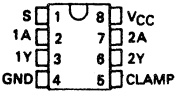
logic

SN75407 — NAND
SN75408 — OR

description

The SN75407 and SN75408 series of dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching outputs. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs. Use of PNP circuitry enables this series to feature very low quiescent power and minimal input current requirements. Applications include logic buffers, hammer drivers, DC motor drivers, and DC relay/solenoid drivers.

SN75408
DUAL-IN-LINE PACKAGE
(TOP VIEW)



postive logic: Y = A + S

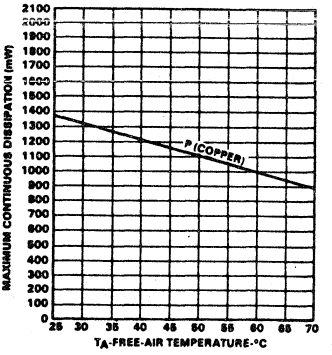
FUNCTION TABLES

SN75407 (each driver)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

SN75408 (each driver)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H



12

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Output current (see Note 2) ..... 550 mA
Output clamp diode current ..... 550 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)
P (copper) ..... 1380 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1, 6mm (1/16 inch) from case for 10 seconds ..... 260°C

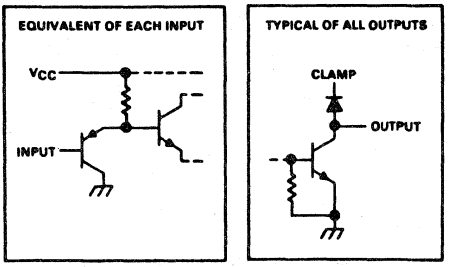
NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. PG package for operation above 25°C free-air temperature, derate linearly at 11.1 mW/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		$I_I = -12\ \mu A$		−0.9	−1.5		V
I_{OH}	High-level output current		$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.10	0.3	V
				$I_{OL} = 200$ mA		0.22	0.45	
				$I_{OL} = 300$ mA		0.45	0.65	
				$I_{OL} = 500$ mA		0.6	1.0	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.75$ V,	$I_{OH} = 100\ \mu A$	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.75$ V,	$I_R = 100\ \mu A$	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.75$ V,	$I_F = 500$ mA	0.6	1.2	2.0	V
I_{IH}	High-level input current		$V_{CC} = 5.25$ V,	$V_I = 5.25$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		−0.5	−10	μA
		Strobe S				−1	−20	
I_{CCH}	Supply current, outputs high	SN75407	$V_{CC} = 5.25$ V,	$V_I = 0$		20	30	mA
		SN75408		$V_I = 5$ V		20	30	
I_{CCL}	Supply current, outputs low	SN75407	$V_{CC} = 5.25$ V	$V_I = 5$ V		20	30	mA
		SN75408		$V_I = 0$		20	30	

†All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

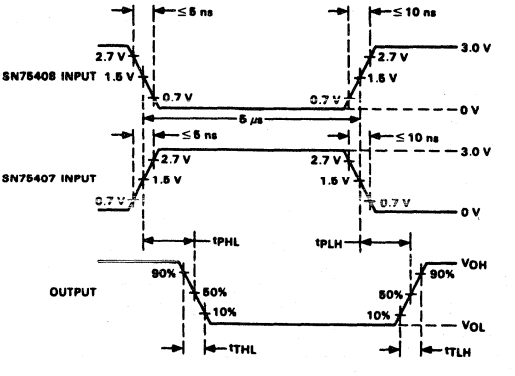
schematics of inputs and outputs



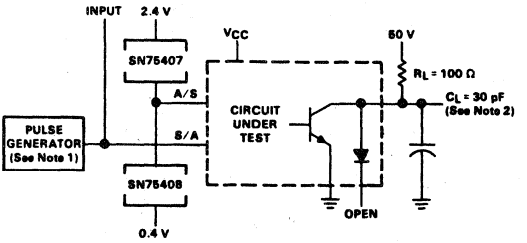
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75407			SN75408			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 1		0.5	1		0.5	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.4	0.8		0.4	0.8	μs
t_{TLH}	Transition time, low-to-high-level output			0.1	0.2		0.1	0.2	μs
t_{THL}	Transition time, high-to-low-level output			0.1	0.2		0.1	0.2	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 500 mA, See Figure 2	V_S-18			V_S-18			mV

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: 1. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50
2. C_L includes probe and jig capacitance.

FIGURE 1 — SWITCHING CHARACTERISTICS

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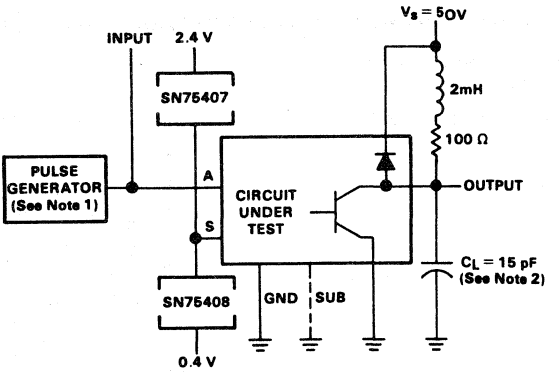
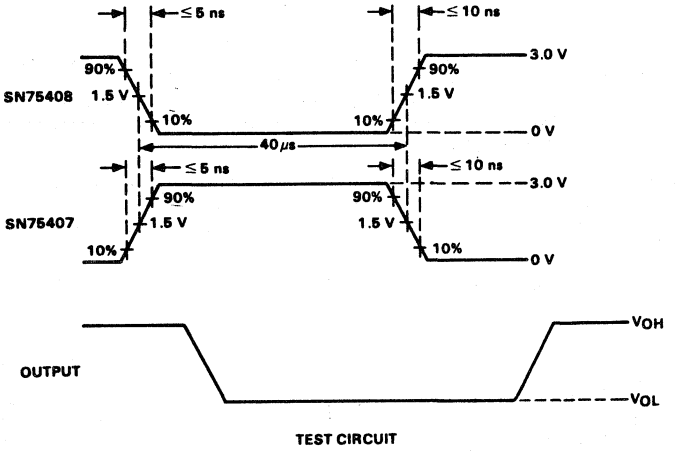


VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: 1. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50
2. C_L includes probe and jig capacitance.

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TYPES SN75423, SN75424 DARLINGTON TRANSISTOR ARRAYS

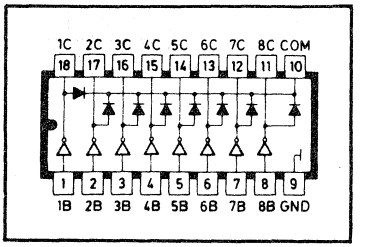
January 1982

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Compatible with ULN2800A-Series

N

DUAL-IN-LINE PACKAGE (TOP VIEW)

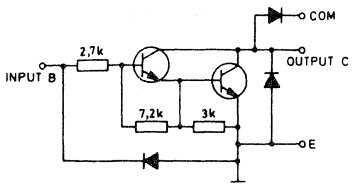


description

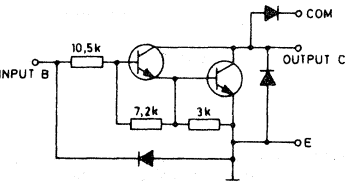
The SN75423/424 are monolithic high-voltage, high-current darlington transistor arrays. Each comprises eight n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each darlington pair is 500 milliampers. Outputs and inputs may each be paralleled for higher-current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75423 has series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The SN75424 has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the SN75423.

schematics (each darlington pair)



SN75423



SN75424

All resistor values shown are nominal and in ohms

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	100 V
Input voltage (see Note 1)	30 V
Continous collector current	500 mA
Output clamp diode current	500 mA
Total substrate-terminal current: N-package	−2.5 A
Continuous dissipation (total package) at (or below) 25°C free air temperature (see Note 2):	
N-Package	1150 mW
Operating free-air temperature range	-20 C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds, N-package	260°C

NOTES: 1. All voltages values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN75423			SN75424			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V I_I = 0			100			100	μA
		2	T_A = 70°C, V_{CE} = 100 V V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 100 V I_C = 500 μA T_A = 70°C	50	65		50	65		μA
I_I	Input current	4	V_I = 3,85 V		0,93	1,35				mA
			V_I = 5 V					0,35	0,5	
			V_I = 12 V					1,0	1,45	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V I_C = 125 mA						5	V
			V_{CE} = 2 V I_C = 200 mA			2,4			6	
			V_{CE} = 2 V I_C = 250 mA			2,7				
			V_{CE} = 2 V I_C = 275 mA						7	
			V_{CE} = 2 V I_C = 300 mA			3				
			V_{CE} = 2 V I_C = 350 mA						8	
$V_{CE(sat)}$	Collector emitter saturation voltage	5	I_I = 250 μA I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V			50			50	μA
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V, f = 1 MHz		15	30		15	30	pF

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PARAMETER MEASUREMENT INFORMATION

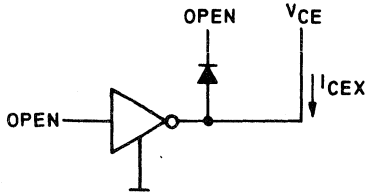

FIGURE 1 - I_{CEX}

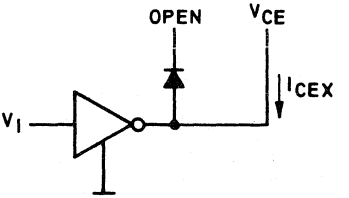

FIGURE 2 - I_{CEX}

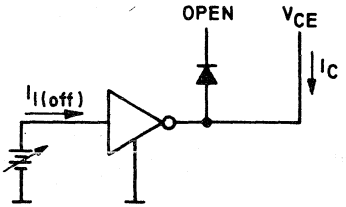

FIGURE 3 - $I_{I(off)}$

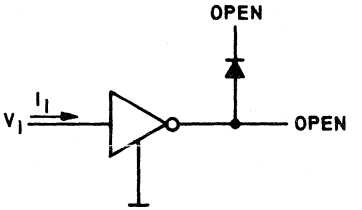

FIGURE 4 - $I_{I(on)}$

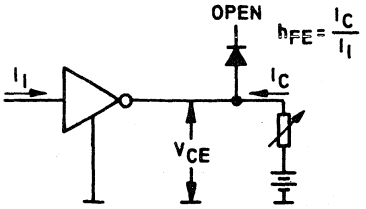

FIGURE 5 - h_{FE}, $V_{CE(sat)}$

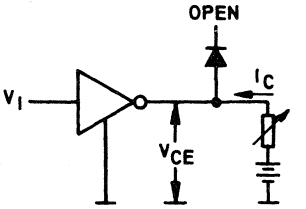

FIGURE 6 - $V_{I(on)}$

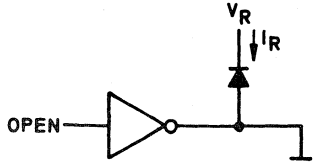

FIGURE 7 - I_R

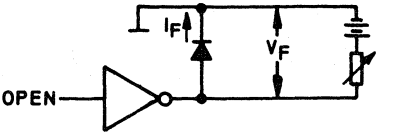

FIGURE 8 - V_F

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switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, R_L = 163 Ohm		130		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, See Figure 9		20		ns
V_{OH}	High-level output voltage after switching	V_S = 60 V, I_O = 300 mA, see Figure 10	V_S-20			mV

PARAMETER MEASUREMENT INFORMATION

switching characteristics

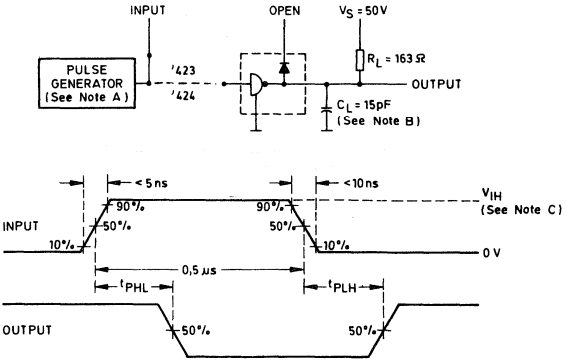

FIGURE 9-PROPOGATION DELAY TIMES VOLTAGE WAVEFORMS

NOTES: a) The pulse generator has the following characteristics: PRR = 1MHz, Z_{OUT} = 50 Ω.
b) C_L includes probe and jig capacitance.
c) For testing the 423, V_{IH} = 3 V; for the '424 V_{IH} = 8 V.

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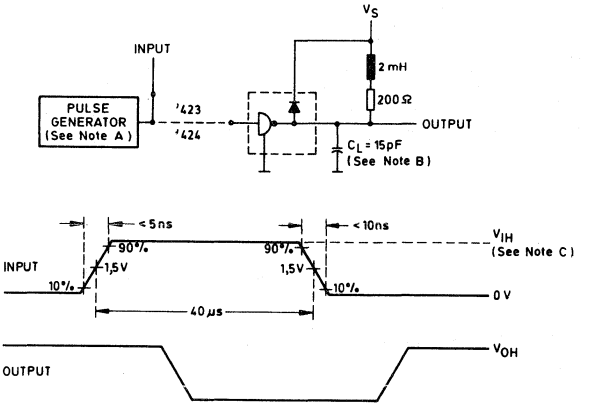

FIGURE 10-LATCH-UP TEST

VOLTAGE WAVEFORMS

NOTES: The pulse generator has the following characteristics: PRR = 12,5 kHz, Z_{OUT} = 50 Ω.
b) C_L includes probe and jig capacitance.
c) For testing the '423, V_{IH} = 3 V; for the '424 V_{IH} = 8 V.

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SN75435
QUADRUPLE PERIPHERAL DRIVER WITH OUTPUT FAULT PROTECTION

D2848, FEBRUARY 1985

- Saturating Outputs With Low On Resistance
- Very Low Standby Power . . . 53 mW Max
- High-Impedance MOS- or TTL-Compatible Inputs
- Standard 5-V Supply Voltage
- No Output Glitch During Power-Up or Power-Down
- Output Clamp Diodes for Transient Suppression
- 2-W Power Package . . . 60 °C/W $R_{\theta JA}$
- 600-mA Output Current
- 35-V Switching Voltage

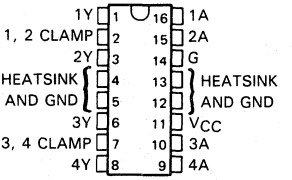
description

The SN75435 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. It features four inverting open-collector drivers with a common enable input that, when taken low, disables all four outputs. Each driver is protected against load shorts with its own latching over-current shutdown circuitry, which will turn the output off when a load short is detected. A short on one load will not affect operation of the other three drivers. The latch for the shutdown will hold the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the over-current shutdown to allow load capacitance of up to 5 nF at 35 volts.

Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

The SN75435 is characterized for operation from 0 °C to 70 °C.

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)

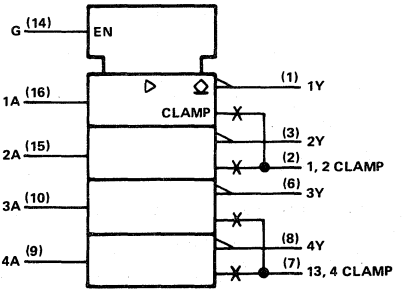


FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

H = high level, L = low level
X = irrelevant

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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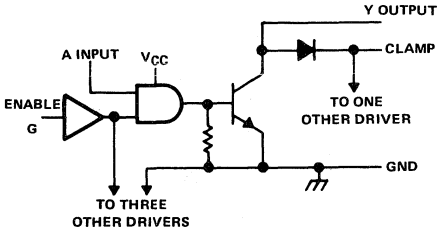
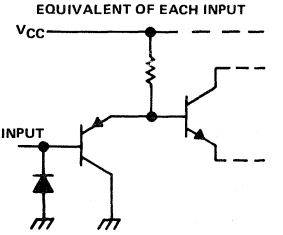
logic diagram (positive logic)



schematic of inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output supply voltage . . . . . 70 V
Output diode clamp current . . . . . 1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range . . . . . 0°C to 70°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output voltage			35	V
Output current			600	mA
Load capacitance (See Figure 3)			35	nF

electrical characteristics over recommended operating free-air temperature range

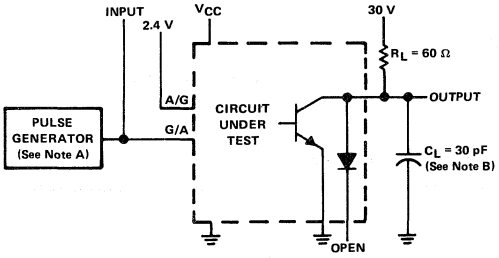
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 300 mA		0.25	0.5	V
			I_{OL} = 600 mA		0.55	1	
V_R	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
V_F	Output clamp diode forward voltage	I_F = 600 mA			1.2	1.6	V
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	μA
	Over-current shutdown current	V_{CC} = 4.75 V to 5.25 V		650	850		mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		6	10	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		55	75	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

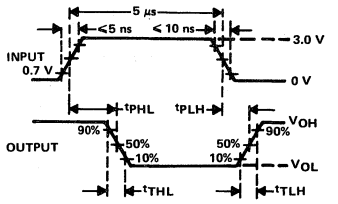
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propogation delay time, low-to-high-level output	C_L = 30 pF, R_L = 60 Ω, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		ns
t_{TLH}	Transition time, low-to-high-level output			200		ns
t_{THL}	Transition time, high-to-low-level output			200		ns
V_{OH}	High-level output voltage after switching	See Figure 2	V_S – 10			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

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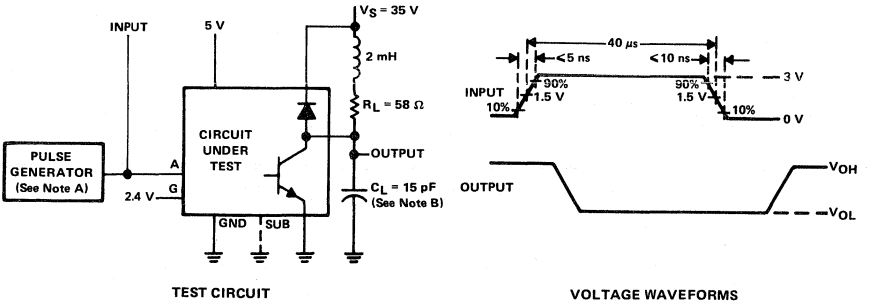
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L include probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

RECOMMENDED OPERATING CONDITIONS

MAXIMUM OUTPUT SUPPLY VOLTAGE
vs
LOAD CAPACITANCE

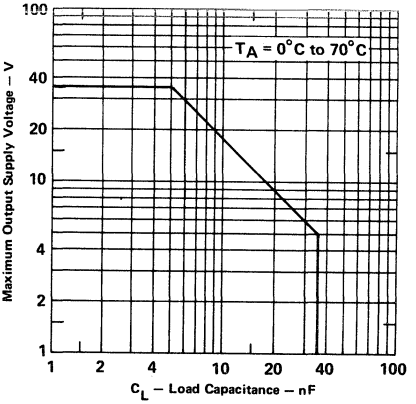


FIGURE 3

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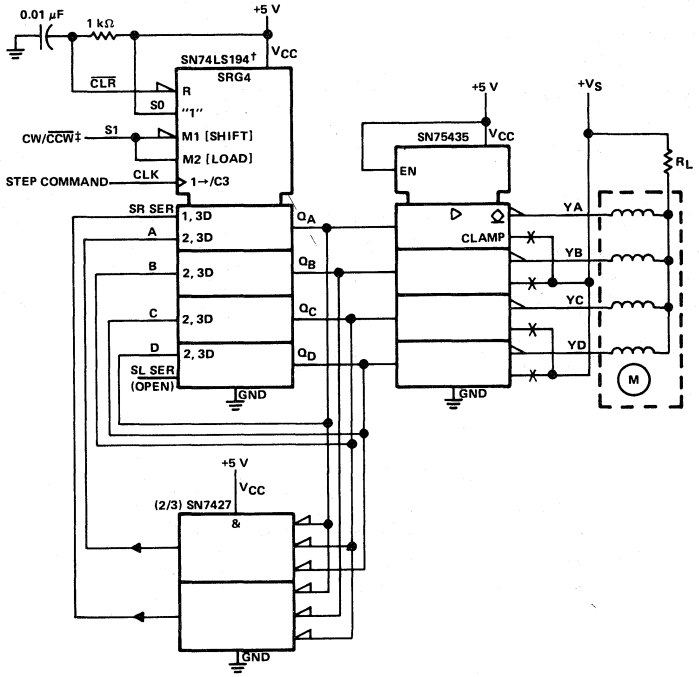
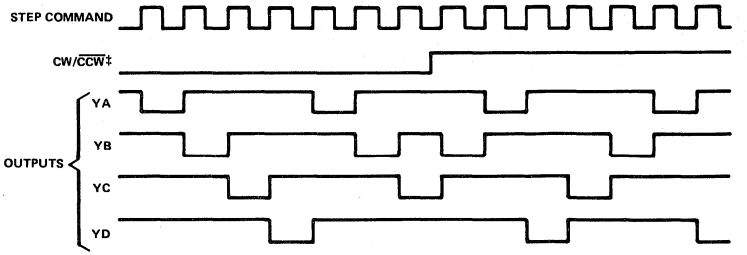
TYPICAL APPLICATION DATA



4-WINDING STEPPER MOTOR CONTROL CIRCUIT



TIMING DIAGRAM FOR MOTOR CONTROL CIRCUIT

†The SN74LS194 is a universal shift register with both shift-right and shift-left capability. In this application S0 (pin 9) is wired high and only the shift-right and parallel-load modes are utilized. The logic symbol shown above has been simplified to show only the utilized modes.

‡This signal is CW/$\overline{\text{CCW}}$ or $\overline{\text{CW}}$/CCW depending on motor winding.

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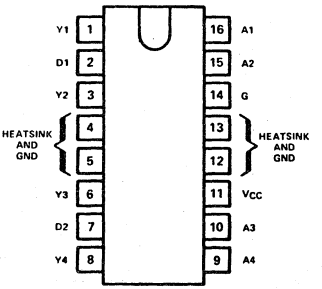
COMMON FEATURES

- SATURATING OUTPUTS WITH LOW ON RESISTANCE
- VERY LOW STANDBY POWER ... 26MW MAX
- HIGH VOLTAGE OUTPUTS ... 70V MIN
- HIGH IMPEDANCE MOS OR TTL COMPATIBLE INPUTS
- STANDARD 5V SUPPLY VOLTAGE
- NO OUTPUT GLITCH DURING POWER UP OR POWER DOWN
- OUTPUT CLAMP DIODES FOR TRANSIENT SUPPRESSION
- 2W POWER PKG. . . $60^{o}C/W$ $R_{\theta JA}$
  $10^{o}C/W$ $R_{\theta JC}$

NE DUAL-IN LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

H = high level, L = low level
X = irrelevant

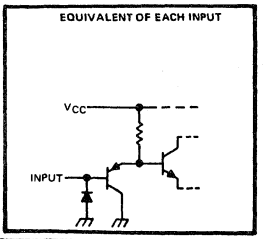
SELECTION GUIDE			
FEATURE	75436	75437 A	75438
OUTPUT CURRENT	500mA	500mA	1000mA
MAX VSAT	0.5V	0.5V	1.0V
MAX SWITCHING VOLT.	50V	35V	35V

DESCRIPTION

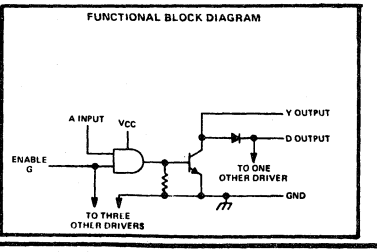
The SN75436, SN75437A, and SN75438 quad peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each features four inverting open collector drivers with a common enable input which, when taken low, disables all four outputs. Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

SCHEMATICS

EQUIVALENT OF EACH INPUT



FUNCTIONAL BLOCK DIAGRAM



12

ABSOLUTE MAXIMUM RATINGS OVER FREE-AIR TEMPERATURE RANGE

Supply voltage, Vcc 7V
Input voltage 5.5V
Output voltage 70V
Output current 1.0A
Output clamp diode current 1.0A
Continuous total dissipation, $T_A \leq 25^oC$ (free air) 2075mW
Operating free air temperature . . . . . 0^oC to 70^oC

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, Vcc	4.75	5.0	5.25	V
Output current SN75436, SN75437			500	mA
SN75438			1.0	A
Output voltage SN75436			50	V
SN75437, SN75438			35	V

SEPTEMBER 23, 1981

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP+	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC}=4.75V,	I_I=12mA		-0.9	-1.5	V
I_{OH}	High-level output current	V_{CC}=4.75V, V_{IL}=0.8V,	V_{IH}=2V V_{OH}=70V			100	uA
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_{IH}=2V	I_{OL}=500mA		0.25	0.5	V
			I_{OL}=1.0A (SN75438)		0.6	1.0	
$V_{(BR)O}$	Output breakdown voltage	V_{CC}=4.75V,	I_{OH}=100uA	70	100		V
$V_{R(D)}$	Output clamp diode reverse voltage	V_{CC}=4.75V,	I_R=100uA	70	100		V
$V_{F(D)}$	Output clamp diode forward voltage	I_F=500mA			1.2	1.6	V
		I_F=1.0A (SN75438)			1.6	2.0	
I_{IH}	High-level input current	V_{CC}=5.25V,	V_I=5.25V		0.01	10	uA
I_{IL}	Low-level input current	V_{CC}=5.25V,	V_I=0.8V		-0.5	-10	uA
I_{CCH}	Supply current, outputs high	V_{CC}=5.25V,	V_I=0		1	5	mA
I_{CCL}	Supply current, outputs low	V_{CC}=5.25V,	V_I=5V		45	65	mA

+All typical values are at V_{CC} = 5V, T_A = 25^oC

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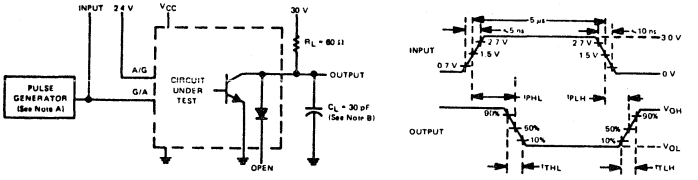
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 30pF, R_L = 60 Ω, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low level output			750		ns
t_{TLH}	Transition time, low-to-high level output			200		ns
t_{THL}	Transition time, high-to-low level output			200		ns
V_{OH}	High-level output voltage after switching	V_S = 50V, Io = 500mA (SN75436)	V_S-10			mV
		V_S = 35V, Io = 500mA (SN75437A)				
		V_S = 35V, Io = 1A (SN75438)				

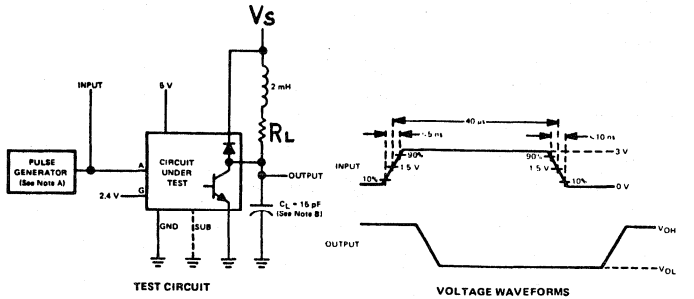
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST

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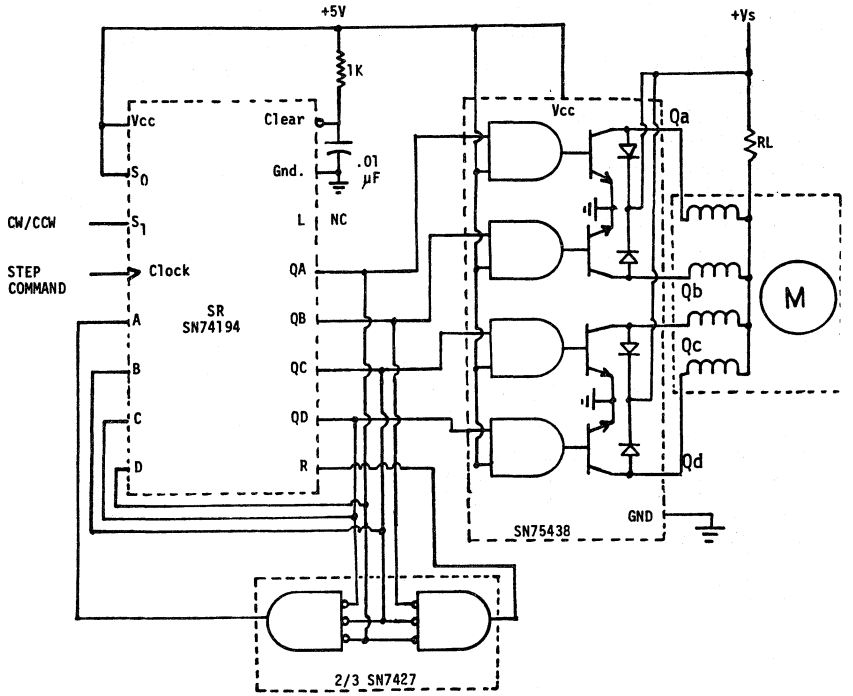
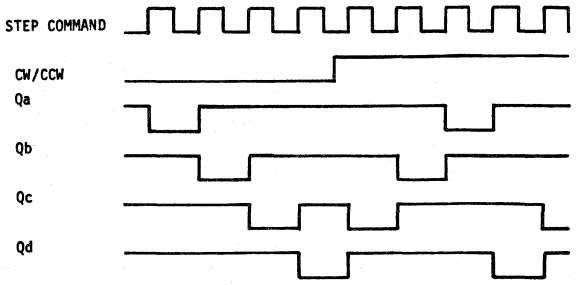
4-WINDING UNIPOLAR STEPPER MOTOR APPLICATION





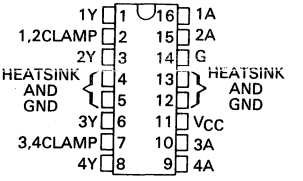
12

SN75440
QUADRUPLE PERIPHERAL DRIVER

D2872, JANUARY 1985

- Saturating Outputs With Low On-State Resistance
- High-Impedance Inputs Compatible with CMOS, MOS, and TTL Levels
- Very Low Standby Power ... 21 mW Maximum
- High-Voltage Outputs ... 70 V Min
- No Output Glitch During Power Up or Power Down
- No Latch-Up Within Recommended Operating Conditions
- Output Clamp Diodes for Transient Suppression
- 2-Watt Power Packages
- Direct Replacement for National Semiconductor DS3669

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE

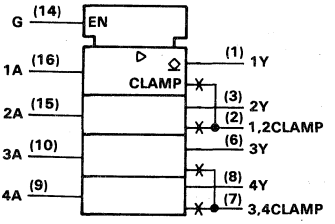
INPUTS		OUTPUT
A	G	Y
L	H	L
H	X	H
X	L	H

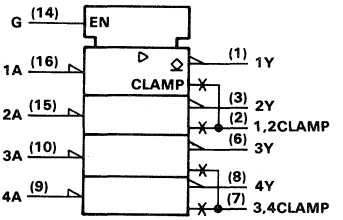
H = high level,
L = low level,
X = irrelevant

description

The SN75440 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. Each devices features four noninverting open-collector outputs with a common enable input that, when taken low, disables all four outputs. The envelope of I-V characteristics exceeds the specifications sufficiently to avoid high-current latch up. Applications include driving relays, lamps, solenoids, motors, LED's, transmission lines, hammers, and other high-power-demand devices.

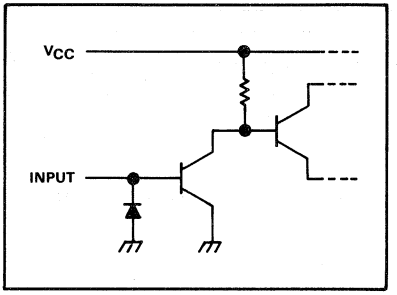
logic symbols (alternatives)



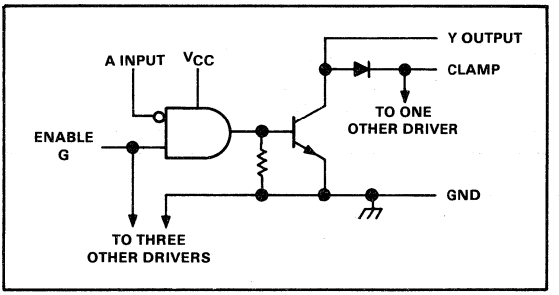


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

equivalent schematic of each input



logic diagram (each driver, positive logic)



absolute maximum ratings (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 30 V
Output current (see Note 1) ..... 0.75 A
Output clamp diode current ..... 1 A
Output Voltage (off-state) ..... 70 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating virtual junction temperature ..... 150°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output current, I_{OL}			600	mA
Output supply voltage in Figure 2 (Inductive switching circuit), V_S			35	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75440 MIN	SN75440 TYP‡	SN75440 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 300 mA			0.4	V
			I_{OL} = 600 mA			0.7	
$V_{R(D)}$	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
$V_{F(D)}$	Output clamp diode forward voltage	I_F = 800 mA			1	1.6	V
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.1	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V		−0.25	−10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25,	V_{IH} = 2 V		1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_{IL} = 0 V	V_{IH} = 2 V,		50	65	mA

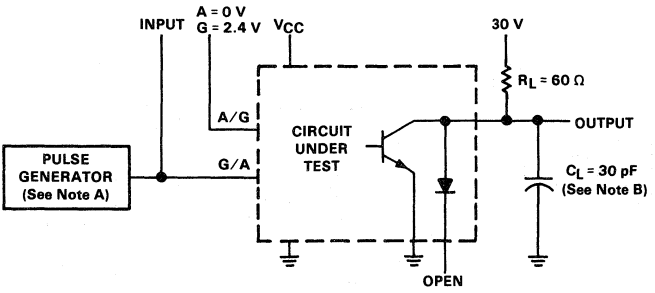
‡All typical values are V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 60 Ω, C_L = 30 pF, See Figure 1	A Input		1.4	5	μs
			G Input		1.5	5	
t_{PHL}	Propagation delay time, high-to-low-level output		A Input		0.1	0.5	μs
			G Input		2.5	5	
t_{TLH}	Transition time, low-to-high-level output				200		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage, after switching	V_S = 35 V, R_L = 70 Ω,	I_O ≈ 500 mA, See Figure 2	V_S −10			mV

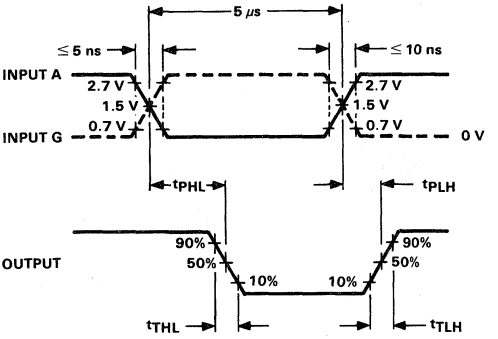
12

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

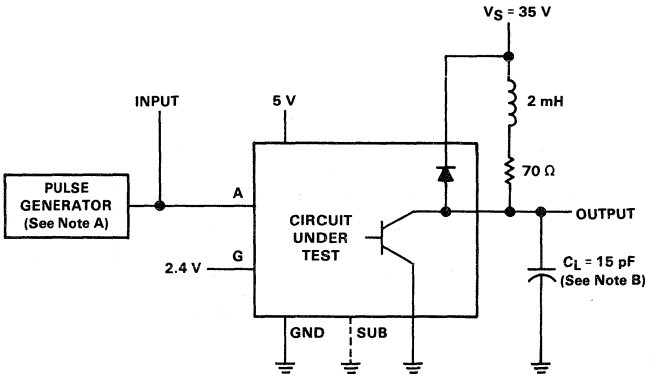
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.



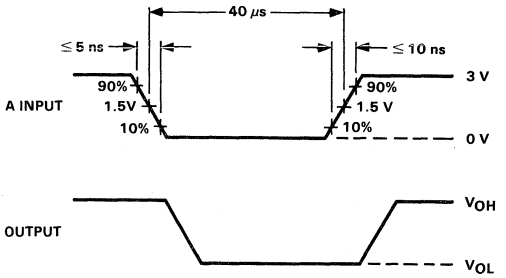
VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS

FIGURE 2. LATCH-UP TEST

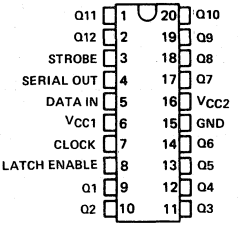
12

TYPE SN75512A
VACUUM FLUORESCENT DISPLAY DRIVER

D2654, MARCH 1983

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

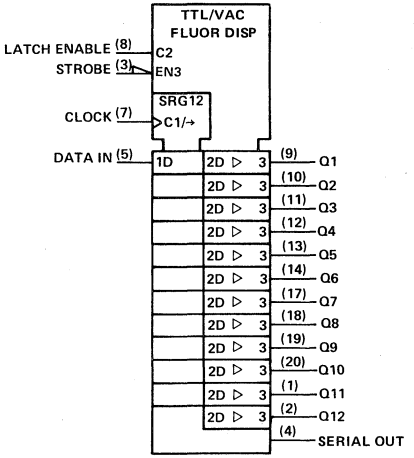
The SN75512A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

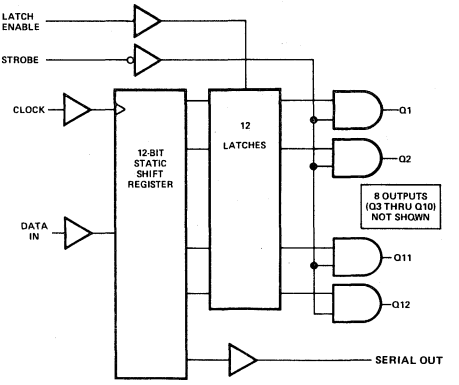
The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the Clock. When high, the Latch Enable input transfers the shift register contents to the outputs of the 12 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Strobe inputs.

The SN75512A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

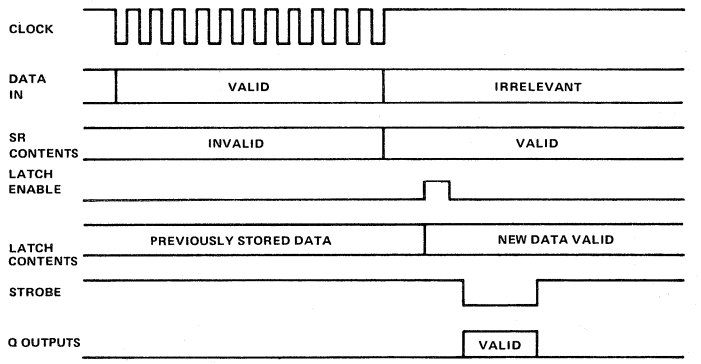
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift§	Determined by Latch Enable¶	R12	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable¶	R12	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R12	Determined by Strobe
	X	H	X	As determined above	New data	R12	Determined by Strobe
STROBE	X	X	H	As determined above	Determined by Latch Enable§	R12	All L
	X	X	L	As determined above	Determined by Latch Enable§	R12	LC1 thru LC12, respectively

H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.

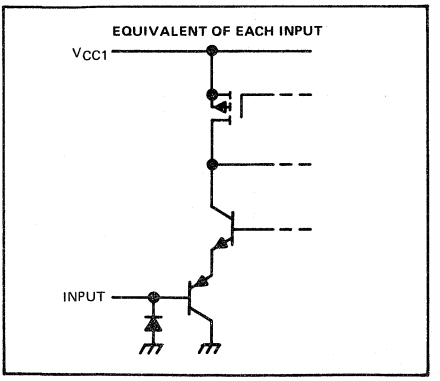
¶New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

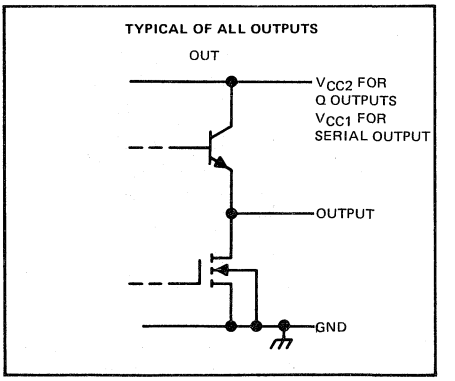
§R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage	5	15	V
V_{CC2}	Supply voltage	0	60	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−25	mA
I_{OL}	Low-level output current		200	μA
f_{clock}	Clock frequency	0	1	MHz
t_w	Pulse duration	500		ns
t_{su}	Setup time, data before CLOCK ↑ (see Figure 1)	250		ns
t_h	Hold time, data after CLOCK ↑ (see Figure 1)	250		ns
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‖	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC2} = 60 V,	I_O = −25 mA	55	57.5		V
		Serial output	I_{OH} = −200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			1	5	V
		Serial output	I_{OL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V		0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V			−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 15 V			800	μA
				V_I = 0 V		10	12	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V,	All outputs high		12	14	mA
				Strobe at 2 V		100	500	μA

‖Typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

12

PARAMETER MEASUREMENT INFORMATION

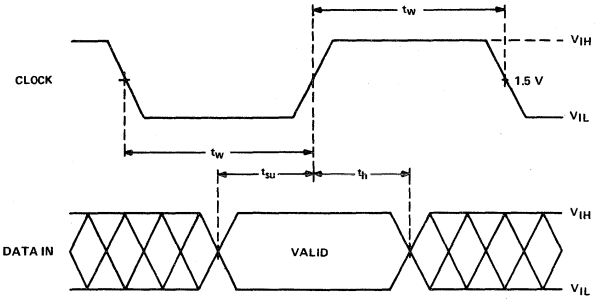


FIGURE 1–INPUT TIMING VOLTAGE WAVEFORMS

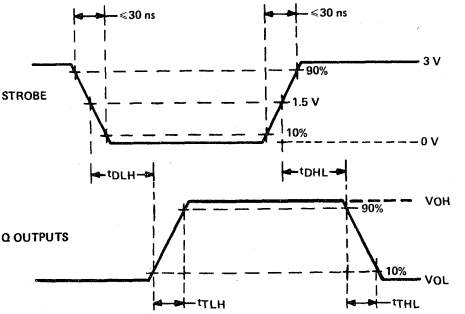


FIGURE 2–SWITCHING-TIME VOLTAGE WAVEFORMS

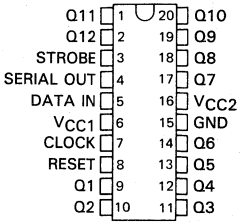
12

TYPE SN75513A VACUUM FLUORESCENT DISPLAY DRIVER

D2721, MARCH 1983

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Input
- Reset Input

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

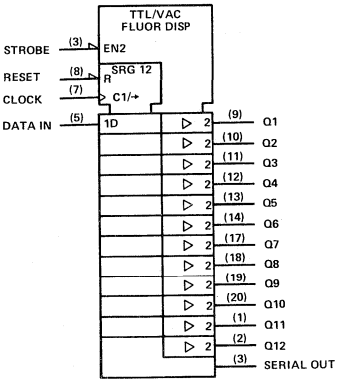
The SN75513A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when left open. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

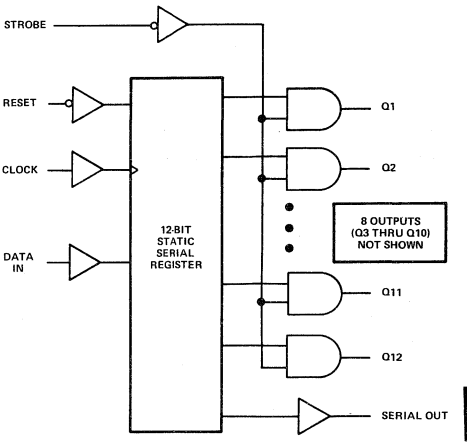
The device consists of a 12-bit shift register and 12 output AND gates. Data is entered into the shift register on the low-to-high transition of the Clock input. The active-low strobe input enables all Q outputs. The Reset input sets the shift register contents to all lows. The serial data output from the shift register may be used to cascade additional devices. This output is not affected by the strobe input.

SN75513A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



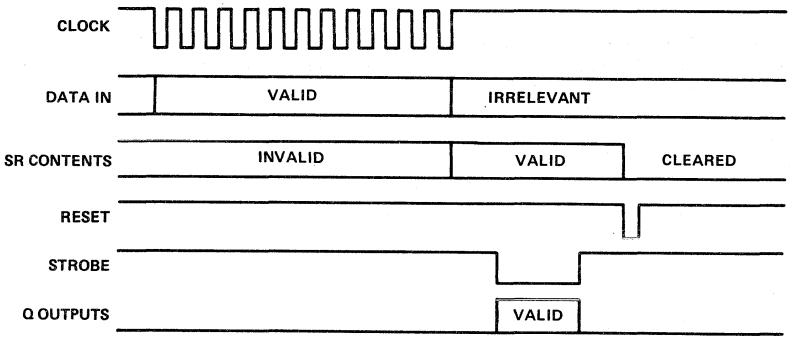
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

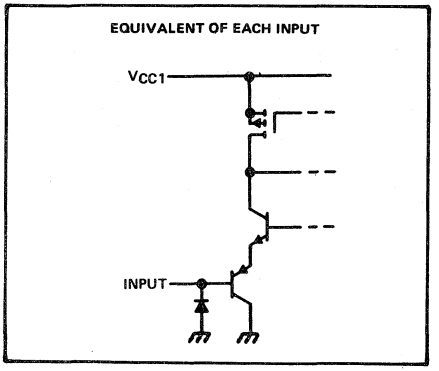
FUNCTION	INPUTS			OUTPUTS		
	RESET	CLOCK	STROBE	SHIFT REGISTERS 1 THRU R12	SERIAL	Q1 THRU Q12
LOAD	H	↑	X	Load and Shift†	R12*	Determined by Strobe
STROBE	H	No↑	H	No Change	R12	All L
	H	No↑	L	No Change	R12	R1 Thru R12, Respectively
RESET	L	H	X	All L	L	All L

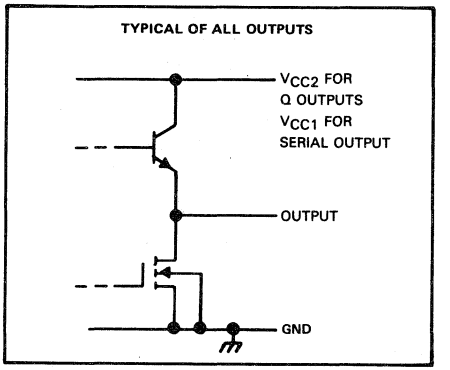
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
†R12 and the serial output take on the state of R11, R11 takes on the state of R10 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply Voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		5		15	V
V_{CC2}	Supply voltage		0		60	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				25	mA
I_{OL}	Low-level output current				200	μA
F_{clock}	Clock frequency	V_{CC1} = 15 V	0		5	MHz
		V_{CC1} = 5 V	0		1	
t_w	Pulse duration, clock high	V_{CC1} = 15 V	100			ns
		V_{CC1} = 5 V	500			
t_{su}	Setup time, data before clock↑ (see Figure 1)	V_{CC1} = 15 V	100			ns
		V_{CC1} = 5 V	250			
t_h	Hold time, data after clock↑ (see Figure 1)	V_{CC1} = 15 V	50			ns
		V_{CC1} = 5 V	250			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_O = −25 mA	57.5	58		V
		Serial output	I_O = −200 μA	9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA		1	5	V
		Serial output	I_{OL} = 200 μA		0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V			−150	μA
I_{CC1}	Supply Current from V_{CC1}		V_{CC1} = 15 V, All inputs at 5 V		1.25	1.5	mA
			V_{CC1} = 15 V, All inputs at 0.8 V		10	12	
I_{CC2}	Supply Current from V_{CC2}		V_{CC1} = 15 V, All outputs high		12	14	mA
			V_{CC1} = 15 V, Strobe at 2 V		0.1	0.5	

†All typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 2			300	ns
t_{DLH}	Delay time, low-to-high-level output				300	ns
t_{THL}	Transition time, high-to-low-level output				500	ns
t_{TLH}	Transition time, low-to-high-level output				500	ns

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PARAMETER MEASUREMENT INFORMATION

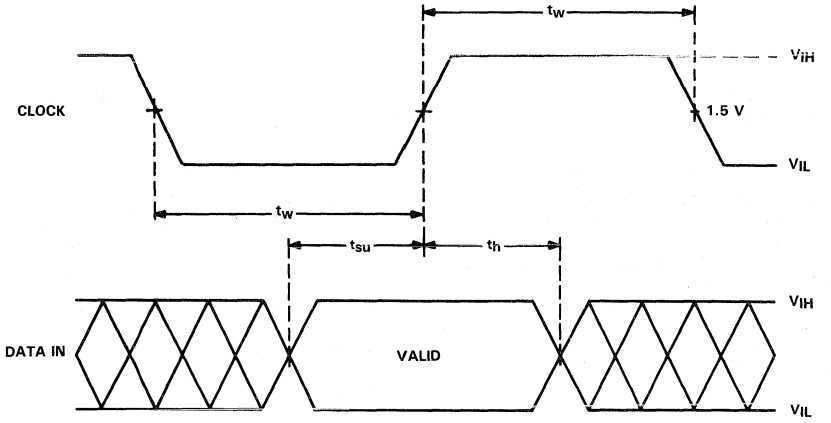


FIGURE 1—INPUT TIMING VOLTAGE WAVEFORMS

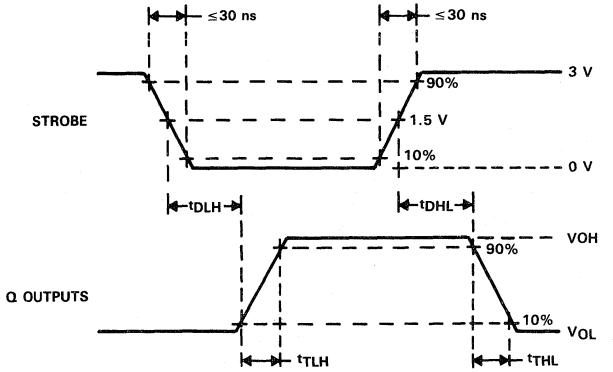


FIGURE 2—SWITCHING-TIME VOLTAGE WAVEFORMS

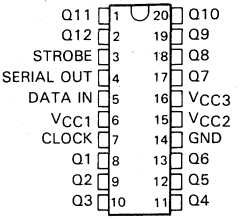
12

TYPE SN75514
VACUUM FLUORESCENT DISPLAY DRIVER

D2732, APRIL 1983

- Each Device Drives 12 Lines
- 125-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

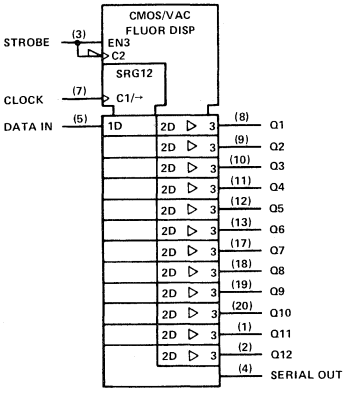
The SN75514 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display. All device inputs are diode-clamped CMOS compatible inputs. The outputs are totem-pole structures formed with double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. On the high-to-low transition of the strobe input, data is transferred from the shift registers to the latches. When Strobe goes high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade additional devices. Serial Out is not affected by the Strobe input.

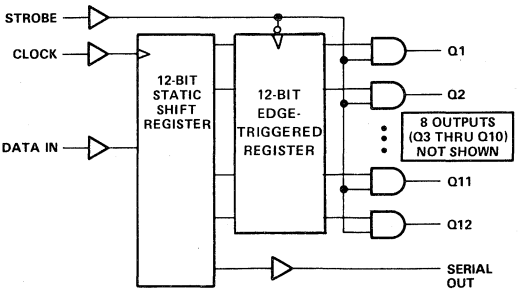
Supply voltage V_{CC2} and V_{CC3} are used to provide 25-milliampere output source current capability at acceptable static device power dissipation. In this mode of operation V_{CC3} should be equal to V_{CC2} + 10 volts. It is possible to operate this device with $V_{CC3} = V_{CC2}$. However, the current capability will be reduced.

The SN75514 is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip—Patented Process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

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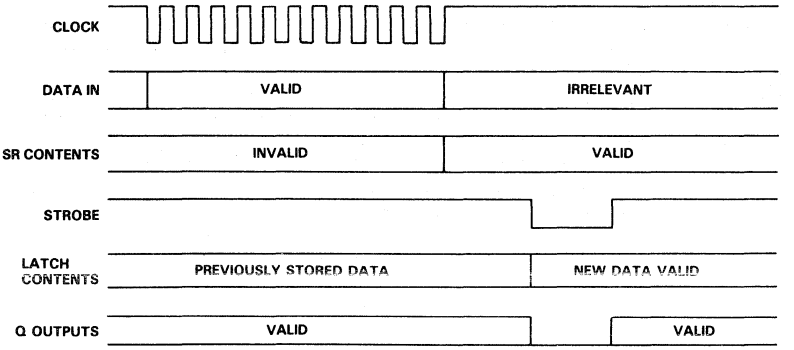
FUNCTION TABLE

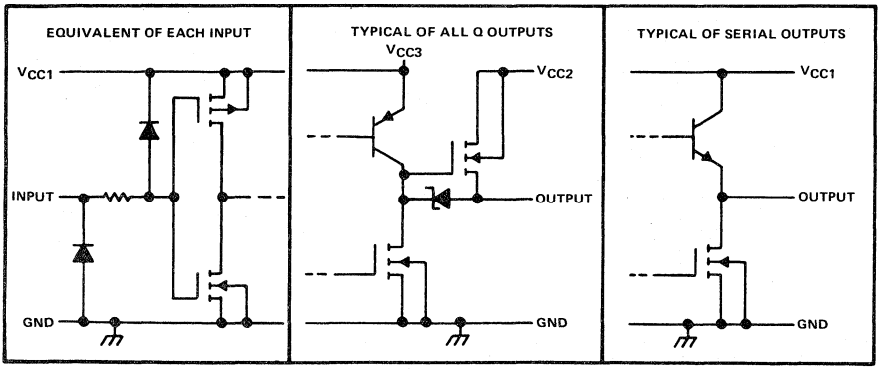
FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	STROBE	R1 THRU R12	LC1 THRU LC12	SERIAL	Q1 THRU Q12
LOAD	↑	X	Load and shift*	Stored data	R12	Determined by Strobe
	Not	X	No change	Stored data	R12	Determined by Strobe
LATCH	X	↓	As determined above	New data	R12	Determined by Strobe
	X	Not	As determined above	Stored data	R12	Determined by Strobe
STROBE	X	H	As determined above	Stored data	R12	LC1 thru LC12, respectively
	X	L	As determined above	Stored data	R12	All L

H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition, ↓ = high-to-low-level transition.
*R12 takes on the state of R11, R11 takes on the state of R10 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 130 V
Supply voltage, V_{CC3} . . . . . 140 V
Supply voltage difference, $V_{CC3} - V_{CC2}$ . . . . . 75 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		4.5		15	V
V_{CC2}	Supply voltage		0		130	V
V_{CC3}	Supply voltage		V_{CC2}		$V_{CC2}+10$	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 4.5 V	3.5			V
		V_{CC1} = 15 V	12			
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 4.5 V			1	V
		V_{CC1} = 15 V			6	
I_{OH}	High-level output current (T_A = 25°C)				−25	mA
I_{OL}	Low-level output current				2.5	mA
f_{clock}	Clock frequency (see Figure 2)		0		7.5	MHz
t_{su}	Data setup time before clock↑ (see Figure 3)		150			ns
t_h	Data hold time after clock↑ (see Figure 3)		150			ns
$t_{d(SL-CH)}$	Delay time, strobe low to clock high	V_{CC} = 4.5 V	1200			ns
		V_{CC} = 15 V	500			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −1 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC2} = 130 V,	I_O = −25 mA	125	126		V
		Serial	I_{OH} = −200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 2.5 mA			1.5	5	V
		Serial	I_{OL} = 200 μA				1	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V		0.01	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V			−5	μA
I_{CC1}	Supply Current from V_{CC1}		V_{CC1} = 15 V				3	mA
			V_{CC1} = 5 V				2.5	
I_{CC2}	Supply Current from V_{CC2}		V_{CC1} = 15 V, V_{CC2} = 130 V, V_{CC3} = 140 V	All outputs high			−5	mA
				All outputs low			0.1	
I_{CC3}	Supply Current from I_{CC3}		V_{CC1} = 15 V, V_{CC2} = 130 V, V_{CC3} = 140 V	All outputs high			5	mA
				Strobe at 0 V			0.1	

†All typical values are at T_A = 25°C.

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switching characteristics, V_{CC1} = 15 V, V_{CC2} = 130 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 1		0.8	μs
t_{DLH}	Delay time, low-to-high-level output			0.8	μs
t_{THL}	Transition time, high-to-low-level output			1	μs
t_{TLH}	Transition time, low-to-high-level output			3	μs

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE V_{CC1}

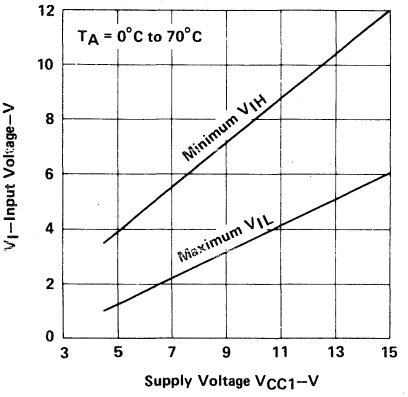

FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE

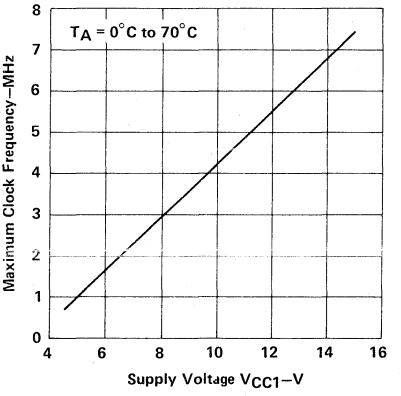

FIGURE 2

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PARAMETER MEASUREMENT INFORMATION

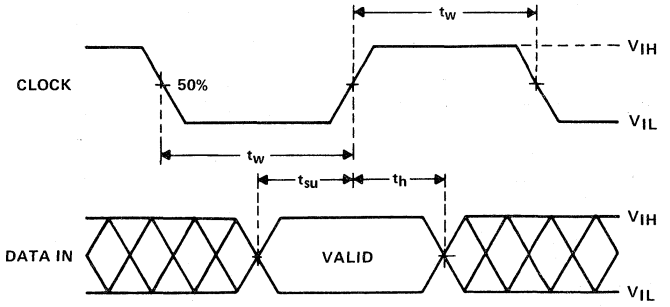

FIGURE 3–INPUT TIMING VOLTAGE WAVEFORMS

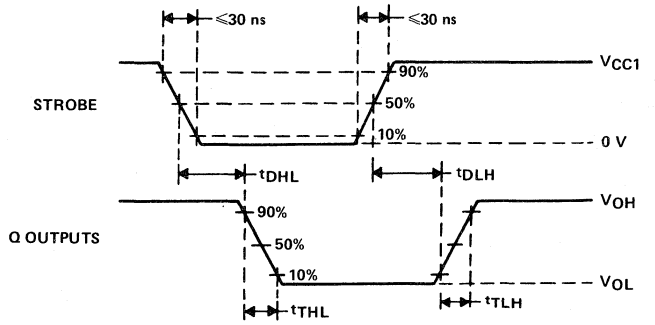

FIGURE 4–SWITCHING-TIME VOLTAGE WAVEFORMS

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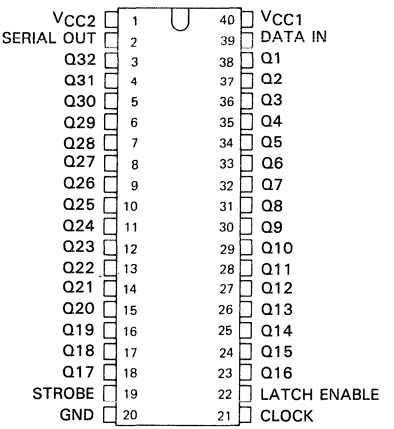
TYPE SN75518
VACUUM FLUORESCENT DISPLAY DRIVER

D2720, MARCH 1983

- Each Device Drives 32 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

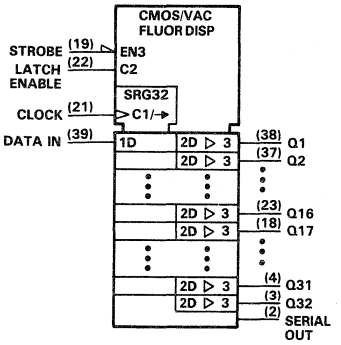
The SN77518 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

The device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. While the latch enable input is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of Latch Enable is latched. The active-low Strobe input enables all Q outputs. When the Strobe input is high, all outputs are low.

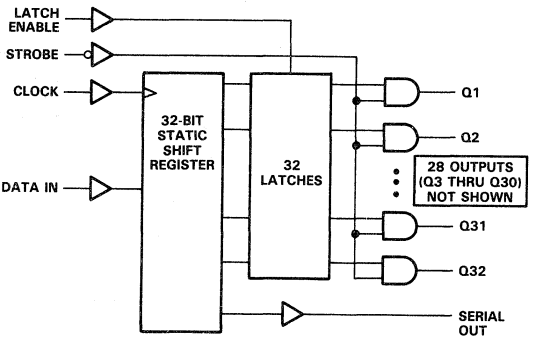
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by the Latch Enable or Strobe Inputs.

The SN75518A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



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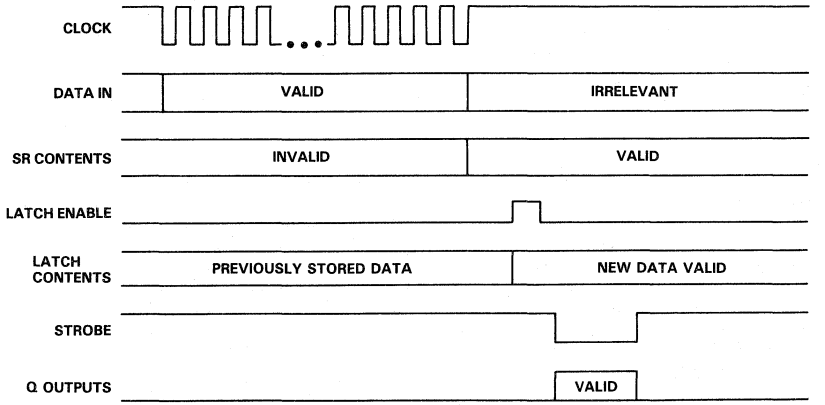
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

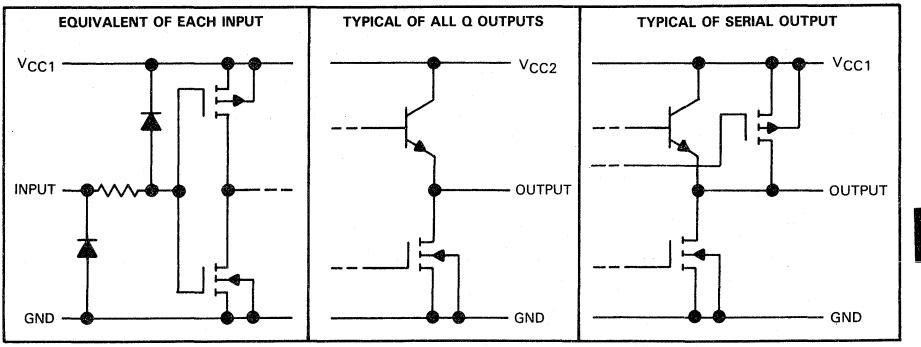
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R32	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable§	R32	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Strobe
	X	H	X	As determined above	New data	R32	Determined by Strobe
STROBE	X	X	H	As determined above	Determined by Latch Enable§	R32	All L
	X	X	L	As determined above	Determined by Latch Enable§	R32	LC1 thru LC12, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
* R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC1}	Supply voltage		4.5	15	V
V_{CC2}	Supply voltage		0	60	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
		V_{CC1} = 15 V	12		
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 4.5 V		1	V
		V_{CC1} = 15 V		6	
I_{OH}	High-level output current			−25	mA
I_{OL}	Low-level output current			2	mA
f_{clock}	Clock frequency (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
		V_{CC1} = 4.5 V	0	1	
$t_{w(CKH)}$	Pulse duration, clock high	V_{CC1} = 10 V to 15 V	100		ns
		V_{CC1} = 4.5 V	500		
$t_{w(CKL)}$	Pulse duration, clock low	V_{CC1} = 10 V to 15 V	100		ns
		V_{CC1} = 4.5 V	500		
t_{su}	Setup time, data before clock↑	V_{CC1} = 10 V to 15 V	75		ns
		V_{CC1} = 4.5 V	150		
t_h	Hold time, data after clock↑	V_{CC1} = 10 V to 15 V	75		ns
		V_{CC1} = 4.5 V	150		
T_A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 5 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_O = −25 mA	57.5	58		V
		Serial output	I_O = −20 μA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			1	V
		Serial output	I_{OL} = 20 μA		0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.1	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V		−0.1	−1	μA
I_{CC1}	Supply Current		V_{CC1} = 4.5 V		1.8	4	mA
			V_{CC1} = 15 V		2	5	
I_{CC2}	Supply Current		Outputs high		7	10	mA
			Outputs low		0.01	0.5	

†All typical values are at T_A = 25°C.

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switching characteristics, V_{CC1} = 5 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 50 pF to GND, See Figure 4		0.6	μs
t_{DLH}	Delay time, low-to-high-level output			1	μs
t_{THL}	Transition time, high-to-low-level output			1	μs
t_{TLH}	Transition time, low-to-high-level output			2	μs

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE V_{CC1}

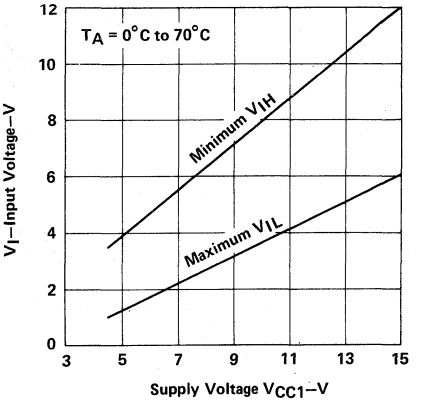

FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE V_{CC1}

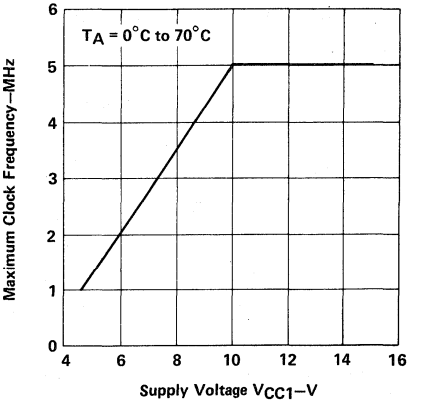

FIGURE 2

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PARAMETER MEASUREMENT INFORMATION

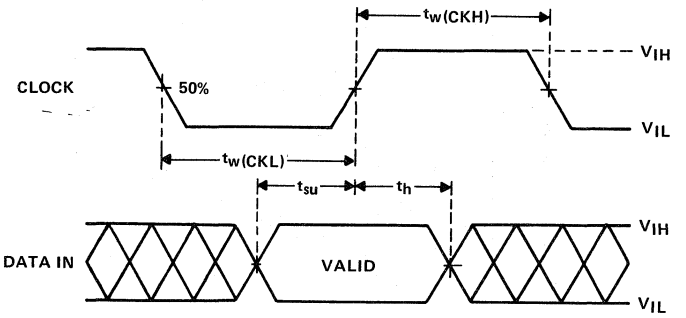

FIGURE 3—INPUT TIMING VOLTAGE WAVEFORMS

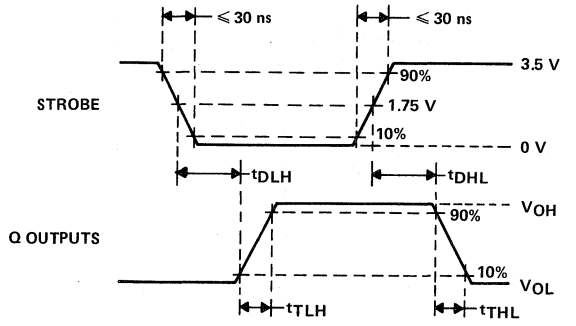

FIGURE 4—SWITCHING-TIME VOLTAGE WAVEFORMS

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TYPES SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVER

D2743, MARCH 1983

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

description

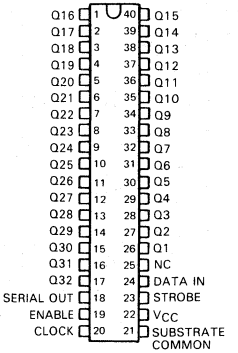
The SN75551 and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence has been reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

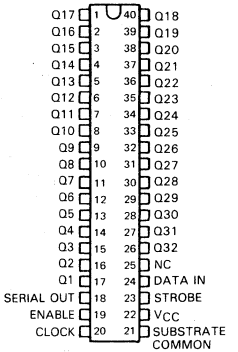
The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN75551



SN75552



NC—no internal connection

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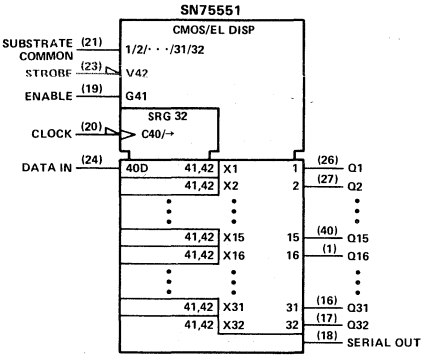
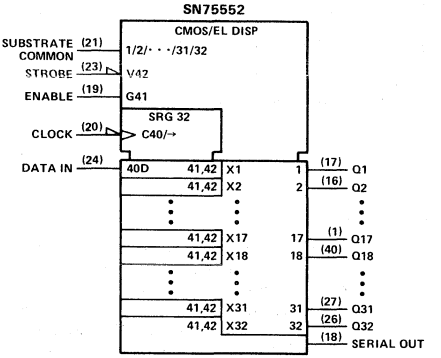
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

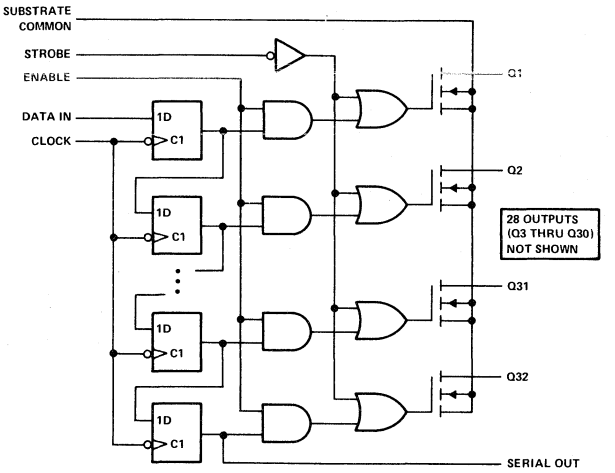
logic symbols‡





‡These symbols are in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

functional block diagram (positive logic)



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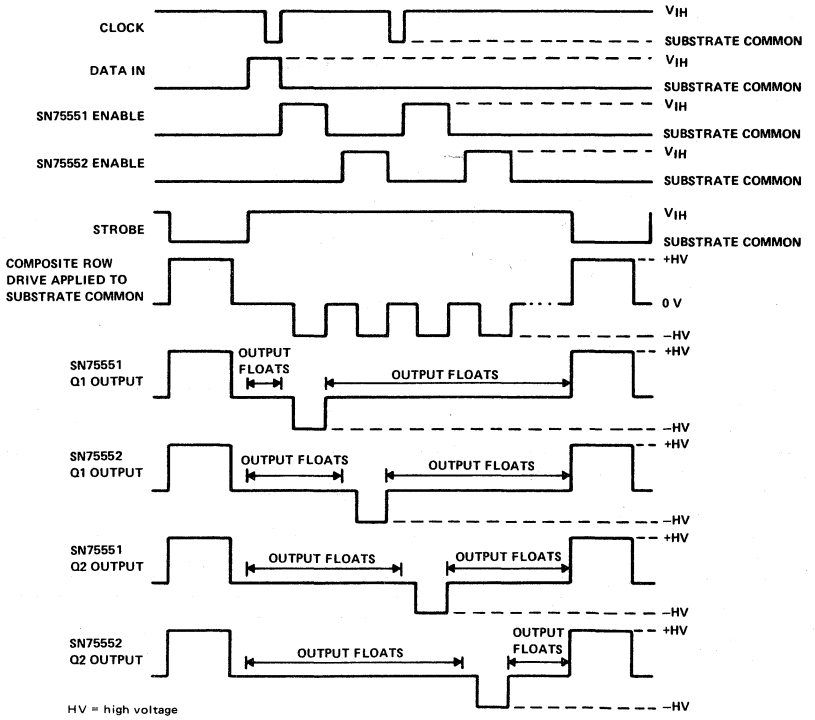
FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift*	R32	Determined by Enable and Strobe
	No ↓	X	X	No Change	R32	Determined by Enable and Strobe
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

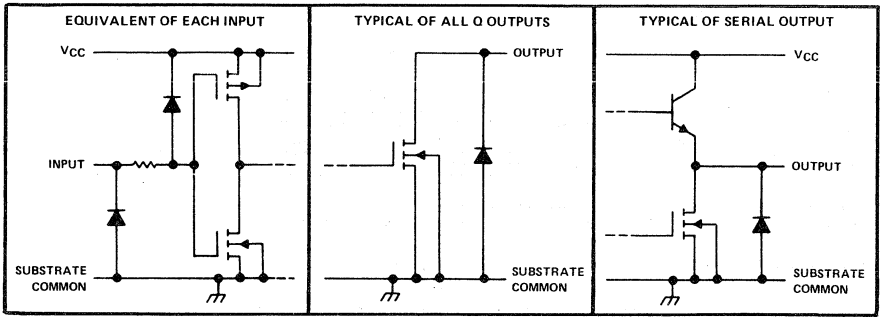
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
*Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Q output voltage, V_O . . . . . 225 V
Input voltage . . . . . V_{CC} +0.3 V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1475 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly to 944 mW at 70°C at the rate of 11.8 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC} = 10.8 V		8.1		11.1	V
		V_{CC} = 15 V		11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC} = 10.8 V		−0.3		2.7	V
		V_{CC} = 15 V		−0.3		3.75	
I_{OL}	Low-level Q output current (see Figure 1)	V_{CC} = 10.8 V	See NOTE 1.	50			mA
		V_{CC} = 15 V		80			
I_{OK}	Output clamp current					−45	mA
f_{clock}	Clock frequency			0		4	MHz
t_w	Pulse duration, clock high or low			125			ns
t_{su}	Data setup time before clock ↓ (see Figure 3)			50			ns
t_h	Data hold time after clock ↓ (see Figure 3)			100			ns
T_A	Operating free-air temperature			0		70	°C

Note 1. $\overline{\text{Strobe}}$ Duty Cycle = 1.0%.

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electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	10.5		V
I_{OL}	Low-Level output voltage	Q outputs	I_{OL} = 50 mA, Note 1.		30	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0 V		−1	μA
I_{CC}	Supply Current from V_{CC}				500	μA

Note 1. $\overline{\text{Strobe}}$ Duty Cycle = 1.0%.

switching characteristics, V_{CC1} = 12 V, T_A = 25°C, see Figure 4

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level Serial Output from Clock	C_L = 20 pF to ground		200	ns
t_{DLH}	Delay time, low-to-high-level Serial Output from Clock			200	ns
t_{on}	Turn on time, Q outputs from Enable	I_{OL} ≈ 50 mA, R_L = 2 kΩ to 130V		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE

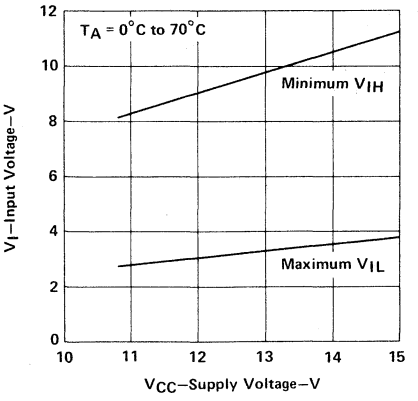

FIGURE 1

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE
For $\overline{\text{Strobe}}$ Duty Cycle = 1.0%

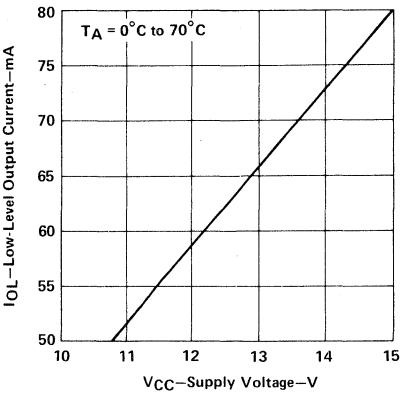

FIGURE 2

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PARAMETER MEASUREMENT INFORMATION

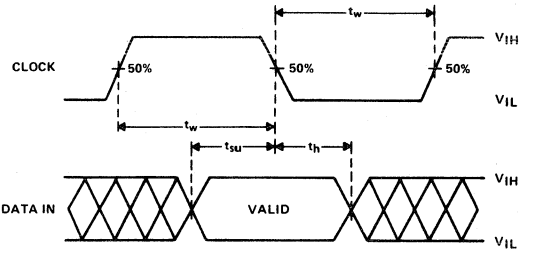

FIGURE 3—INPUT TIMING VOLTAGE WAVEFORMS

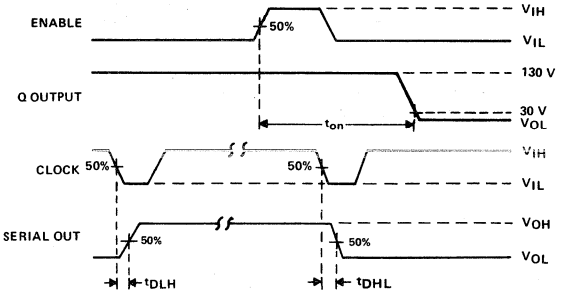

FIGURE 4—VOLTGE WAVEFORMS

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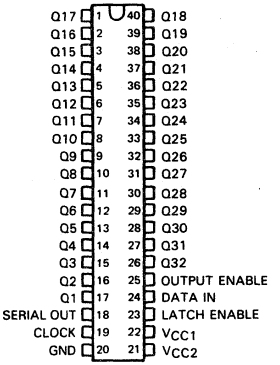
TYPES SN75553, SN75554 ELECTROLUMINESCENT COLUMN DRIVER

D2744, MARCH 1983

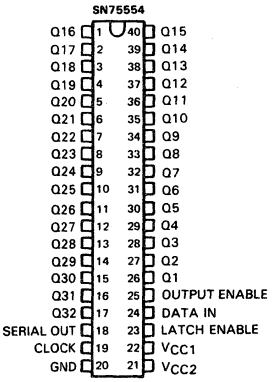
- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN75553



SN75554



description

The SN75553 and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN75554 output sequence has been reversed from the SN75553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

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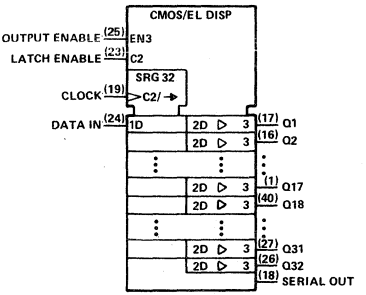
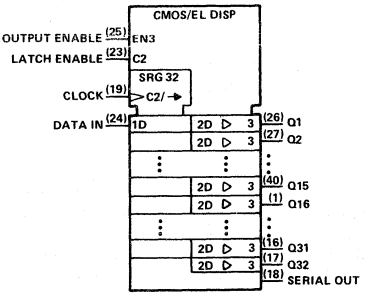
logic symbols‡

SN75553

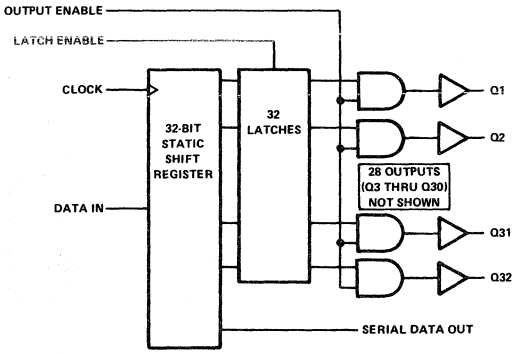


SN75554



‡These symbols are in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

functional block diagram (positive logic)



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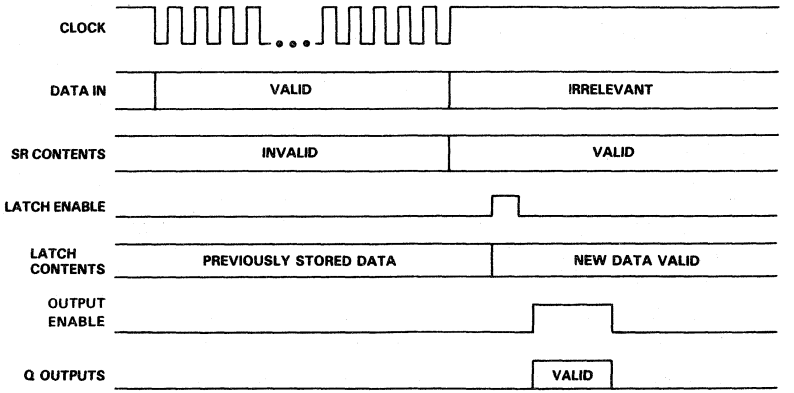
FUNCTION TABLE

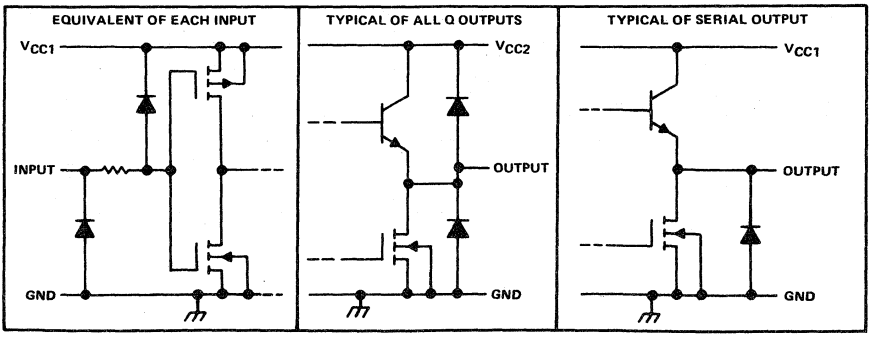
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R32	Determined by Output Enable
	No↑	X	X	No change	Determined by Latch Enable§	R32	Determined by Output Enable
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Output Enable
	X	H	X	As determined above	New data	R32	Determined by Output Enable
OUTPUT ENABLE	X	X	L	As determined above	Determined by Latch Enable§	R32	All L
	X	X	H	As determined above	Determined by Latch Enable§	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
*R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
†New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1470 mW
Ground Current . . . . . 700 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 944 mW at 70°C at the rate of 11.8 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		10.8	12	15	V
V_{CC2}	Supply voltage		0		60	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
		V_{CC1} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
		V_{CC1} = 15 V	−0.3		3.75	
I_{OH}	High-level output current		−15			mA
I_{OL}	Low-level output current		15			mA
I_{OK}	Output clamp current				20	mA
f_{clock}	Clock frequency		0		6.25	MHz
t_w(CK)	Pulse duration, clock high or low (see Figure 2)		80			ns
t_{su}	Data setup time before clock ↑ (see Figure 2)		20			ns
t_h	Data hold time after clock ↑ (see Figure 2)		80			ns
t_w(LE)	Pulse duration, latch enable (see Figure 4)		80			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		Serial output	I_O = −100 μA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0 V		−1	μA
I_{CC1}	Supply Current from V_{CC1}				5	mA
I_{CC2}	Supply Current from V_{CC2}		Outputs high		10	mA
			Outputs low		0.5	

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switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level Serial output from Clock	C_L = 20 pF to ground, See Figure 3		140	ns
t_{DLH}	Delay time, low-to-high-level Serial output from Clock			140	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from Latch Enable	R_L = 3.5 kΩ to V_{CC2}, I_{OL} ≈ 15 mA, See Figure 4		500	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from Latch Enable	R_L = 3.8 kΩ to ground, I_{OL} ≈ −15 mA, See Figure 4		1.0	μs

RECOMMENDED OPERATION CONDITIONS

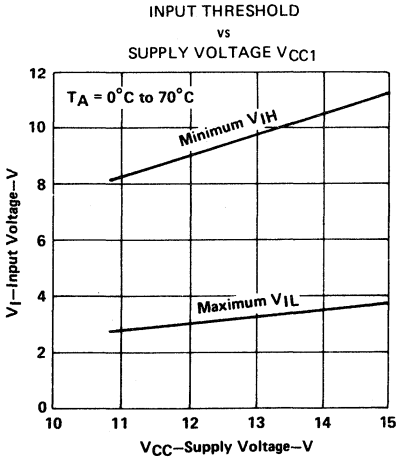

FIGURE 1

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PARAMETER MEASUREMENT INFORMATION

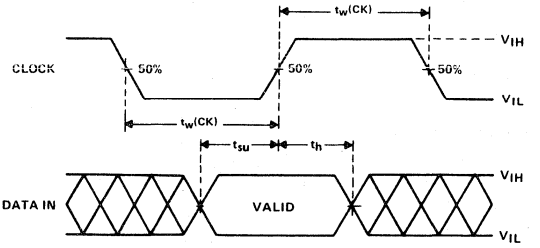

FIGURE 2—INPUT TIMING VOLTAGE WAVEFORMS

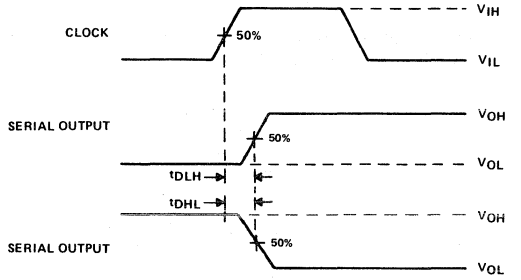

FIGURE 3—VOLTAGE WAVEFORMS FOR DELAY AND TRANSITION TIMES, CLOCK TO SERIAL OUTPUT

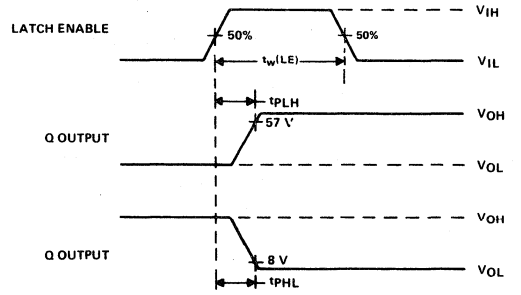

FIGURE 4—VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

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SN75555, SN75556
ELECTROLUMINESCENT COLUMN DRIVER

D2744, APRIL 1985

- Each Device Drives 32 Electrodes
- 90-V Output Voltage Swing Capability Using Ramped Supply
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

description

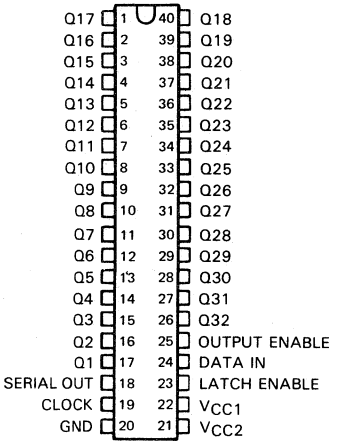
The SN75555 and SN75556 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN75556 output sequence has been reversed from the SN75555 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Data must be loaded into the latches and Output Enable must be high before supply voltage V_{CC2} is ramped up.

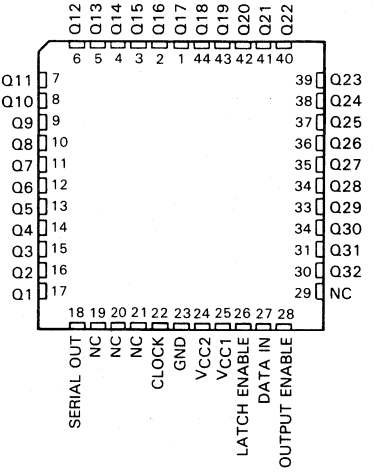
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN75555 and SN75556 are characterized for operation from 0°C to 70°C.

SN75555 . . .N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



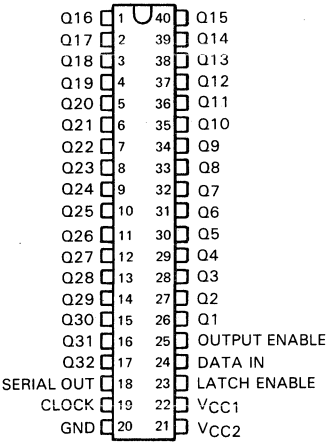
SN75555 . . . FN
PLASTIC CHIP CARRIER PACKAGE
(TOP VIEW)



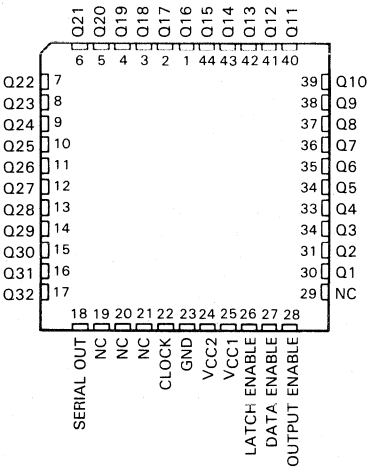
NC—No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

SN75556 . . . N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



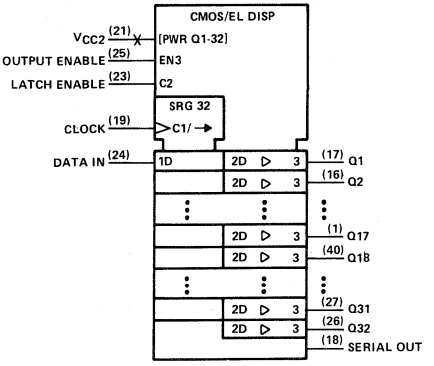
SN75556 . . . FN
PLASTIC CHIP CARRIER PACKAGE
(TOP VIEW)



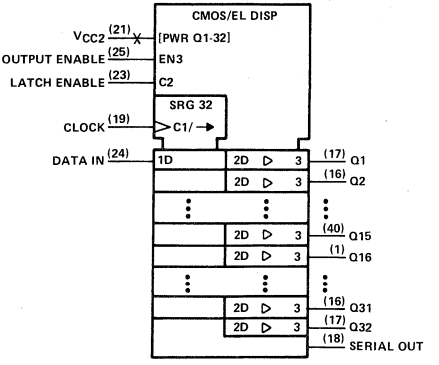
NC—No internal connection

logic symbols†

SN75555



SN75556



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for N packages.

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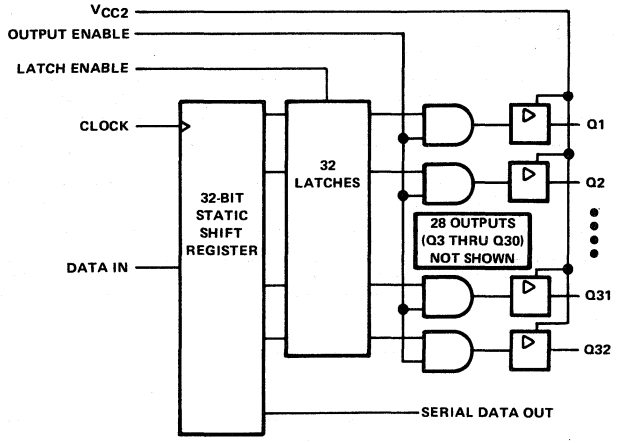
logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by Latch Enable‡	R32	Determined by Output Enable
	No↑	X	X	No change	Determined by Latch Enable‡	R32	Determined by Output Enable
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Output Enable
	X	H	X	As determined above	New data	R32	Determined by Output Enable
OUTPUT ENABLE	X	X	L	As determined above	Determined by Latch Enable‡	R32	All L
	X	X	H	As determined above	Determined by Latch Enable‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

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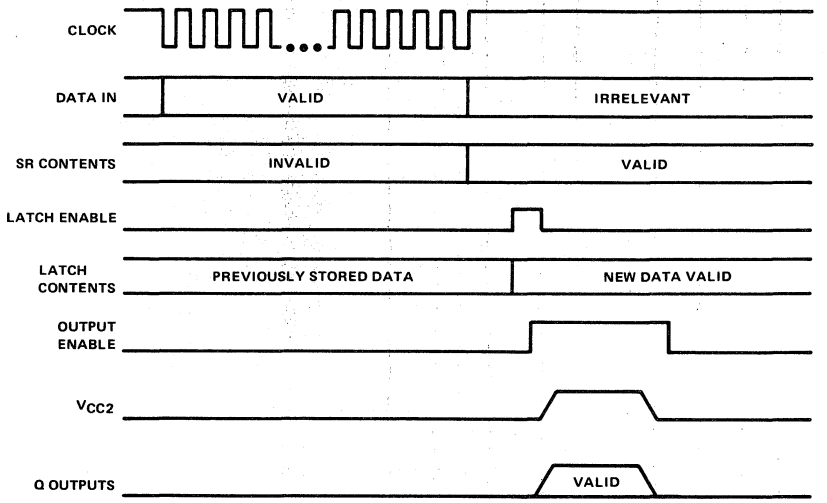
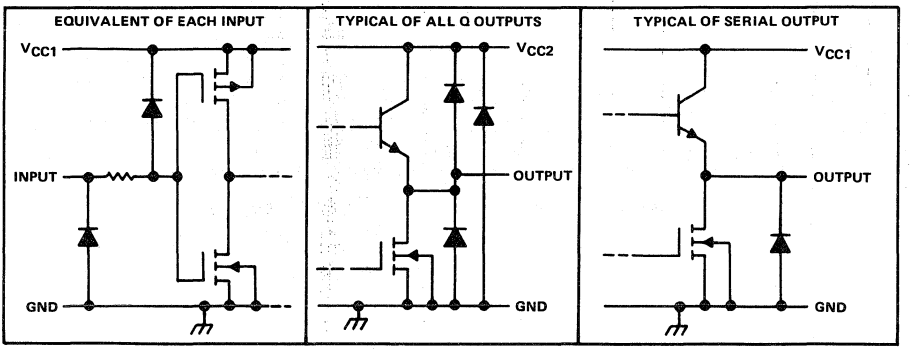
typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} (See Note 2) . . . . . 90 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
N package . . . . . 1250 mW
FN package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These devices have been designed to be used in applications where the high-voltage supply, V_{CC2}, is switched to ground before changing the state of the outputs.
3. For operation above 25°C free-air temperature, derate the N package at the rate of 10 mW/°C and the FN package at the rate of 13.6 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage			10.8	12	15	V
V_{CC2}	Supply voltage			0		80	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 10.8 V		8.1		11.1	V
		V_{CC1} = 15 V		11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 10.8 V		−0.3		2.7	V
		V_{CC1} = 15 V		−0.3		3.75	
I_{OH}	High-level output current			−15			mA
I_{OL}	Low-level output current			15			mA
I_{OK}	Output clamp current					20	mA
f_{clock}	Clock frequency			0		6.25	MHz
$t_{w(CLK)}$	Pulse duration, clock high or low (see Figure 2)			80			ns
$t_{w(LE)}$	Pulse duration, latch enable (see Figure 4)			80			ns
t_{su}	Setup time	Data before clock ↑ (see Figure 2)		20			ns
		Output enable before V_{CC}↑ (see Figure 4)		500			
t_h	Hold time	Data after clock ↑ (see Figure 2)		80			ns
		Output enable after V_{CC}↑ (see Figure 4)		100			
dV/dt	Rate of rise for V_{CC2} (see Figure 4)					80	V/μs
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 80 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	77		V
		Serial output	I_O = −100 μA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				2	mA
I_{CC2}	Supply current from V_{CC2}				5	mA

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switching characteristics, V_{CC1} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level Serial output from Clock	C_L = 20 pF to ground, V_{CC2} = 0, (See Figure 3)		140	ns
t_{PLH}	Propagation delay time, low-to-high level Serial output from Clock			140	ns
t_d	Delay time, V_{CC2} to Q outputs	dV/dt = 80 V/μs (See Figure 4)		100	ns

RECOMMENDED OPERATION CONDITIONS

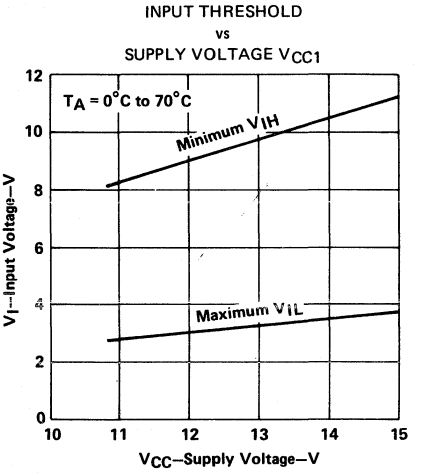

FIGURE 1

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PARAMETER MEASUREMENT INFORMATION

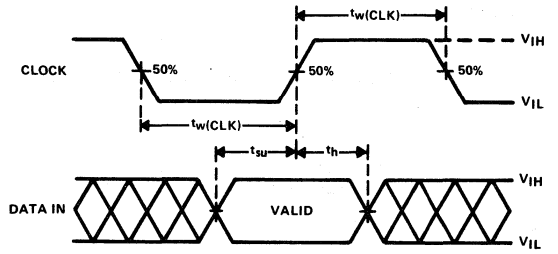

FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

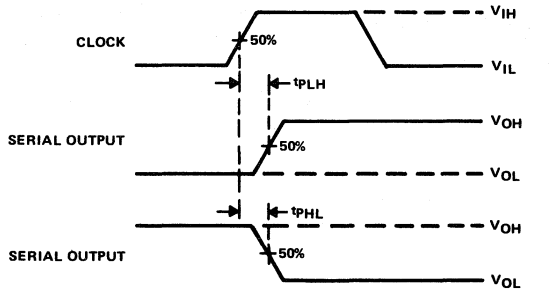

FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

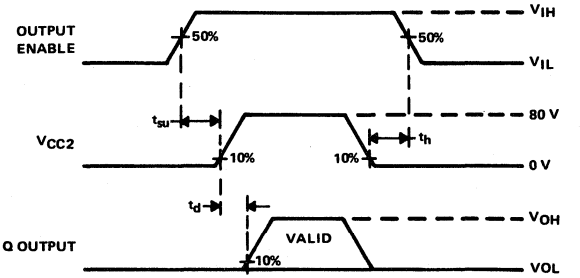

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

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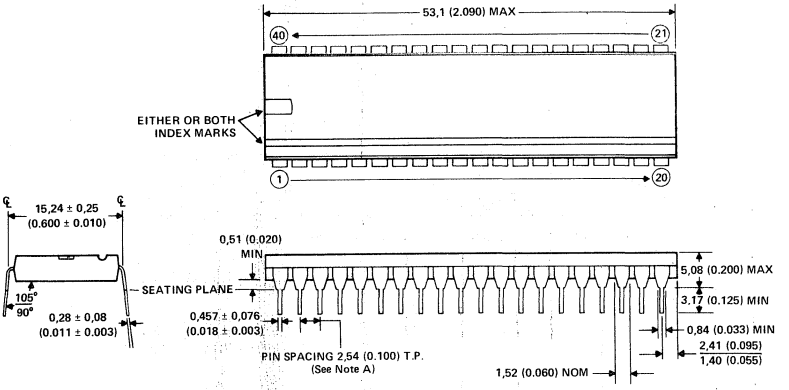
MECHANICAL DATA

40-pin N plastic dual-in-line package

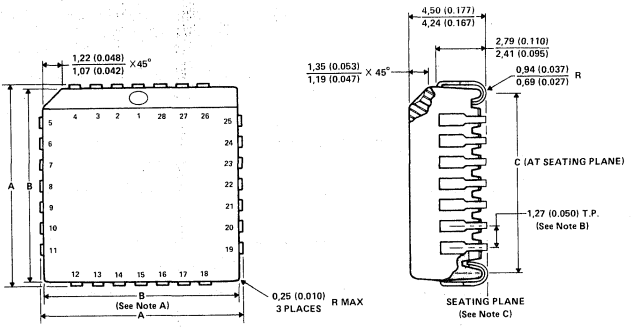


NOTE: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

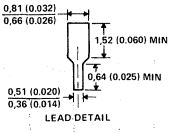
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

44-pin FN plastic chip carrier package

(28-terminal package shown)



NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,80 (0.665)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)



NOTES: A. Centerline of center pin each side is within 0,10 (0.004)) of package centerline as determined by dimension B.
B. Location of each is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0.10 (0.004).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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TEXAS INSTRUMENTS

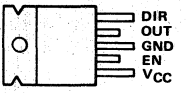
TYPES SN75603, SN75604, SN75605 HIGH-CURRENT HALF-H DRIVERS

D2832, MARCH 1984

- Three-State Outputs
- Continuous Output Current of ±2 A
- Outputs Can Switch 40 V
- Transient Suppression
- Thermal Shutdown
- Inputs Compatible with TTL and 5-V CMOS
- V_{CC} Range: 8 V to 40 V
- Internal Protection Against Simultaneous Conduction of Sink and Source Sides of the Output

KC, KH, AND KV PACKAGES

(TOP VIEW)



GROUND TERMINAL IS IN ELECTRICAL CONTACT WITH MOUNTING BASE

FUNCTION TABLE

INPUTS		OUTPUT		
EN	DIR	SN75603	SN75604	SN75605
L	L	Z	Z	L
L	H	Z	Z	Z
H	L	L	H	Z
H	H	H	L	H

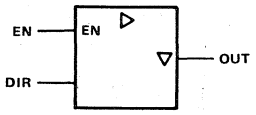
description

The SN75603, SN75604, and SN75606 are high-current half-H drivers designed for high-current switching of bidirectional loads at voltages from 8 V to 40 V. The devices are ideal for the switching of bidirectional dc and stepping motors.

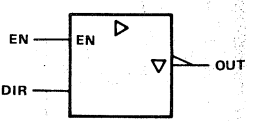
The SN75603 and SN75604 are designed to be used together in pairs, which eliminates the need for additional control logic. The SN75605 is a functional replacement for Sprague UDN2949. It has a single direction input with propagation delays that prevent the sink and source sides of the output from conducting simultaneously. The enable input in conjunction with the direction input of the SN75605 allows for a high-impedance output state.

logic symbols

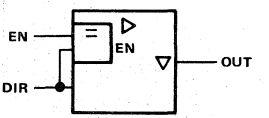
SN75603



SN75604

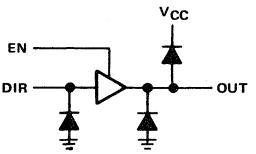


SN75605

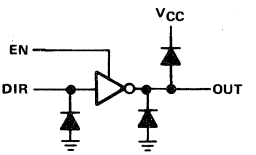


logic diagrams (positive logic)

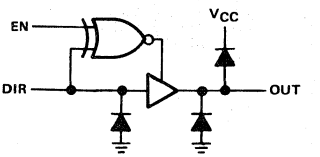
SN75603



SN75604



SN75603



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PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 40 V
Output voltage, V_O . . . . . 42 V
Input voltage, V_I . . . . . 40 V
Output current, I_O . . . . . ±2.5 mA
Power dissipation at (or below) 125°C case temperature . . . . . 6.25 W
Operating case temperature range . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	8		40	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_C	Case temperature	−40		125	°C
T_J	Junction temperature	−40		150	°C

electrical characteristics, V_{CC} = 8 V to 40 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA		−0.9	−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −1 A	V_{CC}−1.5	V_{CC}−0.9		V
		I_{OH} = −2 A	V_{CC}−2	V_{CC}−1.2		
		V_{CC} = 40 V, I_{OH} = 0	V_{CC}−10			
V_{OL}	Low-level output voltage	I_{OL} = 1 A		0.9	1.5	V
		I_{OL} = 2 A		1.1	2	
		V_{CC} = 40 V, I_{OL} = 0			10	mV
V_{OK}	Output clamp voltage	I_{OK} = 1 A		1.2	1.5	V
		I_{OK} = 2 A		1.4	2	
I_{OZ}	High-impedance-state output current	V_O = 40 V		0.1	100	μA
		V_O = 0		−0.1	−100	
I_{IH}	High-level input current	V_I = 5.5 V		0.01	10	μA
I_{IL}	Low-level input current	V_I = 0		−8	−20	μA
I_{CC}	Supply current	Output at high impedance		16	30	mA
		Output at high level		35	50	
		Output at low level		30	40	

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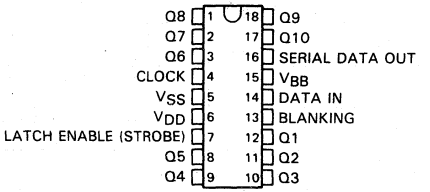
TL4810B
VACUUM FLUORESCENT DISPLAY DRIVER

D2715, DECEMBER 1984

- **Each Device Drives 10 Lines**
- **60-V Output Voltage Rating**
- **40-mA Output Source Current**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Latches on All Driver Outputs**
- **Improved Direct Replacement for UCN4810A and TL4810A**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

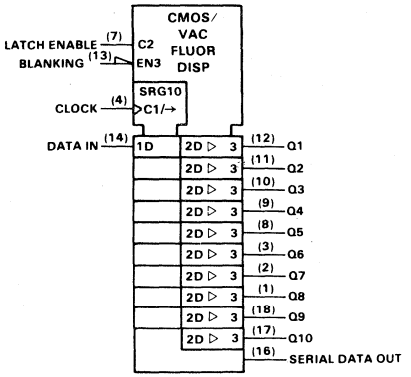
The TL4810B is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and will be latched when the latch enable is low. When the blanking input is high, all outputs are low.

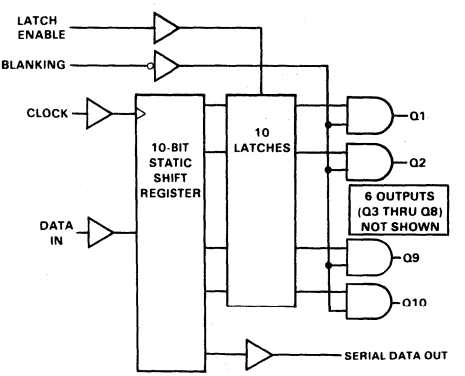
Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 volts, and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The TL4810B is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



†BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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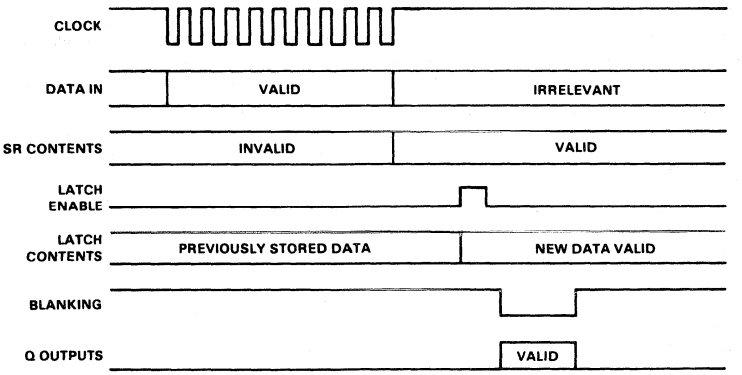
FUNCTION TABLE

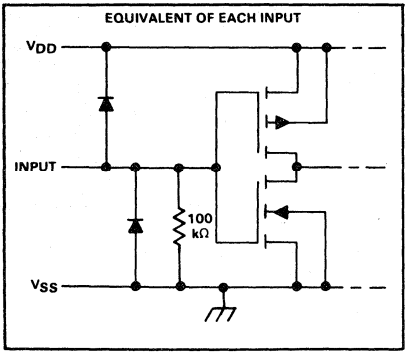
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING	R1 THRU R10	LC1 THRU LC10†	SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift‡	Determined by Latch Enable†	R10	Determined by Blanking
	No ↑	X	X	No change	Determined by Latch Enable†	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable†	R10	All L
	X	X	L	As determined above	Determined by Latch Enable†	R10	LC1 thru LC12 respectively

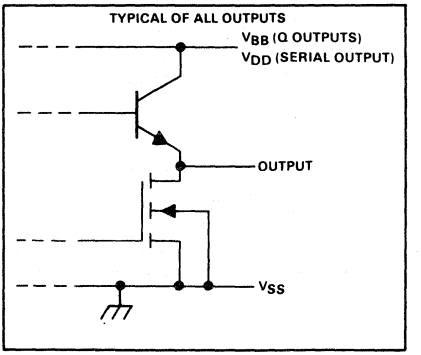
H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
‡Register R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Driver supply voltage, V_{BB} . . . . . 70 V
Output voltage . . . . . 70 V
Input voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous output current . . . . . −40 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 560 mW at 70°C at the rate of 7.0 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75		15.75	V
V_{BB}	Supply voltage		5		60	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	for V_{DD} = 5 V	3.5		5.3	V
		for V_{DD} = 15 V	13.5		15.3	
V_{IL}	Low-level input voltage		−0.3†		0.8	V
I_{OH}	Continuous high-level output current				−25	mA
T_A	Operating free-air temperature		0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 4.75 V to 15.75 V, V_{BB} = 60 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		Serial output	V_{DD} = 5 V,	I_{OH} = −100 μA	4	4.5		
			V_{DD} = 15 V,	I_{OH} = −100 μA	14	14.7		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 μA,	Blanking input at V_{DD}		0.5	1	V
		Serial output	V_{DD} = 5 V,	I_{OL} = 100 μA		0.05	0.1	
			V_{DD} = 15 V,	I_{OL} = 100 μA		0.02	0.1	
I_{OL}	Low-level output current (pull-down current)		V_O = 60 V,	Blanking input at V_{DD}	3	3.7		mA
$I_{O(off)}$	Off-state output current		V_O = 0, T_A = 70°C	Blanking input at V_{DD},		−1	−15	μA
I_{IH}	High-level input current		V_I = V_{DD}			30	50	μA
I_{BB}	Supply current from V_{BB}		All outputs high			2.7	4	mA
			All outputs low			0.5	1	
I_{DD}	Supply current from V_{DD}		All inputs at 0 V, One output high	V_{DD} = 5 V		10	50	μA
				V_{DD} = 15 V		10	100	
			All inputs at 0 V, All outputs low	V_{DD} = 5 V		10	50	
				V_{DD} = 15 V		10	100	

† All typical values are at T_A = 25°C, except for $I_{O(off)}$.

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timing requirements for V_{DD} = 5 V and V_{DD} = 15 V, T_A = 0°C to 70°C

PARAMETER		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{w(CKH)}$	Pulse duration, clock high	250	165		50	35		ns
$t_{w(LEH)}$	Pulse duration, latch enable high	250	75		50	15		ns
$t_{su(D)}$	Setup time, data before clock↑	125	65		25	5		ns
$t_{h(D)}$	Hold time, data after clock↑	125	25		25	10		ns
$t_{CKH-LEH}$	Delay time, clock ↑ to latch enable high	125	30		25	1		ns

†All typical values are at T_A = 25°C.

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output	V_{DD} = 5 V		1		μs
		V_{DD} = 15 V		0.5		

PARAMETER MEASUREMENT INFORMATION

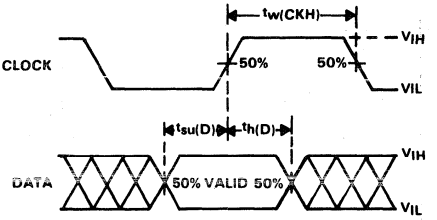


FIGURE 1. INPUT TIMING

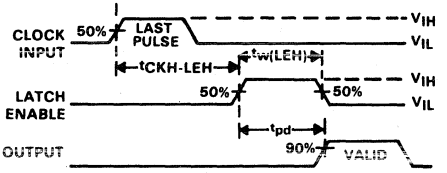
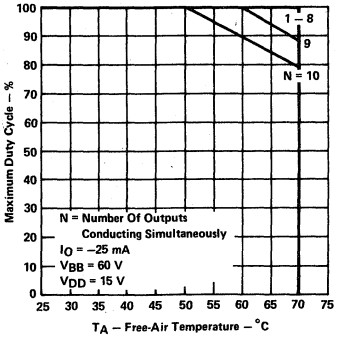


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION

THERMAL INFORMATION
DUTY CYCLE
vs
FREE-AIR TEMPERATURE



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TEXAS INSTRUMENTS

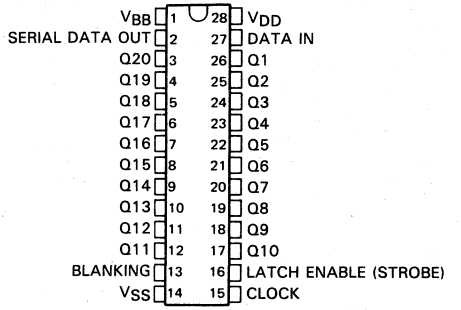
ADVANCE INFORMATION

TL5812
VACUUM FLUORESCENT DISPLAY DRIVER

D2914, OCTOBER 1985

- **Drives Up to 20 Lines**
- **70-V Output Voltage Swing Capability**
- **40-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Direct Replacement for Sprague UCN5812A**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

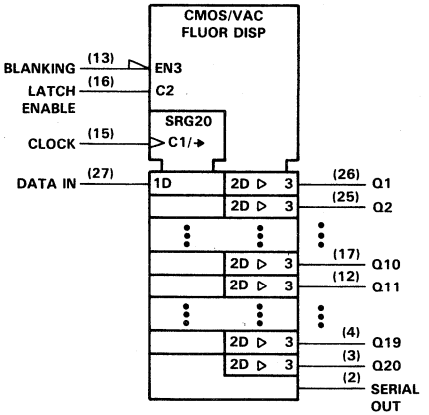
The TL5812 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of the clock input. Parallel data is transferred to the output buffers through a 20-bit D-type latch while the Latch Enable input is high and is latched when the Latch Enable input is low. When the blanking input is high, all outputs are low.

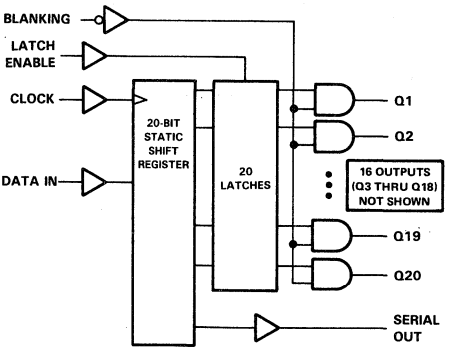
The outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 volts and a source-current capability of 40 milliamperes. All inputs are CMOS compatible.

The TL5812 is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — patented process.
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

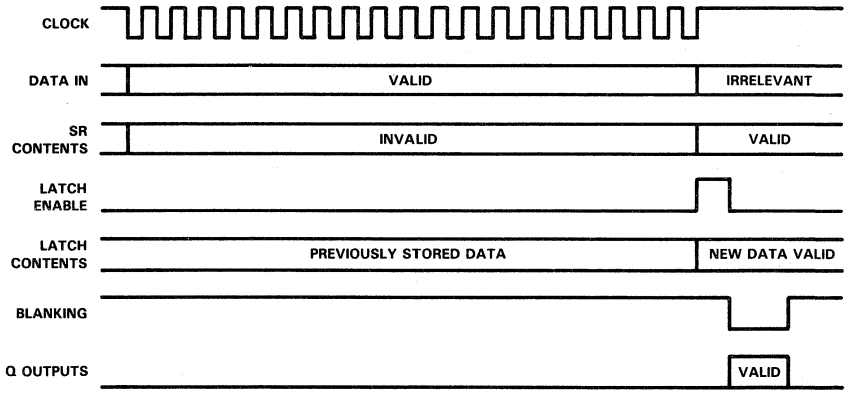
TEXAS INSTRUMENTS

FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING	R1 THRU R20	LC1 THRU LC20	SERIAL	Q1 THRU Q20
LOAD	↑	X	X	Load and shift†	Determined by	R20	Determined by
	No↑	X	X	No change	Latch Enable‡	R20	Blanking
LATCH	X	L	X	As determined above	Stored data	R20	Determined by
	X	H	X	As determined above	New data	R20	Blanking
BLANK	X	X	H	As determined above	Determined by	R20	All L
	X	X	L	As determined above	Latch Enable‡	R20	LC1 thru LC20, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R20 takes on the state of R19, R19 takes on the state of R18,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



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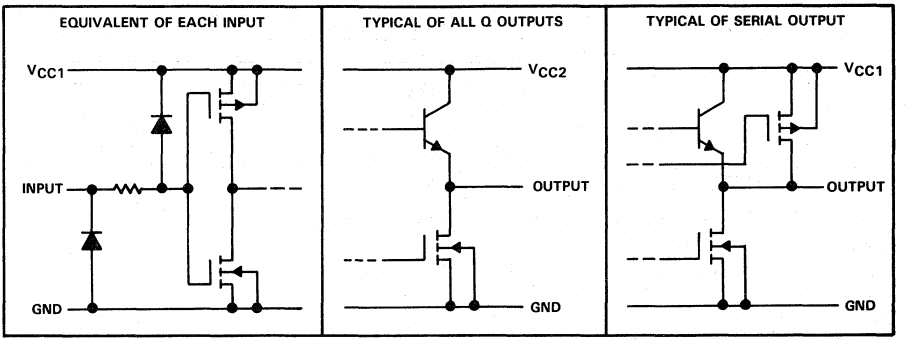
schematics of inputs and outputs



absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{BB} . . . . . 70 V
Output voltage, V_O . . . . . 70 V
Input voltage, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Output current, I_O . . . . . −40 mA
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) . . . . . 1250 mW
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260 °C

NOTES 1. All voltage values are with respect to V_{SS}.
2. For operation above 25 °C free-air temperature, derate linearly to 800 mW at 70 °C at the rate of 10 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		15	V
Supply voltage, V_{BB}	0		60	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	V_{DD} −1.5		V_{DD} +0.3	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
High-level output current, I_{OH}			−40	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58.2		V
		Serial outputs	V_{DD} = 5 V,	I_{OH} = −20 μA	4.5	4.9		
			V_{DD} = 15 V,	I_{OH} = −20 μA	14.5	14.9		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	Blanking at V_{DD}		0.7	1.5	V
		Serial outputs	V_{DD} = 5 V,	I_{OL} = 20 μA		0.06	0.3	
			V_{DD} = 15 V,	I_{OL} = 20 μA,		0.03	0.3	
I_{IH}	High-level input current		V_I = V_{DD}			0.3	1	μA
I_{IL}	Low-level input current		V_I = 0			−0.3	−1	μA
I_{OL}	Low-level output current (pull down current)		V_O = 60 V,	Blanking at V_{DD}	2.5	3.2		mA
$I_{O(off)}$	Off-state output current		V_O = 0,	Blanking at V_{DD}		< −1	−15	μA
I_{BB}	Supply current from V_{BB}		Outputs high			3.5	8	mA
			Outputs low			0.02	0.5	
I_{DD}	Supply current from V_{DD}		V_{DD} = 5 V			1.5	3	mA
			V_{DD} = 15 V			1.7	4	

† All typical characteristics are at T_A = 25°C.

timing requirements over operating free-air temperature range

PARAMETER			MIN	MAX	UNIT
t_{wCKH}	Pulse duration, clock high	V_{DD} = 5 V	500		ns
		V_{DD} = 15 V	100		
t_{wLEH}	Pulse duration, latch enable high	V_{DD} = 5 V	500		ns
		V_{DD} = 15 V	100		
t_{suD}	Setup time, data before clock↑	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		
t_{hD}	Hold time, data after clock↑	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		
$t_{CKH-LEH}$	Delay time, clock↑ to latch enable high	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output	V_{DD} = 5 V		2.2		μs
		V_{DD} = 15 V		0.8		

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PARAMETER MEASUREMENT INFORMATION

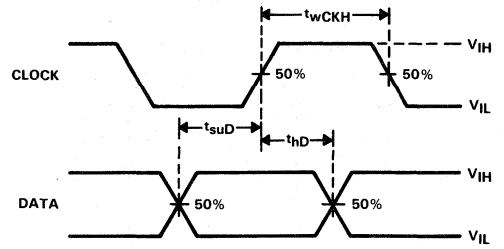

FIGURE 1. INPUT TIMING

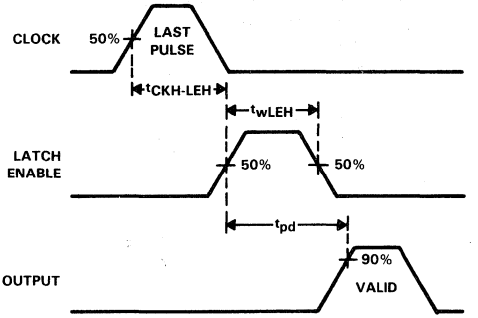

FIGURE 2. OUTPUT SWITCHING TIMES

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THERMAL INFORMATION

DUTY CYCLE
vs
FREE-AIR TEMPERATURE

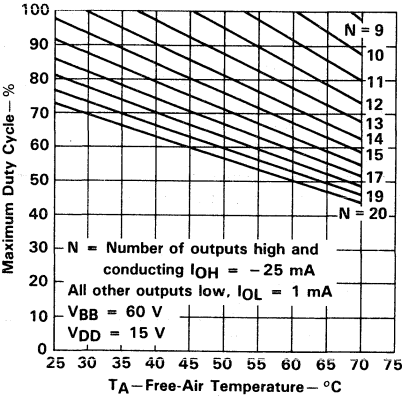


FIGURE 3

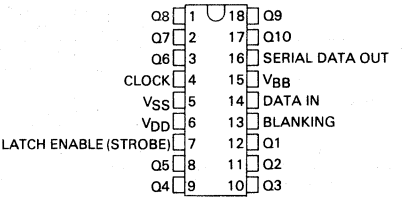
TEXAS INSTRUMENTS

TYPE UCN4810A
VACUUM FLUORESCENT DISPLAY DRIVER

D2676, OCTOBER 1982

- **Each Device Drives 10 Lines**
- **60-V Output Voltage Rating**
- **40-mA Output Source Current**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Latches on All Driver Outputs**
- **Designed to be Interchangeable with Sprague UCN4810A**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

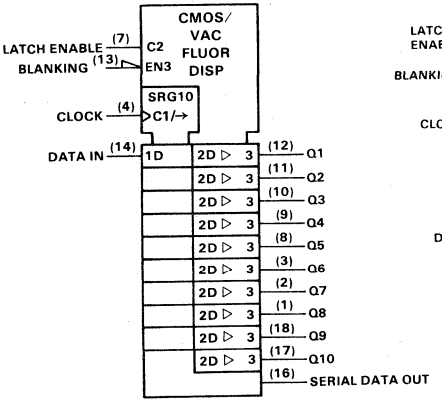
The UCN4810A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and will be latched when the latch enable is low. When the blanking input is high, all outputs are low.

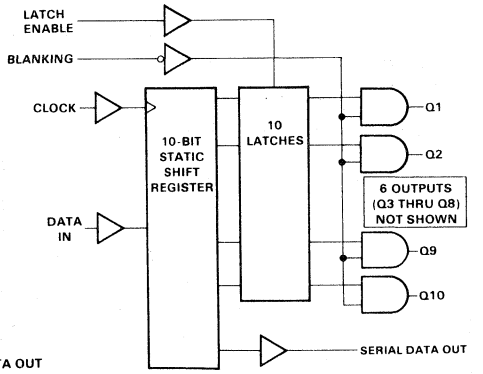
Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 60 volts, and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The UCN4810A is characterized for operation from 0 °C to 70 °C.

logic symbol‡



functional block diagram



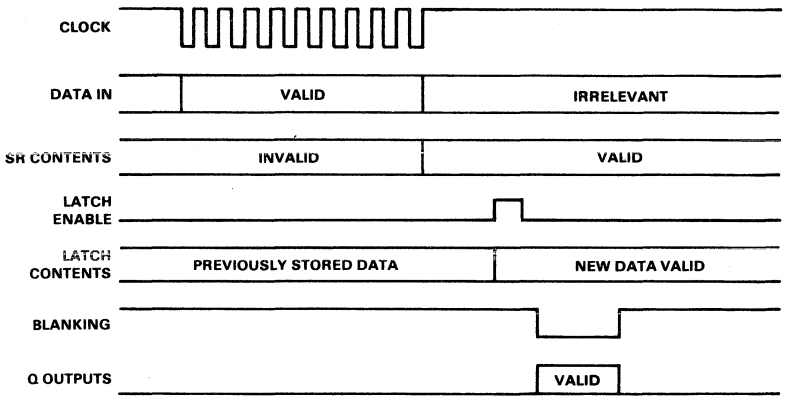
†BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions of IEC and IEEE.

TYPE UCN4810A
VACUUM FLUORESCENT DISPLAY DRIVER

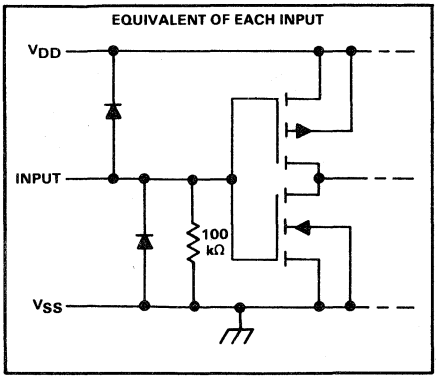
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING	R 1 THRU R10	LC1 THRU LC10§	SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R10*	Determined by Blanking
	No ↑	X	X	No change	Determined by Latch Enable§	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable§	R10	All L
	X	X	L	As determined above	Determined by Latch Enable§	R10	LC1 thru LC12 respectively

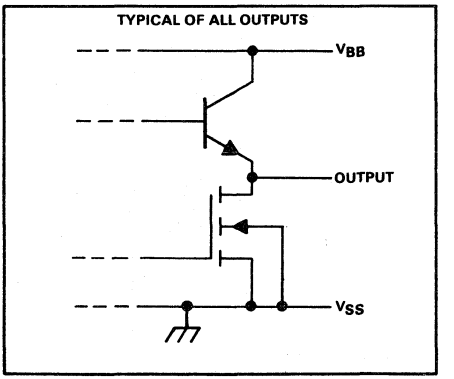
H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
*R10 takes on the state of R9, R9 takes on the state of R8 . . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) ..... 18 V
Driver supply voltage, V_{BB} ..... 60 V
Output voltage ..... 60 V
Input voltage ..... −0.3 V to V_{DD}+0.3 V
Continuous output current ..... −40 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) ..... 1150 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		15.75	V
Supply voltage, V_{BB}		5		60	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3¶		0.8	V
Continuous high-level output current, I_{OH}				−25	mA
Operating free-air temperature, T_A		0		70	°C

¶The algebraic convention, where the less-positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics, V_{DD} = 4.75 V to 15.75 V, V_{BB} = 60 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −25 mA		57.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 μA,	Blanking input at V_{DD}			1	V
I_{OL}	Low-level output current (pull-down current)	V_O = 60 V,	Blanking input at V_{DD}	0.4		0.85	mA
$I_{O(off)}$	Off-state output current	V_O = 60 V, All other terminals open,	V_{SS} = 0 V, T_A = 70°C			15	μA
I_{IH}	High-level input current	V_{DD} = 5 V,	V_I = 5V			0.1	mA
		V_{DD} = 15V,	V_I = 15 V			0.3	
r_i	Input resistance	V_{DD} = 5 V		50			kΩ
r_o	Output resistance	V_{DD} = 5 V				20	kΩ
		V_{DD} = 15V				6	
I_{BB}	Supply current from V_{BB}	All outputs high				13	mA
		All outputs low				1.3	
I_{DD}	Supply current from V_{DD}	All inputs at 0 V, One output high	V_{DD} = 5 V			1	mA
			V_{DD} = 15 V			3	
		All inputs at 0 V, All outputs low	V_{DD} = 5 V			0.1	
			V_{DD} = 15 V			0.2	

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timing requirements for V_{DD} = 5 V and V_{DD} = 15 V, T_A = 0°C to 70°C

PARAMETER	V_{DD} = 5 V		V_{DD} = 15 V		UNIT
	MIN	MAX	MIN	MAX	
Pulse duration, clock high, $t_{w(CKH)}$	1000		250		ns
Pulse duration, latch enable high, $t_{w(LEH)}$	500		300		ns
Setup time, data before clock ↑, $t_{su(D)}$	250		150		ns
Hold time, data after clock ↑, $t_{h(D)}$	250		150		ns
Delay time, clock ↑ to latch enable high, $t_{CKH-LEH}$	1000		400		ns

switching characteristics, V_{DD} = 5 V or 15 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output		1		μs

PARAMETER MEASUREMENT INFORMATION

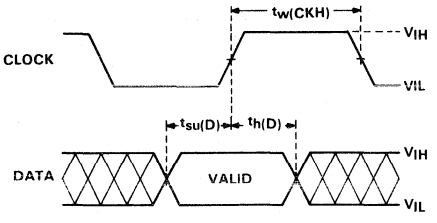


FIGURE 1—INPUT TIMING

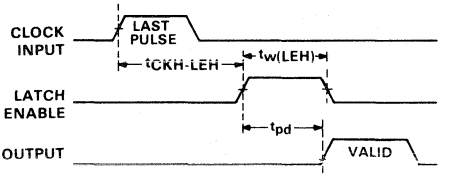
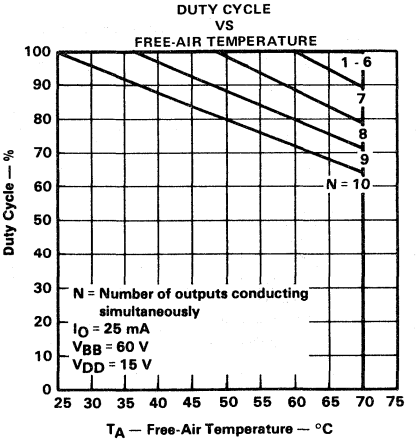


FIGURE 2—OUTPUT SWITCHING TIMES

THERMAL INFORMATION



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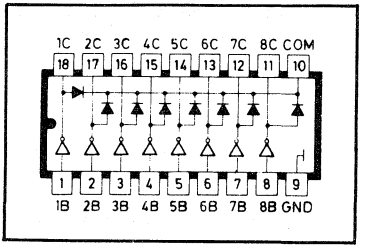
HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500 mA Rated Collector Current (single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible with Various Types of Logic.**
- **Relay Driver Applications**
- **Compatible with ULN2800A-Series from Sprague**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)

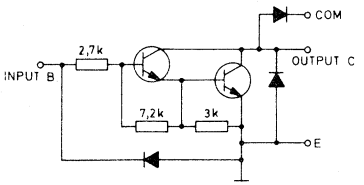


description

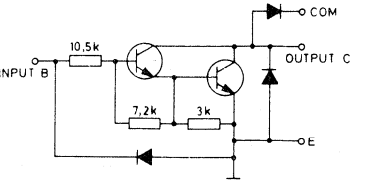
The ULN2803/04 are monolithic high-voltage, high-current darlington transistor arrays. Each comprises eight n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher-current capability.
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers and logic buffers.

The ULN2803A has series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The ULN2804A has an appropriate series input resistor to allow its operation directly from CMOS or PMOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the ULN2803A.

schematics (each darlington pair)



ULN2803A



ULN2804A

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage . . . . . 50 V
Input voltage (see Note 1) . . . . . 30 V
Continuous collector current . . . . . 500 mA
Ouput clamp diode current . . . . . 500 mA
Total substrate-terminal current: N-package . . . . . −2,5 A
Continuous dissipation (total package) at (or below) 25°C free air temperature (see Note 2):
N-package . . . . . 1150 mW
Operating free-air temperature range . . . . . -20 C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds, N-package . . . . . 260°C

NOTES: 1. All voltages values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2803A			ULN2804A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V, I_I = 0			50			50	μA
		2	T_A = 70°C, V_{CE} = 50 V, V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		50	65		μA
$I_{I(ON)}$	Input current	4	V_I = 3,85 V		0.93	1.35				mA
			V_I = 5 V					0,35	0,5	
			V_I = 12 V					1,0	1,45	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V, I_C = 125 mA						5	V
			V_{CE} = 2 V, I_C = 200 mA			2,4			6	
			V_{CE} = 2 V, I_C = 250 mA			2.7				
			V_{CE} = 2 V, I_C = 275 mA						7	
			V_{CE} = 2 V, I_C = 300 mA			3				
			V_{CE} = 2 V, I_C = 350 mA						8	
$V_{CE(sat)}$	Collector emitter saturation voltage	5	I_I = 250 μA, I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA, I_C = 200 mA		1.0	1.3		1.0	1.3	
			I_I = 500 μA, I_C = 350 mA		1.3	1.6		1.3	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V			50			50	μA
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0 V, f = 1 MHz		15	25		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, R_L = 163 Ohm, C_L = 15 pF, See Figure 9		130		ns
t_{PHL}	Propagation delay time, high-to-low-level output			20		ns
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, see Figure 10	V_S-20			mV

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PARAMETER MEASUREMENT INFORMATION

switching characteristics

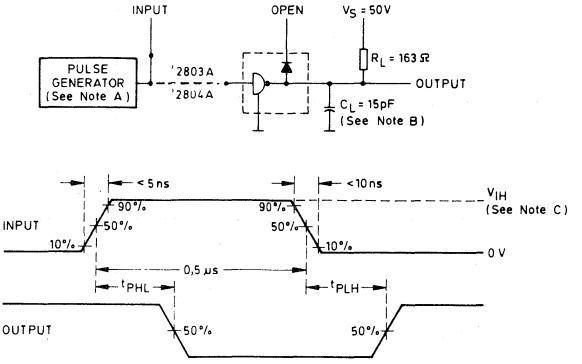

FIGURE 9-PROPOGATION DELAY TIMES

VOLTAGE WAVEFORMS

NOTES: a) The pulse generator has the following characteristics: PRR = 1MHz, Z_{out} = 50 Ω.
b) C_L includes probe and jig capacitance.
c) For testing the ULN2803A, V_{IH} = 3 V; for the ULN2804A, V_{IH} = 8 V.

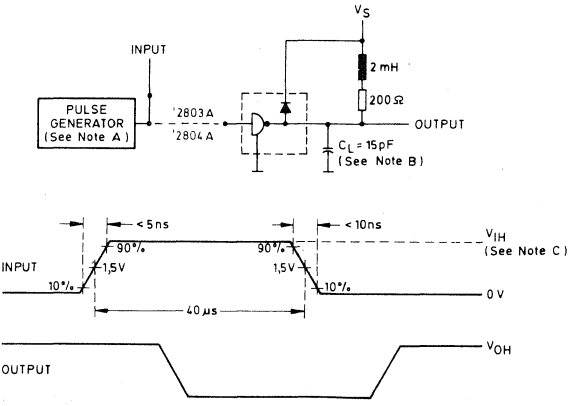

FIGURE 10-LATCH-UP TEST

VOLTAGE WAVEFORMS

NOTES: a) The pulse generator has the following characteristics: PRR = 12,5 kHz, Z_{out} = 50 Ω.
b) C_L includes probe and jig capacitance.
c) For testing the ULN2803A, V_{IH} = 3 V; for the ULN2804A, V_{IH} = 8 V.

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PARAMETER MEASUREMENT INFORMATION

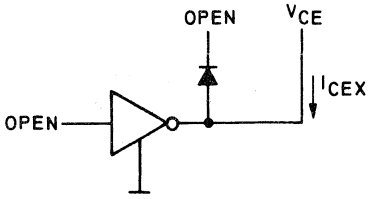

FIGURE 1 - I_{CEX}

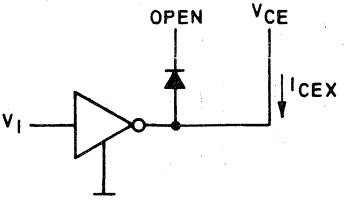

FIGURE 2 - I_{CEX}

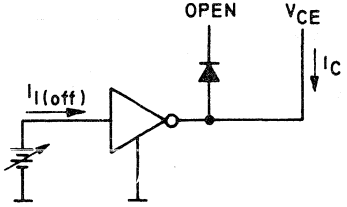

FIGURE 3 - $I_{I(off)}$

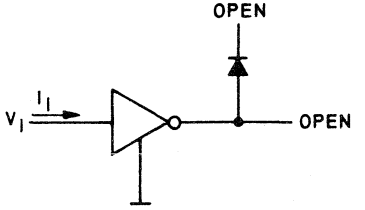

FIGURE 4 - $I_{I(on)}$

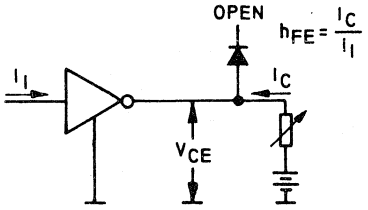

FIGURE 5 - h_{FE}, $V_{CE(sat)}$

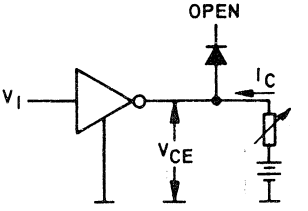

FIGURE 6 - $V_{I(on)}$

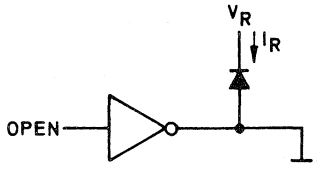

FIGURE 7 - I_R

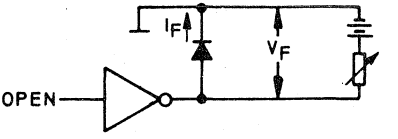

FIGURE 8 - V_F

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PRINTED IN U.K.